



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

74VCX86

Low Voltage Quad 2-Input Exclusive-OR Gate with 3.6V Tolerant Inputs and Outputs

General Description

The VCX86 contains four 2-input exclusive OR gates. This product is designed for low voltage (1.2V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V

The 74VCX86 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

- 1.2V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
3.0 ns max for 3.0V to 3.6V V_{CC}
- Power-off high impedance inputs and outputs
- Static Drive (I_{OH}/I_{OL})
 ± 24 mA @ 3.0V V_{CC}
- Uses proprietary noise/EMI reduction circuitry
- Latchup performance exceeds JEDEC 78 conditions
- ESD performance:
Human body model > 2000V
Machine model > 250V
- Leadless Pb-Free DQFN package

Ordering Code:

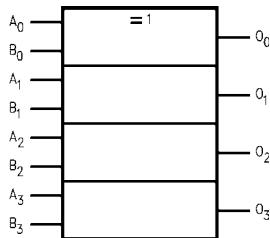
Order Number	Package Number	Package Description
74VCX86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VCX86BQX (Note 1)	MLP014A	Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74VCX86MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
 Pb-Free package per JEDEC J-STD-020B.

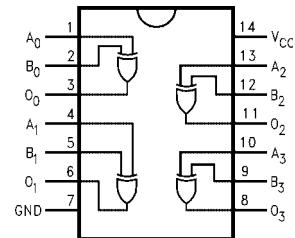
Note 1: DQFN package available in Tape and Reel only.

Logic Symbol

IEEE/IEC

**Connection Diagrams**

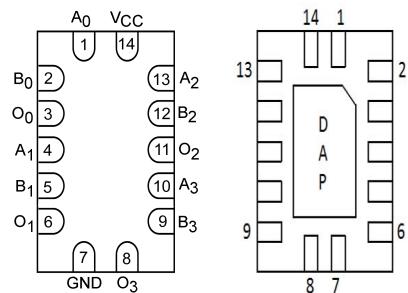
Pin Assignments for SOIC and TSSOP

**Pin Descriptions**

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs
DAP	No Connect

Note: DAP (Die Attach Pad)

Pad Assignments for DQFN



(Top View)

(Bottom View)

Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions (Note 4)			
Supply Voltage (V_{CC})	-0.5V to +4.6V	Power Supply			
DC Input Voltage (V_I)	-0.5V to +4.6V	Operating	1.2V to 3.6V		
Output Voltage (V_O)		Input Voltage	-0.3V to +3.6V		
HIGH or LOW State (Note 3)	-0.5V to V_{CC} +0.5V	Output Voltage (V_O)			
$V_{CC} = 0V$	-0.5V to +4.6V	HIGH or LOW State	0V to V_{CC}		
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA	Output Current in I_{OH}/I_{OL}			
DC Output Diode Current (I_{OK})		$V_{CC} = 3.0V$ to 3.6V	±24 mA		
$V_O < 0V$	-50 mA	$V_{CC} = 2.3V$ to 2.7V	±18 mA		
$V_O > V_{CC}$	+50 mA	$V_{CC} = 1.65V$ to 2.3V	±6 mA		
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA	$V_{CC} = 1.4V$ to 1.6V	±2 mA		
DC V_{CC} or GND Current per Supply Pin (I_{CC} or Ground)	±100 mA	$V_{CC} = 1.2V$	±100 μ A		
Storage Temperature Range (T_{STG})	-65°C to +150°C	Free Air Operating Temperature (T_A)	-40°C to +85°C		
		Minimum Input Edge Rate ($\Delta t/\Delta V$)			
		$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V		
Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.					
Note 3: I_O Absolute Maximum Rating must be observed.					
Note 4: Floating or unused inputs must be held HIGH or LOW.					
DC Electrical Characteristics					
Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0	
			2.3 - 2.7	1.6	
			1.65 - 2.3	0.65 × V_{CC}	
			1.4 - 1.6	0.65 × V_{CC}	
			1.2	0.65 × V_{CC}	
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		
			2.3 - 2.7		0.8
			1.65 - 2.3		0.7
			1.4 - 1.6		0.35 × V_{CC}
			1.2		0.35 × V_{CC}
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7 - 3.6	$V_{CC} - 0.2$	
		$I_{OH} = -12 mA$	2.7	2.2	
		$I_{OH} = -18 mA$	3.0	2.4	
		$I_{OH} = -24 mA$	3.0	2.2	
		$I_{OH} = -100 \mu A$	2.3 - 2.7	$V_{CC} - 0.2$	
		$I_{OH} = -6 mA$	2.3	2.0	
		$I_{OH} = -12 mA$	2.3	1.8	
		$I_{OH} = -18 mA$	2.3	1.7	
		$I_{OH} = -100 \mu A$	1.65 - 2.3	$V_{CC} - 0.2$	
		$I_{OH} = -6 mA$	1.65	1.25	
		$I_{OH} = -100 \mu A$	1.4 - 1.6	$V_{CC} - 0.2$	
		$I_{OH} = -2 mA$	1.4	1.05	
		$I_{OH} = -100 \mu A$	1.2	$V_{CC} - 0.2$	

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μ A	2.7 - 3.6		0.2	V
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 18 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
	I _{OL} = 100 μ A	I _{OL} = 100 μ A	2.3 - 2.7		0.2	
		I _{OL} = 12 mA	2.3		0.4	
		I _{OL} = 18 mA	2.3		0.6	
	I _{OL} = 100 μ A	I _{OL} = 100 μ A	1.65 - 2.3		0.2	
		I _{OL} = 6 mA	1.65		0.3	
	I _{OL} = 100 μ A	I _{OL} = 100 μ A	1.4 - 1.6		0.2	
		I _{OL} = 2 mA	1.4		0.35	
		I _{OL} = 100 μ A	1.2		0.05	
I _I	Input Leakage Current	0 \leq V _I \leq 3.6V	1.2 - 3.6		\pm 5.0	μ A
I _{OFF}	Power-OFF Leakage Current	0 \leq (V _I , V _O) \leq 3.6V	0		10	μ A
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND V _{CC} \leq (V _I)	1.2 - 3.6 1.2 - 3.6		20 \pm 20	μ A
Δ I _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} -0.6V	2.7 - 3.6		750	μ A

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PHL} t _{PLH}	Propagation Delay	C _L = 30 pF, R _L = 500 Ω	3.3 \pm 0.3	0.6	3.0	ns	Figures 1, 2
			2.5 \pm 0.2	0.8	3.9		
			1.8 \pm 0.15	1.0	7.8		
		C _L = 15 pF, R _L = 2k Ω	1.5 \pm 0.1	1.0	15.6		Figures 3, 4
			1.2	1.5	39		
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 6)	C _L = 30 pF, R _L = 500 Ω	3.3 \pm 0.3		0.5	ns	
			2.5 \pm 0.2		0.5		
			1.8 \pm 0.15		0.75		
		C _L = 15 pF, R _L = 2k Ω	1.5 \pm 0.1		1.5		
			1.2		1.5		

Note 5: For C_L = 50pF, add approximately 300 ps to the AC maximum specification.

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

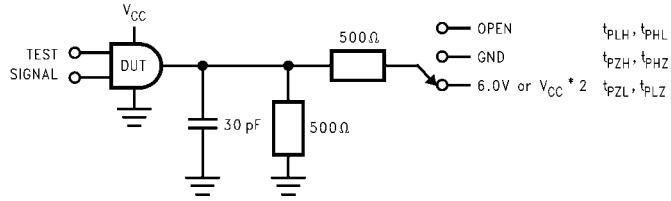
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
			Typical	
C _{IN}	Input Capacitance	V _{CC} = 1.8, 2.5V or 3.3V, V _I = 0V or V _{CC}	6	pF
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)



TEST	SWITCH
t _{PLH} , t _{PHL}	Open

FIGURE 1. AC Test Circuit

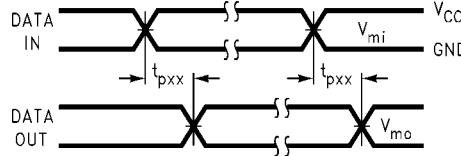
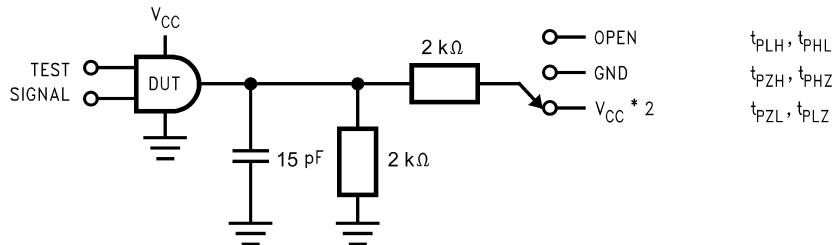


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

Symbol	V _{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V _{mi}	1.5V	V _{CC} /2	V _{CC} /2
V _{mo}	1.5V	V _{CC} /2	V _{CC} /2

AC Loading and Waveforms ($V_{CC} 1.5V \pm 0.1V$ to $1.2V$)

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZH}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5 \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

FIGURE 3. AC Test Circuit

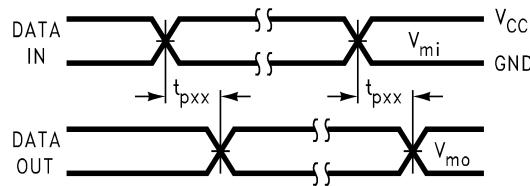


FIGURE 4. Waveform for Inverting and Non-Inverting Functions

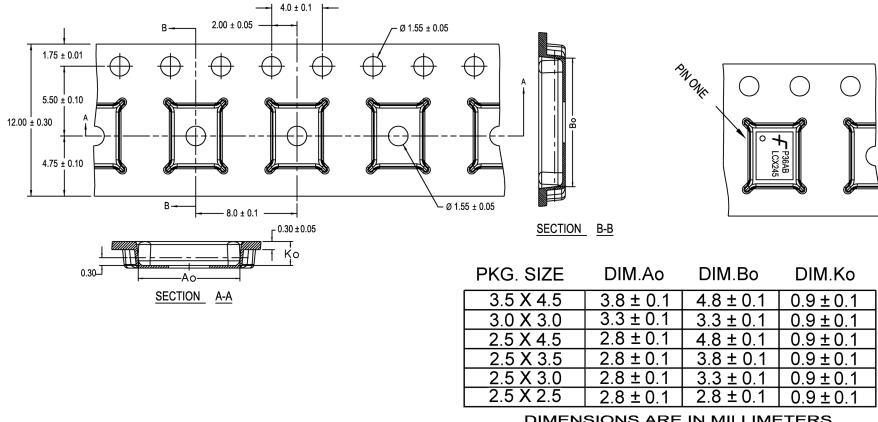
Symbol	V_{CC}
$1.5V \pm 0.1V$	
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$

Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

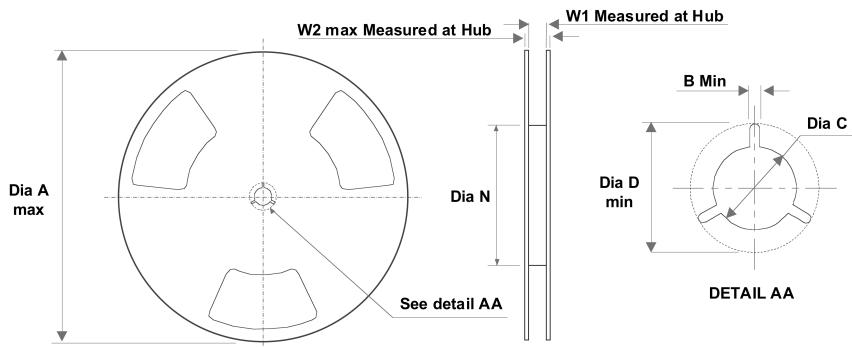
TAPE DIMENSIONS inches (millimeters)



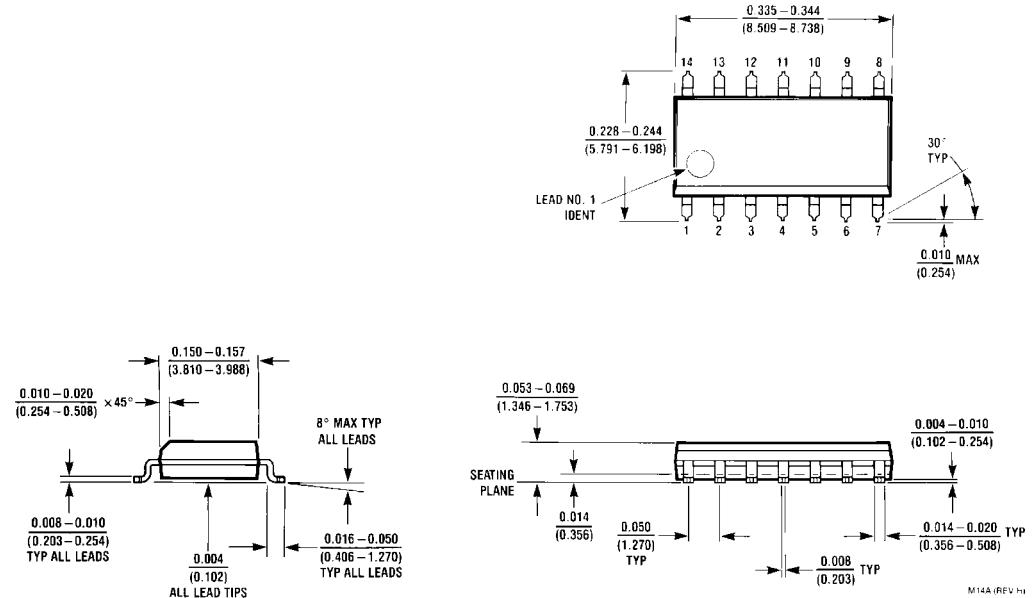
NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

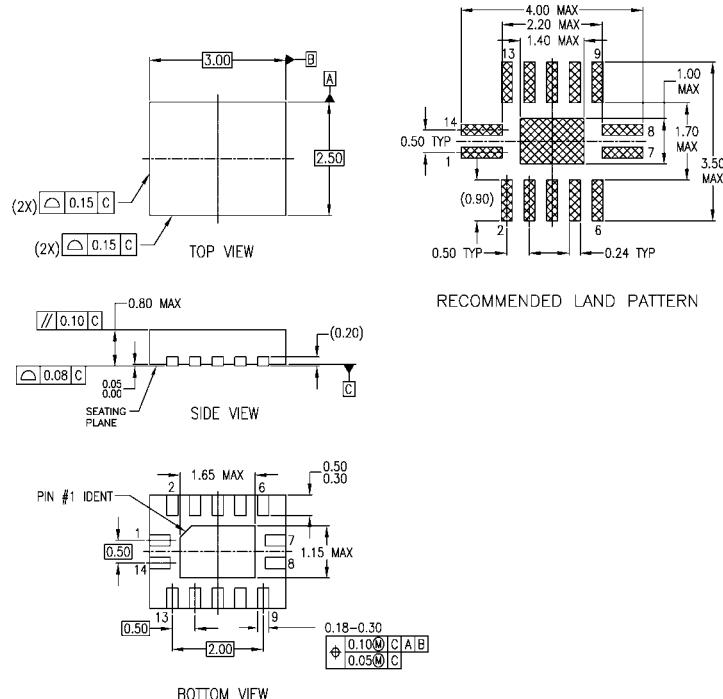
REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



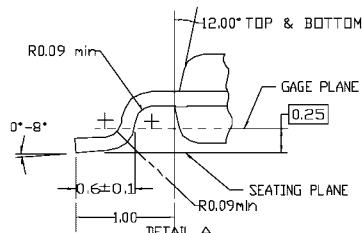
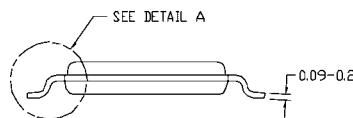
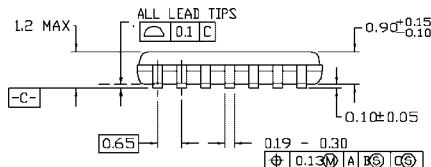
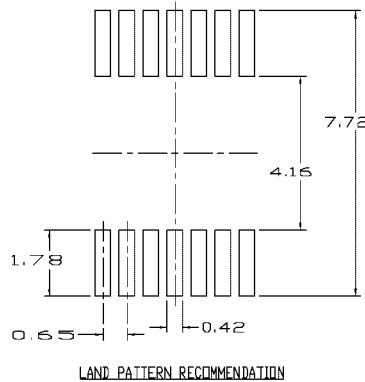
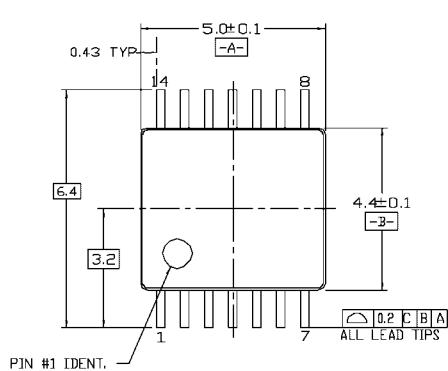
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP014ArevA

Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
Package Number MLP014A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor](#):

[74VCX86MTCX](#) [74VCX86BQX](#) [74VCX86MTC](#)