3-volt single-chip microcontroller peripheral PSD313L

T-49-19-63

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 3.0 to 5.5 Volt Operation
- ❑ 19 Individually Configurable I/O pins that can be used as:
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 18 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8-bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — $\overline{PSEN}$ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 1M bit of UV EPROM
  - — Configurable as 128K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 16K x 8
  - — 250 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8
  - — 250 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (e.g., Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ CMiser-Bit
  - — Programmable option to further reduce power consumption
- ❑ Built-In Security
  - — Locks the PSD313L and PAD Decoding Configuration
- ❑ Available in a Choice of Packages
  - — 44 Pin PLDCC and CLDCC
- ❑ Simple Menu-Driven Software: Configure the PSD313L on an IBM PC
- ❑ Pin and Functionally Compatible with the PSD3XX and PSD3XXL Series

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERAMIC	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	°C
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0° C to +70°C	3.0 V to 5.5 V

Recommended Operating Conditions

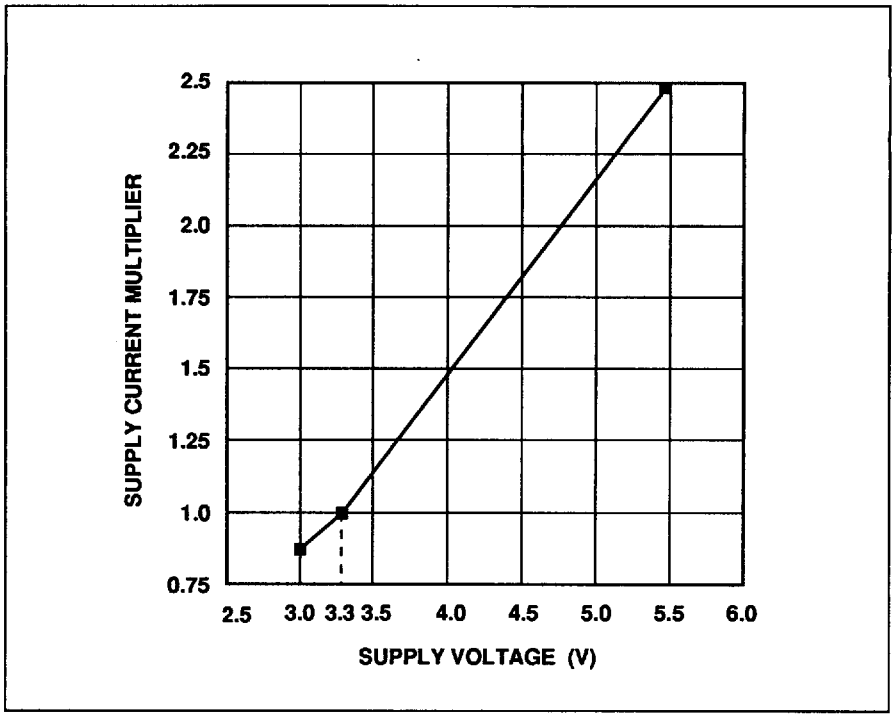
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	3.0	3.3	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IL}	Low-level Input Voltage	V_{CC} = 3.0 V to 5.5 V	– 0.5		0.3 V_{CC}	V

DC Characteristics

Symbol	Parameter	Conditions				CMiser = 1 Subtract:			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 3.0 V		0.01	0.1				V
		I_{OL} = 4 mA V_{CC} = 3.0 V		0.15	0.4				V
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 3.0 V	2.9	2.99					V
		I_{OH} = –1 mA V_{CC} = 3.0 V	2.4	2.6					V
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 2 and 3)	V_{CC} = 3.3 V		1	5				µA
I_{CC1}	Active Current (CMOS) (No Internal Memory Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		3.0	5	mA
		V_{CC} = 3.3 V (Note 6)		10	20		3.0	5	mA
I_{CC2}	Active Current (CMOS) (EPROM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		6	12		2	3	mA
		V_{CC} = 3.3 V (Note 6)		10	20		2	3	mA
I_{CC3}	Active Current (CMOS) (SRAM Block Selected) (Notes 2 and 5)	V_{CC} = 3.3 V (Note 5)		20	33		5	8	mA
		V_{CC} = 3.3 V (Note 6)		24	40		5	8	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND	–1	±0.1	1				µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND	–10	±5	10				µA

NOTES: 2. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
3. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
4. Add 2.0 mA/MHz for AC power component (power = AC + DC).
5. Ten (10) PAD product terms active. (Add 190 µA per product term, typical, or 240 µA per product term maximum.)
6. Forty (40) PAD product terms active.

Figure 1. Normalized Supply Current vs. Supply Voltage



The Normalized Supply Current vs. Supply Voltage graph shown above, provides a multiplier for any I_{SB} or I_{CC} value in the D.C. Characteristics table. As noted, it is normalized for a supply voltage of 3.3 volts. Since device characterization data shows very little supply current difference over speed, the multiplier includes all frequencies of operation from standby to quiescent to full dynamic speed. To use, calculate the supply current at 3.3 volts for your operation configuration using the D.C. Characteristics table. Then multiply that value by the Supply Current Multiplier for the supply voltage actually being used.

AC Characteristics[8] (See Timing Diagrams)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T1	ALE or AS Pulse Width	75		80			ns
T2	Address Set-up Time	30		35			ns
T3	Address Hold Time	30		35		0	ns
T4	Leading Edge of Read to Data Active	0		0		0	ns
T5	ALE Valid to Data Valid		250		300	25	ns
T6	Address Valid to Data Valid		250		300	25	ns
T7	$\overline{CSI}$ Active to Data Valid		275		325	30	ns
T8	Leading Edge of Read to Data Valid		90		95	0	ns
T9	Read Data Hold Time	0		0		0	ns
T10	Trailing Edge of Read to Data High-Z		50		55	0	ns
T11	Trailing Edge of ALE or AS to Leading Edge of Write		40		45		ns
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	100		110		0	ns
T12A	$\overline{WR}$ Pulse Width	90		95		0	ns
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0	ns
T14	Address Valid to Trailing Edge of Write	250		300		0	ns
T15	$\overline{CSI}$ Active to Trailing Edge of Write	275		375		0	ns
T16	Write Data Set-up Time	60		65		0	ns
T17	Write Data Hold Time	25		30		0	ns
T18	Port to Data Out Valid Propagation Delay		70		75	0	ns
T19	Port Input Hold Time	0		0		0	ns
T20	Trailing Edge of Write to Port Output Valid	100		110		0	ns
T21	ADi or Control to $\overline{CSOi}$ Valid	6	80	5	85	0	ns
T22	ADi or Control to $\overline{CSOi}$ Invalid	4	80	4	85	0	ns
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		70		75	0	ns
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		100		110	0	ns

NOTE: 8. These AC Characteristics are for VCC = 3.0 – 3.6V.

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AC Characteristics (Cont.)

Symbol	Parameter	-25		-30		CMiser = 1 Add:	Unit
		Min	Max	Min	Max		
T24	Track Mode Trailing Edge of ALE or AS to Address High-Z		60		65	0	ns
T25	Track Mode Read Propagation Delay		70		75	0	ns
T26	Track Mode Read Hold Time	10	70	10	75		ns
T27	Track Mode Write Cycle, Data Propagation Delay		60		65	0	ns
T28	Track Mode Write Cycle, Write to Data Propagation Delay	7	80	7	85	0	ns
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	4		4		0	ns
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	110	8	120	0	ns
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	110	8	120	0	ns
T32	Direct PAD Input as Hold Time	24		30		0	ns
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	60		65		0	ns
T34	E or $\overline{DS}$ End to R/W	60		65		0	ns
T35	AS Inactive to E high	40		45		0	ns
T36	Address to Leading Edge of Write	50		60		0	ns

NOTES: 9. ADi = any address line.
10. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
11. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
12. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 2. AC Testing Input/Output Waveform

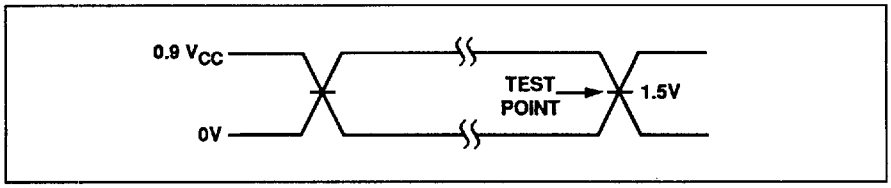


Figure 3. AC Testing Load Circuit

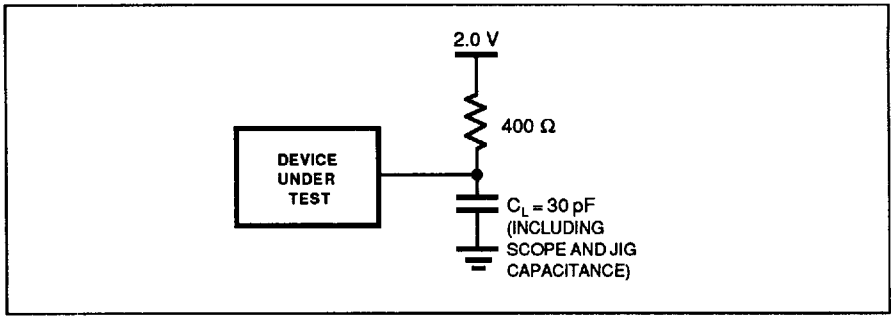


Figure 4. The Reset Cycle (RESET)

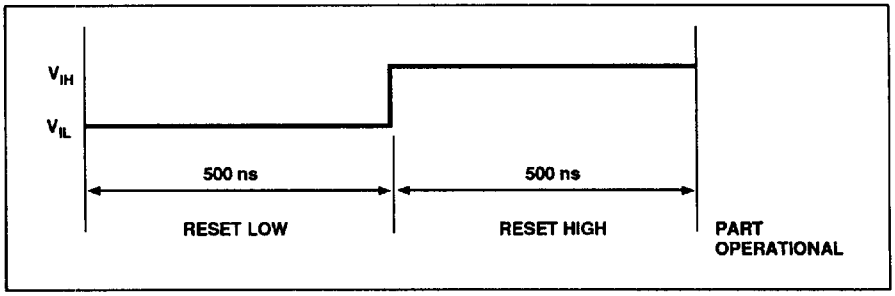
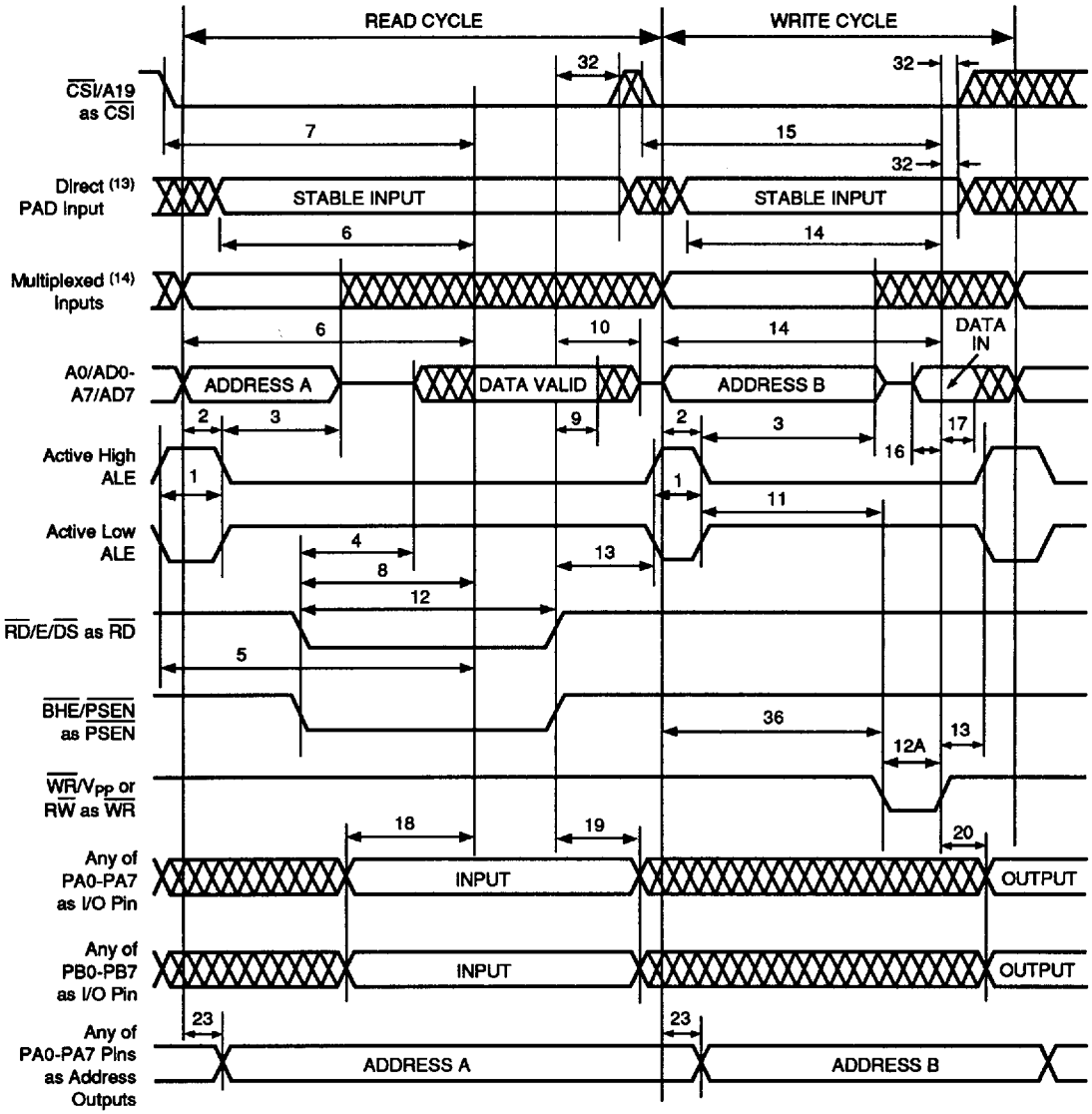
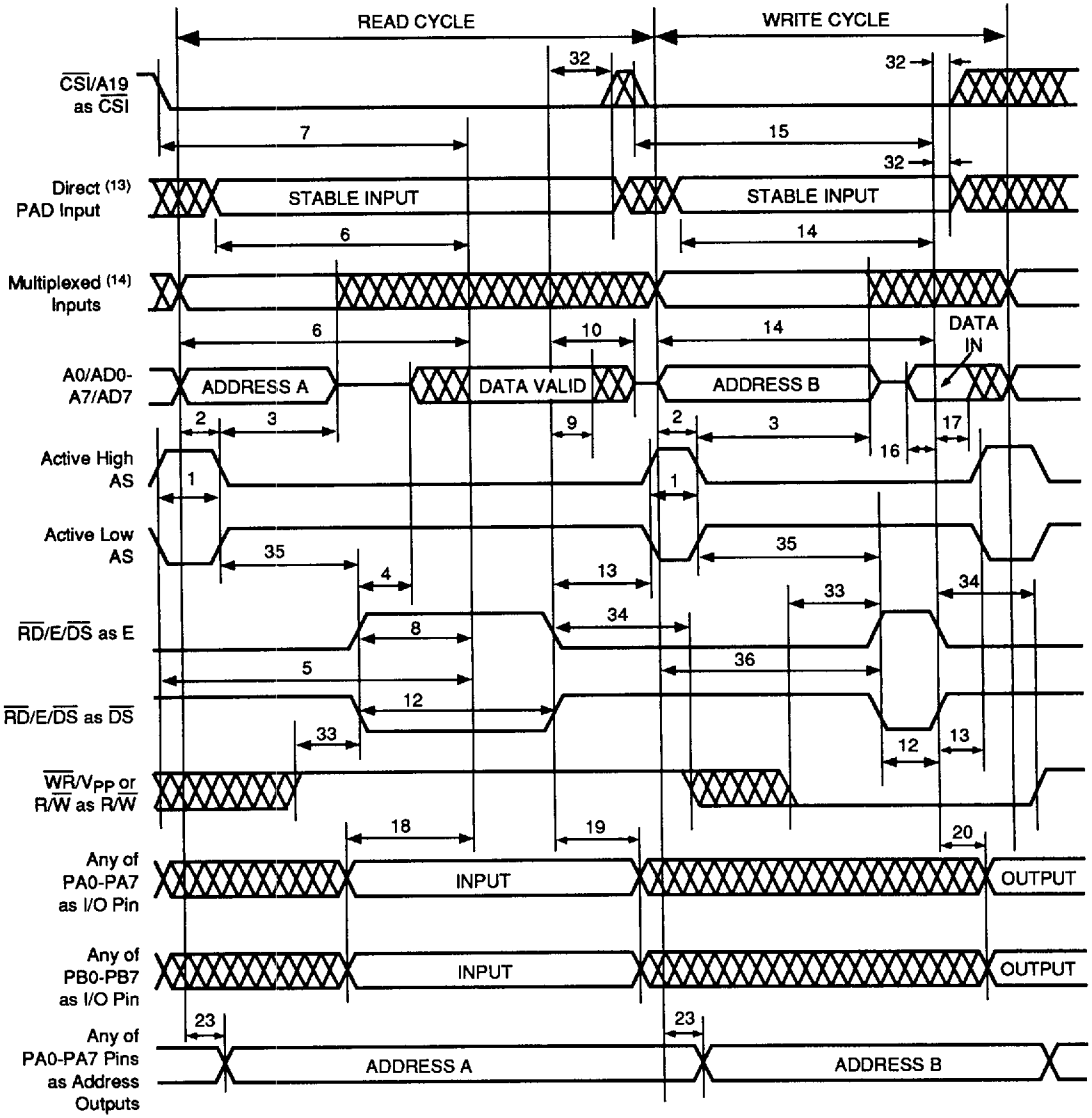


Figure 5. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



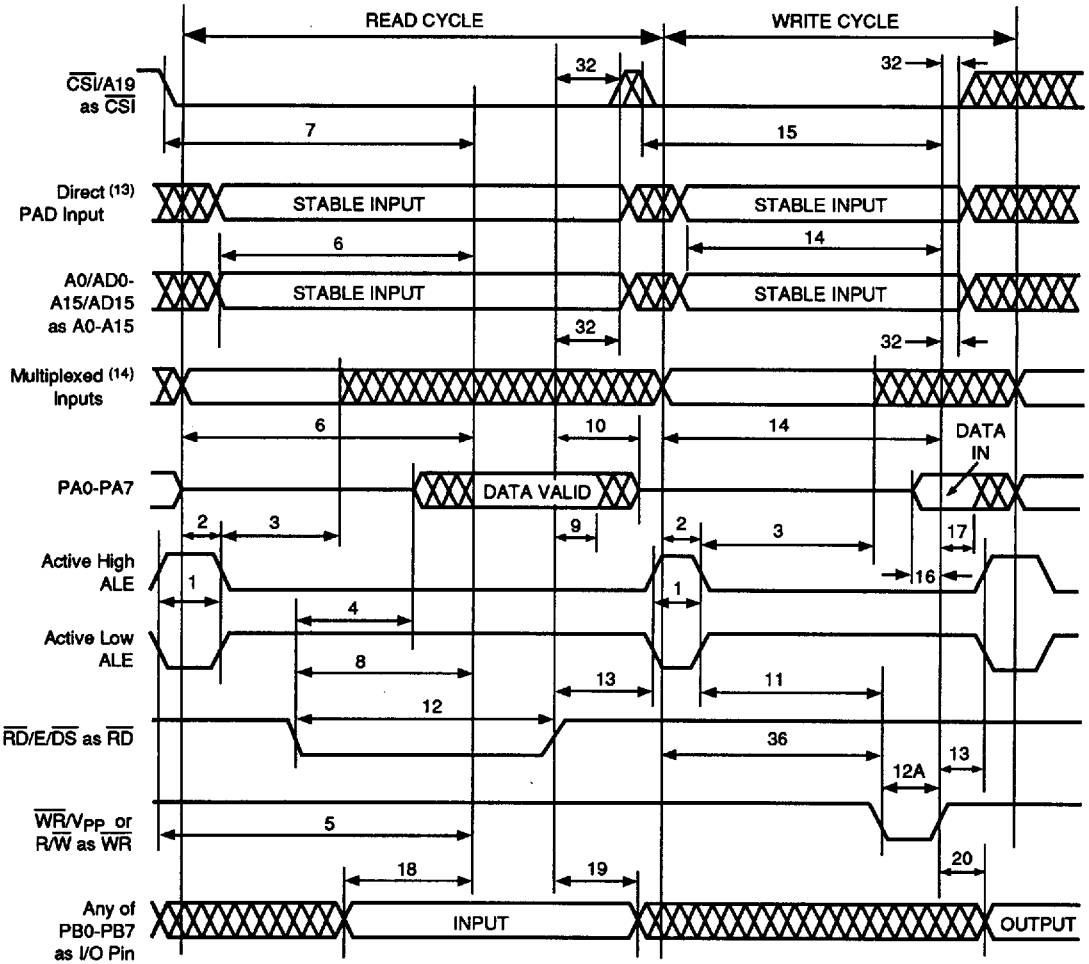
See referenced notes on page 296.

Figure 6. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



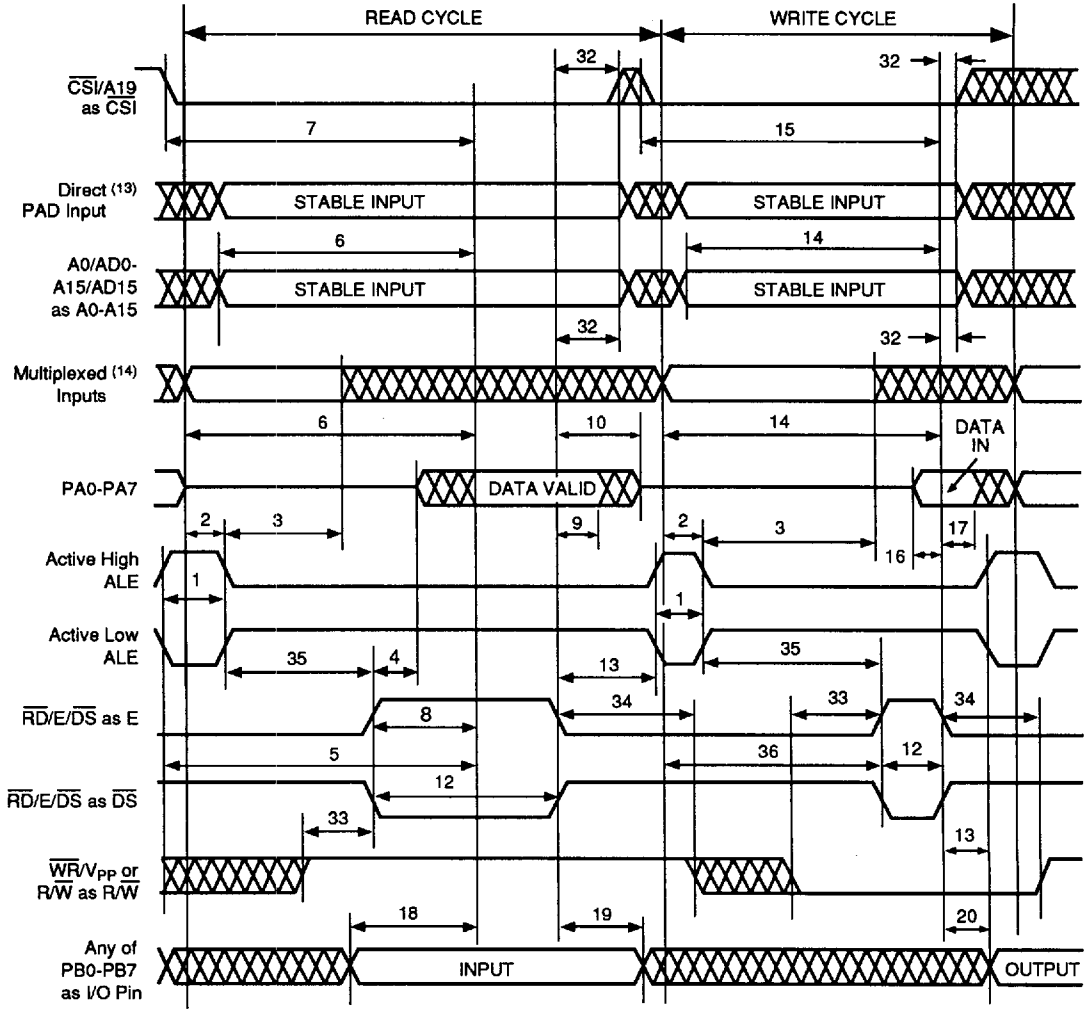
See referenced notes on page 296.

Figure 7. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



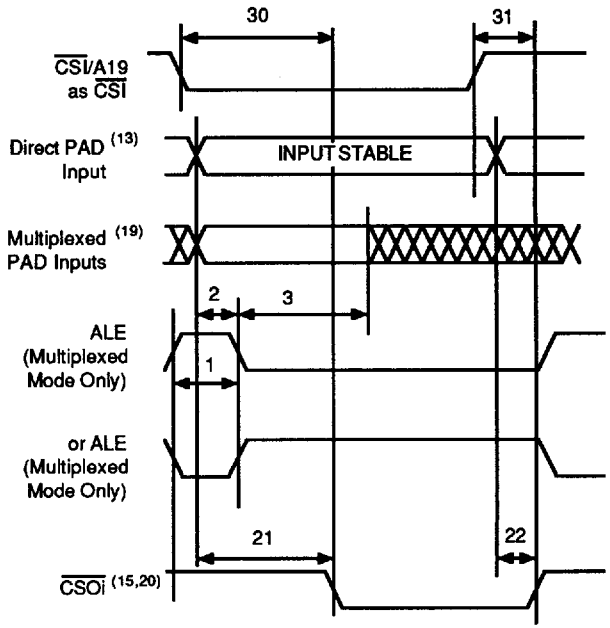
See referenced notes on page 296.

Figure 8. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



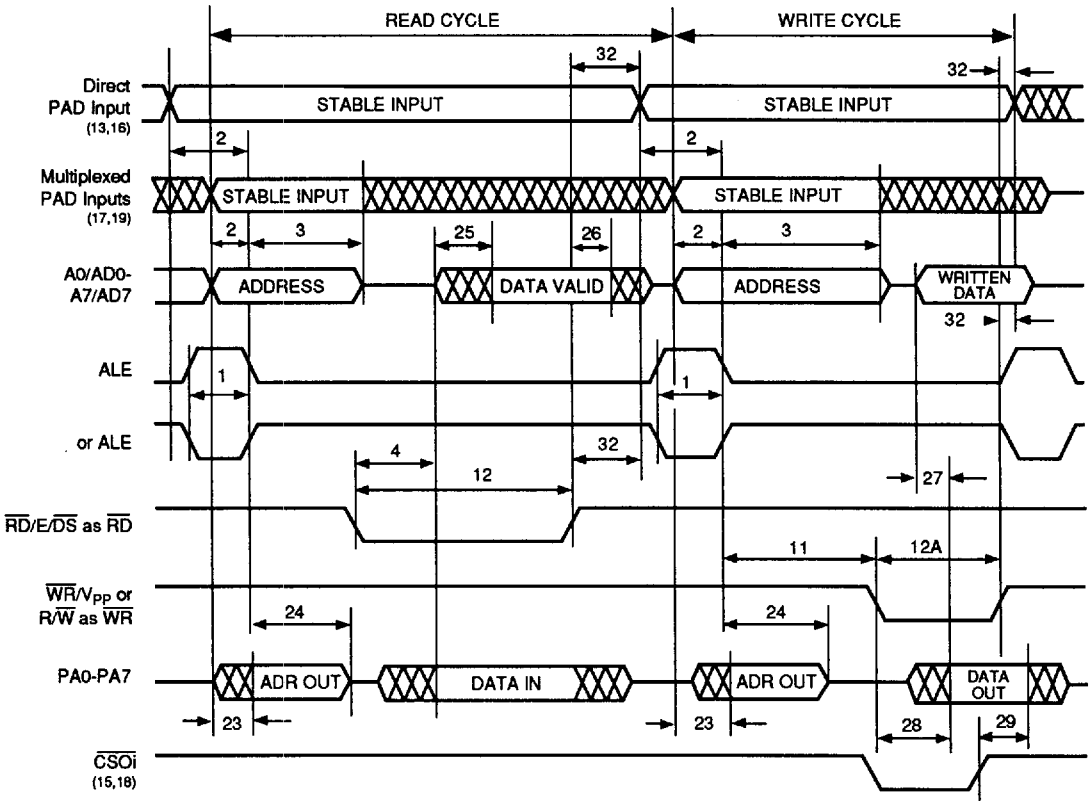
See referenced notes on page 296.

Figure 9. Chip-Select Output Timing



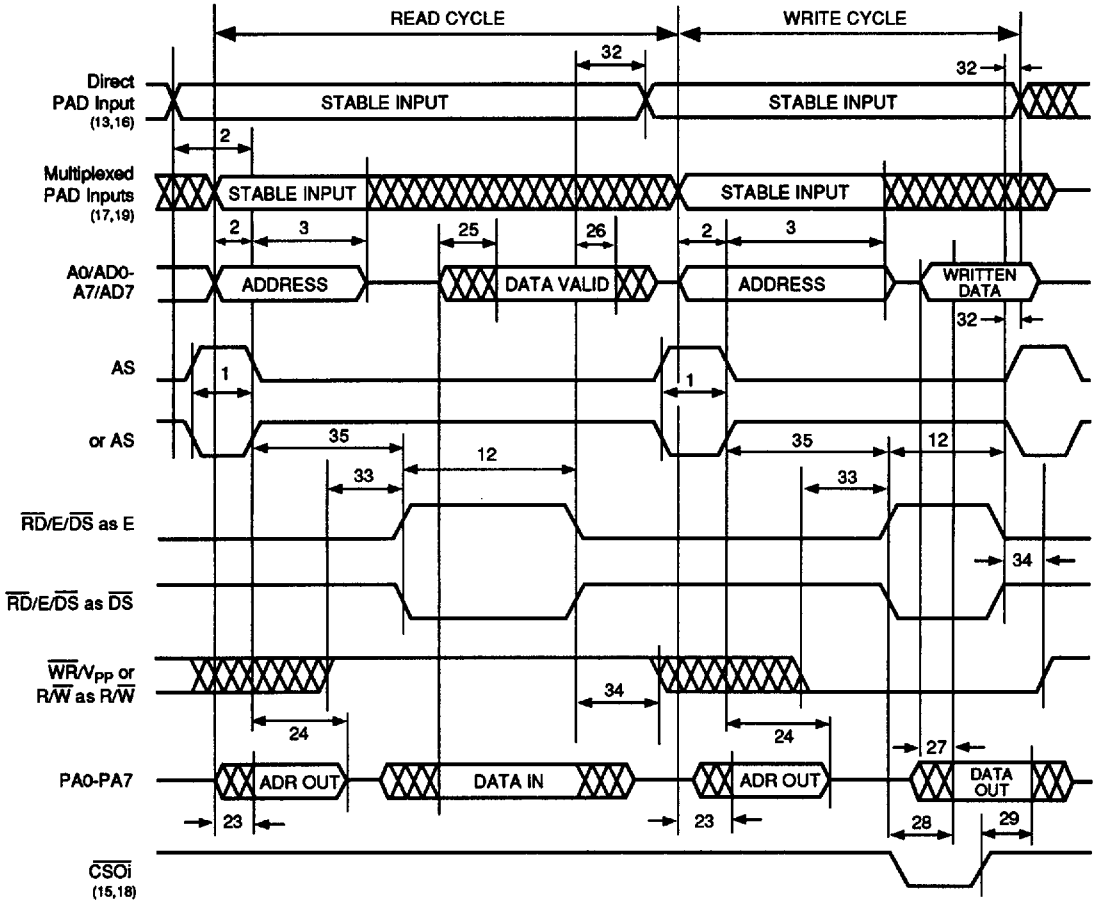
See referenced notes on page 296.

Figure 10. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 296.

Figure 11. Port A as AD0 – AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

13. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
14. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–$\overline{A15}$/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
15. CSOi = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
16. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
17. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
18. The write operation signals are included in the $\overline{CSOi}$ expression.
19. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
20. $\overline{CSOi}$ product terms can include any of the PAD input signals except for reset and $\overline{CSI}$.

Pin Capacitance[21]

$T_A = 25°C$, $f = 1$ MHz

Symbol	Parameter	Conditions	Typical[22]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 21. This parameter is only sampled and is not 100% tested.
22. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD313L and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery, or after each erasure, the PSD313L device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Pin Assignments

Pin Name	44-Pin PLDCC/CLDCC Package
$\overline{PSEN}$	1
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2
$\overline{RESET}$	3
PB7	4
PB6	5
PB5	6
PB4	7
PB3	8
PB2	9
PB1	10
PB0	11
GND	12
ALE or AS	13
PA7	14
PA6	15
PA5	16
PA4	17
PA3	18
PA2	19
PA1	20
PA0	21
$\overline{RD}$/E/$\overline{DS}$	22
AD0/A0	23
AD1/A1	24
AD2/A2	25
AD3/A3	26
AD4/A4	27
AD5/A5	28
AD6/A6	29
AD7/A7	30
A8	31
A9	32
A10	33
GND	34
A11	35
A12	36
A13	37
A14	38
A15	39
PC0	40
PC1	41
PC2	42
A19/$\overline{CSI}$	43
V_{CC}	44

Package Information

Figure 12. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLCC) with Window (Package Type L)

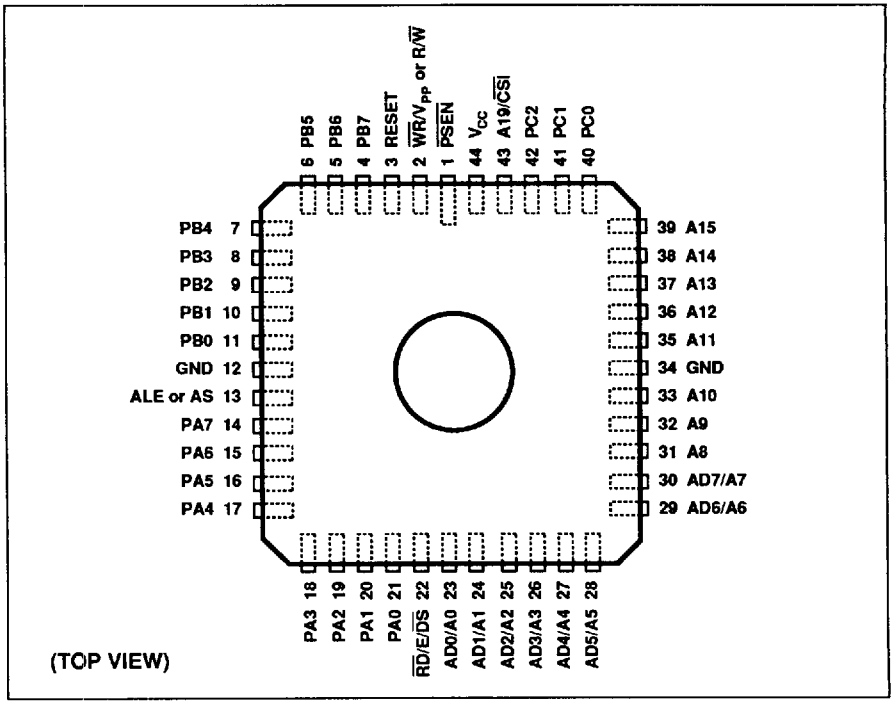
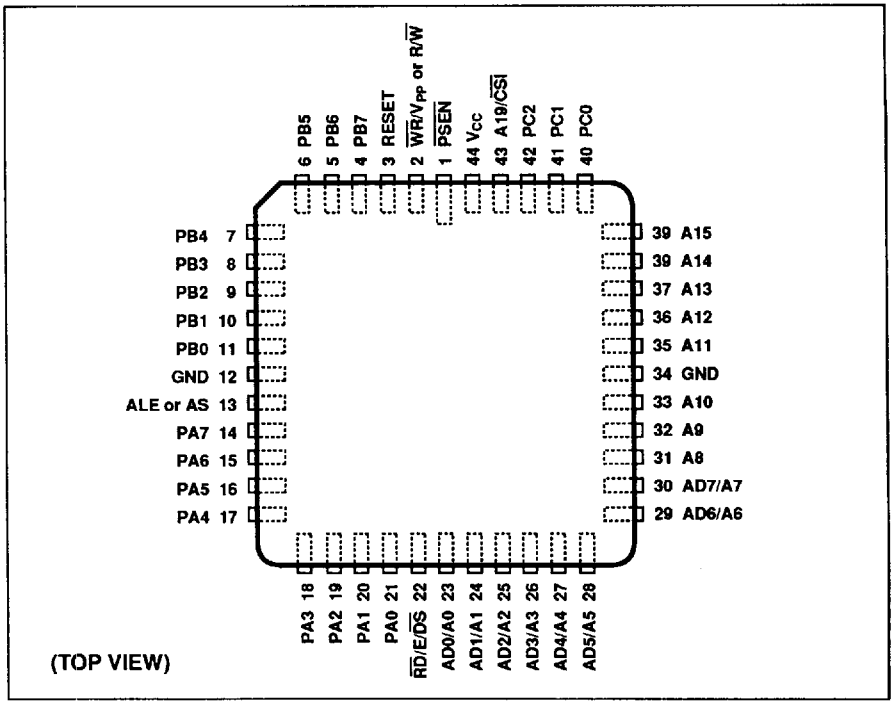


Figure 13. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)



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Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	Manufacturing Procedure
PSD313L25 A	250	44-pin PLCC	J2	Commercial	Standard
PSD313L25 KA	250	44-pin CLCC	L4	Commercial	Standard
PSD313L30 A	300	44-pin PLCC	J2	Commercial	Standard
PSD313L30 KA	300	44-pin CLCC	L4	Commercial	Standard