Product data sheet

1. General description

The HEF4071B is a quad 2-input OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

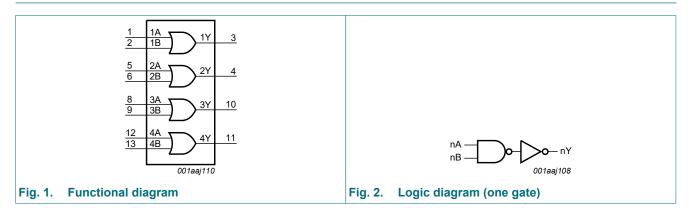
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- · CMOS low power dissipation
- · High noise immunity
- Standardized symmetrical output characteristics
- · Inputs and outputs are protected against electrostatic effects
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
HEF4071BT	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			

4. Functional diagram

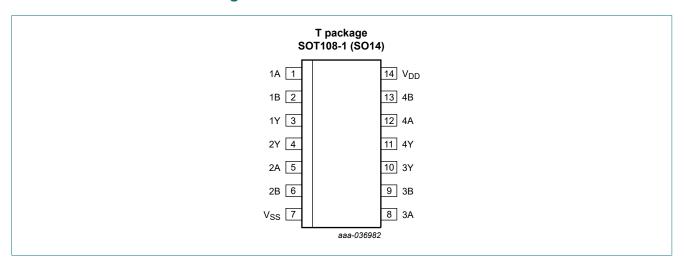




Quad 2-input OR gate

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description				
1A , 2A, 3A, 4A	1, 5, 8, 12	input				
1B, 2B, 3B, 4B	2, 6, 9, 13	input				
1Y, 2Y, 3Y, 4Y	3, 4, 10, 11	output				
V _{SS}	7	ground (0 V)				
V_{DD}	14	supply voltage				

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Input	Output	
nA	nB	nY
L	L	L
L	Н	Н
Н	L	Н
Н	Н	Н

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0 \text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
VI	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V_{O} < -0.5 V or V_{O} > V_{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C [1]	-	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
VI	input voltage		0	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	3.75	μs/V
		V _{DD} = 10 V	-	0.5	μs/V
		V _{DD} = 15 V	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0 \ V$; $V_I = V_{SS}$ or V_{DD} , unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	-40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} = -	+125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
	voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input	nput I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
	voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level IIO output voltage	thut voltage	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V

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Symbol	Parameter	Conditions V	V_{DD}	T _{amb} =	-40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} =	Unit	
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{OL}	LOW-level	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
	output current	V _O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I _{OL}	LOW-level	V _O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
	output current	V _O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V _O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
l _l	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μΑ
I _{DD}	supply current	all valid input	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μΑ
		combinations; I _O = 0 A	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μΑ
		10 - 0 A	15 V	-	1.0	-	1.0	-	30.0	-	30.0	μΑ
C _I	input capacitance			-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

 T_{amb} = 25 °C, unless otherwise specified. For waveforms see Fig. 3; for test circuit see Fig. 4.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	nA or nB to nY	5 V	28 ns + (0.55 ns/pF)C _L	-	55	115	ns
	propagation delay		10 V	15 ns + (0.23 ns/pF)C _L	-	25	50	ns
			15 V	12 ns + (0.16 ns/pF)C _L	-	20	35	ns
t _{PLH}	LOW to HIGH	nA or nB to nY	5 V	18 ns + (0.55 ns/pF)C _L	-	45	90	ns
	propagation delay		10 V	9 ns + (0.23 ns/pF)C _L	-	20	45	ns
			15 V	7 ns + (0.16 ns/pF)C _L	-	15	30	ns
t _t	transition time		5 V [2]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V [2]	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V [2]	6 ns + (0.28 ns/pF)C _L	-	20	40	ns

^[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 8. Dynamic power dissipation

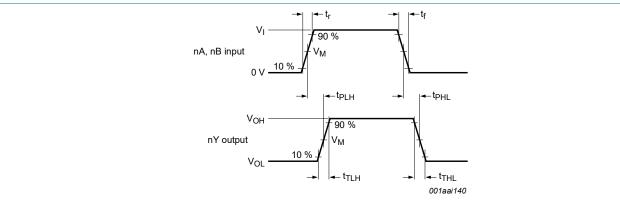
 $V_{SS} = 0 \ V; \ t_r = t_f \le 20 \ ns; \ T_{amb} = 25 \ ^{\circ}C.$

Symbol	Parameter	V_{DD}	Typical formula	where:
P_D	dynamic power dissipation	5 V	$P_D = 1150 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2 (\mu W)$	
		10 V		f _o = output frequency in MHz; C _L = output load capacitance in pF;
		15 V	$P_{D} = 19700 \times f_{i} + \Sigma (f_{o} \times C_{L}) \times V_{DD}^{2}$	$\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.

^[2] t_t is the same as t_{THL} and t_{TLH} .

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10.1. Waveforms and test circuit



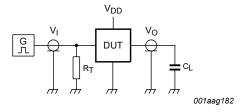
Measurement points are given in <u>Table 9</u>.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V _M	V _M
5 V to 15 V	$0.5 \times V_{DD}$	0.5 × V _{DD}



Test data is given in Table 10.

Definitions test circuit:

 C_L = load capacitance including jig and probe capacitance;

 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 4. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load	
V_{DD}	V _I	t _r , t _f	CL
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

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11. Package outline

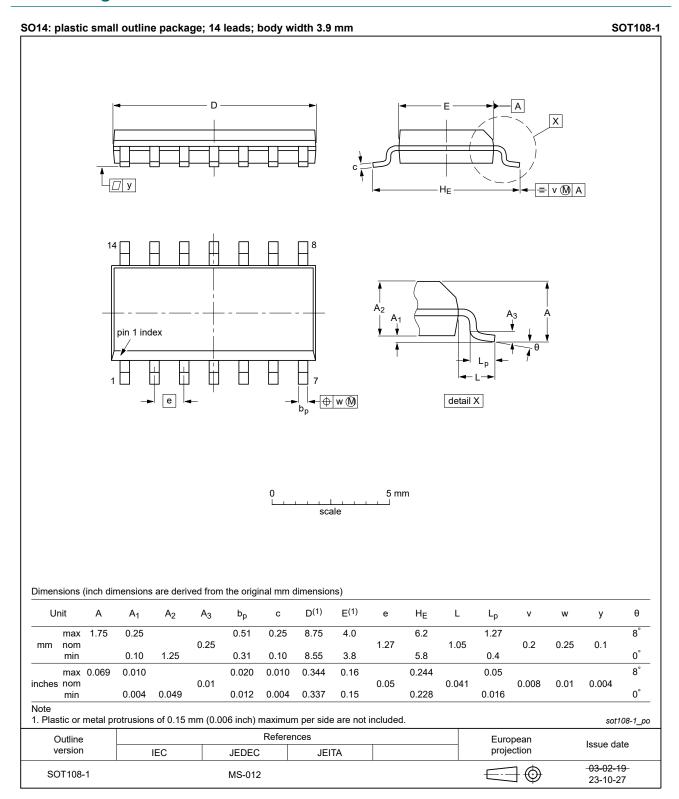


Fig. 5. Package outline SOT108-1 (SO14)

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12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
НВМ	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
HEF4071B v.10	20240905	Product data sheet	-	HEF4071B v.9.1	
Modifications:	 <u>Section 2</u>: ESD specification updated according to the latest JEDEC standard. <u>Fig. 5</u>: Aligned SO package outline drawing to JEDEC MS-012 				
HEF4071B v.9.1	20231019	Product data sheet	-	HEF4071B v.8	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Table 4: Derating values for P_{tot} total power dissipation updated. Section 1 and Section 2 updated. 				
HEF4071B v.8	20151216	Product data sheet	-	HEF4071B v.7	
Modifications:	Type number HEF4071BP (SOT27-1) removed.				
HEF4071B v.7	20111115	Product data sheet	-	HEF4071B v.6	
Modifications:	 Section Applications removed. Table 6: I_{OH} minimum values changed to maximum. 				
HEF4071B v.6	20091201	Product data sheet	-	HEF4071B v.5	
HEF4071B v.5	20090728	Product data sheet	-	HEF4071B v.4	
HEF4071B v.4	20081128	Product data sheet	-	HEF4071B_CNV v.3	
HEF4071B_CNV v.3	19950101	Product specification	-	HEF4071B_CNV v.2	
HEF4071B_CNV v.2	19950101	Product specification	-	-	

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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