256K X 16 MULTIPORT VIDEO RAM

Features

- 256K x 16 Multiport Video RAM
- Performance:

Parameter		-6H	-60	-70
t_{RP}	$\overline{RE}$ Precharge	25ns	25ns	30ns
t_{SCA}	Serial Access Time	12ns	15ns	17ns
t_{CAC}	Access Time from $\overline{CE}$	15ns	15ns	17ns
t_{AA}	Column Address Access Time	25ns	30ns	35ns
t_{SCC}	Serial Clock Cycle Time	12ns	18ns	20ns
t_{RC}	Read or Write Cycle Time	95ns	95ns	110ns
t_{PC}	Fast Page Mode Cycle Time	30ns	30ns	40ns
t_{HPC}	Extended Data Out Cycle Time	20ns	25ns	30ns

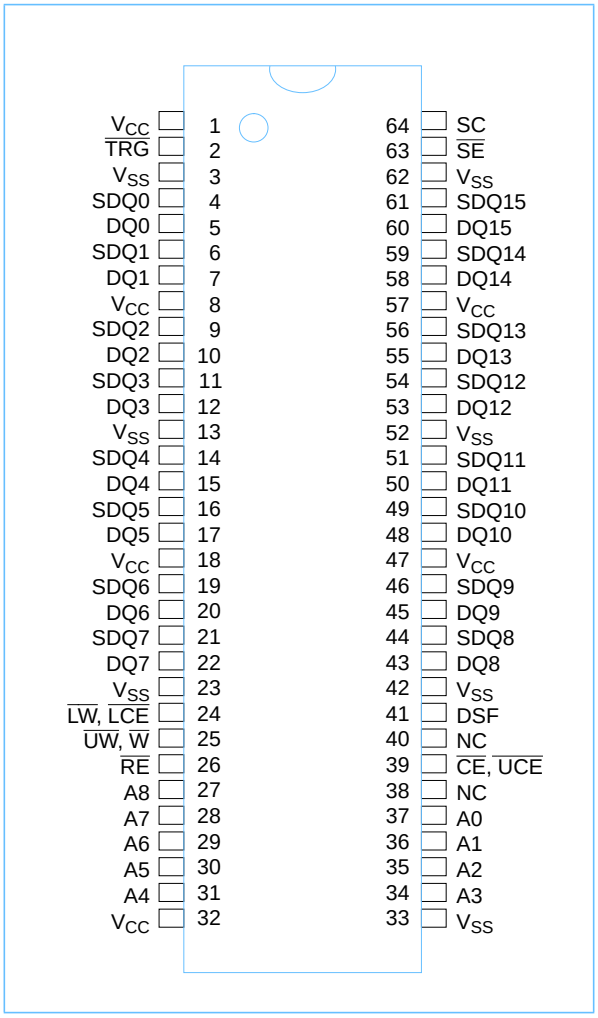
- Fully Asynchronous operation of Random port and Serial port
- Compatible to Full Depth SAM in SRS mode
- 8 Column Block Write with masking Column and WPB masking along with individual Byte Control
- 50 MHz EDO performance
- FLASH WRITE with WPBM- 512 x 16 bits
- Persistent & Non-Persistent WPBM mode
- Split Serial Register with Width Control
- 256 Location Start Address Pointer for SAM
- Full Read and Split Read Transfer
- Masked Write Transfer
- Masked Split Write Transfer
- Power Supply: 5.0V ± 0.5V and 3.3V ± 0.3V
- High Performance, CMOS 0.55µm process
- SSOG-64 JEDEC Standard
- TTL compatible

Description

This 4Mb dual port Video RAM (VRAM) consists of a Dynamic Random Access Memory (DRAM) organized as 256K x 16 interfaced to a Serial Register / Serial Access Memory (SAM) organized as 256 x 16. The VRAM supports three basic operations: Bidirectional Random Access to the DRAM, Bidirectional Serial Access to the SAM, and Bidirectional Data Transfer between any DRAM row and the SAM. Full compatibility is provided between Half Depth SAM (256 x 16) and Full Depth SAM (512 x 16) by setting the VRAM in Serial Register Stop (SRS) mode with a stop address of 128 bit (or less).

Unique features have been added to these basic VRAM operations to improve graphics performance of the system. Higher update rates can be achieved with either Flash Write or Block Write modes. Two $\overline{W}$ or two $\overline{CE}$ inputs are provided for individual byte control for both normal Write and Block Write. For individual bit control, a Write-Per-Bit Mask (WPBM) can be supplied on the data pins at $\overline{RE}$ time to be used during Masked Write transfers or Masked Write cycles. A permanent mask to be used during Block Write cycles can be loaded using the Load Mask Register (LMR) cycle.

Pin Assignments



Pin Description

$\overline{RE}$	Row Enable
$\overline{CE}$	Column Enable (only in dual $\overline{WE}$ parts)
$\overline{LCE}$, $\overline{UCE}$	Lower & Upper Column Enable (Only In Dual $\overline{CE}$ Parts)
$\overline{W}$	Write (Only In Dual $\overline{CE}$ parts)
$\overline{LW}$, $\overline{UW}$	Lower & Upper Byte Write (Only In Dual $\overline{W}$ Parts)
$\overline{TRG}$	Data Transfer & Output Enable
DSF	Designated Special Function
A_8-A_0	Address Inputs
DQ_{15} - DQ_0	Random Port Data Input/Output
SDQ_{15} - SDQ_0	Serial Port Data Input/Output
SC	Serial Clock
$\overline{SE}$	Serial Enable
V_{CC}	Voltage (5.0V ± 0.5V or 3.3V ± 0.3V). All voltages are referenced to the nearest V_{SS} pin.
V_{SS}	Ground. V_{SS}=0V
NC	No Connect

Detailed Pin Description

$\overline{RE}$ - Row Enable; also known as $\overline{RAS}$

This pin is functionally equivalent to a chip enable signal in that whenever it is activated, 8192 storage cells of the selected row are sensed simultaneously and the sense amplifiers restore all data. The falling edge of $\overline{RE}$ latches data on address pins A_0 -A_8. $\overline{CE}$, $\overline{TRG}$, $\overline{W}$, and DSF are simultaneously latched to invoke the DRAM port and Serial port operations.

$\overline{CE}$ - Column Enable (Dual $\overline{WE}$ parts only); also known as $\overline{CAS}$.

This pin serves as a chip select signal. It activates the column decoder and the I/O buffer. The falling edge of $\overline{CE}$ latches the column address A_0 -A_8. State of DSF at falling edge of $\overline{CE}$ invokes various DRAM port and Serial port functions.

$\overline{LCE}$, $\overline{UCE}$ - Lower and Upper Column Enable (Dual $\overline{CE}$ parts only).

These pins enable lower and upper byte respectively of the selected column for Read/Write. The falling edge of either $\overline{LCE}$ or $\overline{UCE}$ latches the column address and state of DSF to invoke various DRAM port and Serial port functions.

$\overline{W}$ - Write (Dual $\overline{CE}$ parts only)

This pin enables the DRAM port write circuitry. It is also used as a control input pin to define the various operations at $\overline{RE}$ fall time.

$\overline{LW}$, $\overline{UW}$ - Lower and Upper Write (Only in Dual $\overline{W}$ parts)

These pins enable the DRAM port write circuitry for Lower and Upper Byte Write respectively. Either $\overline{LW}$ or $\overline{UW}$ being low is considered low for Write cycles.

$\overline{TRG}$ - Data Transfer and Output Enable ($\overline{DT}$/$\overline{OE}$)

This is a multifunctional input pin. In conjunction with $\overline{LW}$/$\overline{UW}$, DSF and $\overline{CE}$, it either enables the DRAM data outputs or enables transfer operations between DRAM and SAM. This is also used as a control input pin to define the various operating modes at $\overline{RE}$ time.

DSF - Designated Special Function

A control pin used in conjunction with other control pins to define the various operating modes at $\overline{RE}$ and $\overline{CE}$ time.

A_0 - A_8 - Address Inputs

These pins are multiplexed as row and column address inputs. Row addresses are first used to select one of the possible 512 rows for a Read, Write, Data Transfer, or Refresh cycles. Column addresses are then supplied to select one of the possible 512 columns for a Read or a Write cycle or one of the possible 256 starting locations for the next Serial Read/Write cycle for the Serial port.

DQ_0 - DQ_{15} - Random Port Data Input/Output

In a Read cycle, these pins serve as outputs for the selected storage cells. In a Write cycle, data input on these pins is latched by the falling edge of $\overline{CE}$ or $\overline{LW}/\overline{UW}$ whichever occurs later. Data will not appear at the outputs until after both $\overline{CE}$ and $\overline{TRG}$ have been brought low. During transfer operations, the DQ outputs remain in the high-Z state for the entire cycle. In a Block Write cycle, data input on these pins is used to mask the selected columns in the block. At $\overline{RE}$ falling edge, the data input at these pins can be used for loading the Write-per-Bit Mask (WPBM).

SDQ_0 - SDQ_{15} - Serial Port Data Input/Output

16 bit data can be written or read from these pins. The output data remains valid until the next SC clock is activated.

SC - Serial Clock

The rising edge of the SC signal is used to initiate a Read/Write from/to the SAM Register (starting from the location specified in the data transfer cycle). In the Serial Read mode, 16 of the 4096 data bits from the SAM Register are transferred to 16 Serial Data Buses and read out. In the Serial Write operation, input data is latched on the rising edge of SC clock. Whenever SC clock is low, the Serial port is in standby.

$\overline{SE}$ - Serial Port Enable

This signal enables or disables the Serial Input/Output buffer. When $\overline{SE}$ is high, the output of the Serial port is in tri-state. ***While $\overline{SE}$ is held high, the serial clock is not disabled. Thus, external SC pulses will increment the internal Serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of Serial output from $\overline{SE}$ low since the Serial Clock input buffer and the Serial address counter are not disabled by $\overline{SE}$.***

V_{cc} - (5.0V $\pm$ 0.5V) or (3.3V $\pm$ 0.3V) voltage.

All voltages are referenced to the nearest V_{SS} pin.

V_{ss} - Circuit ground. V_{ss} = 0V.

NC - No Connect.

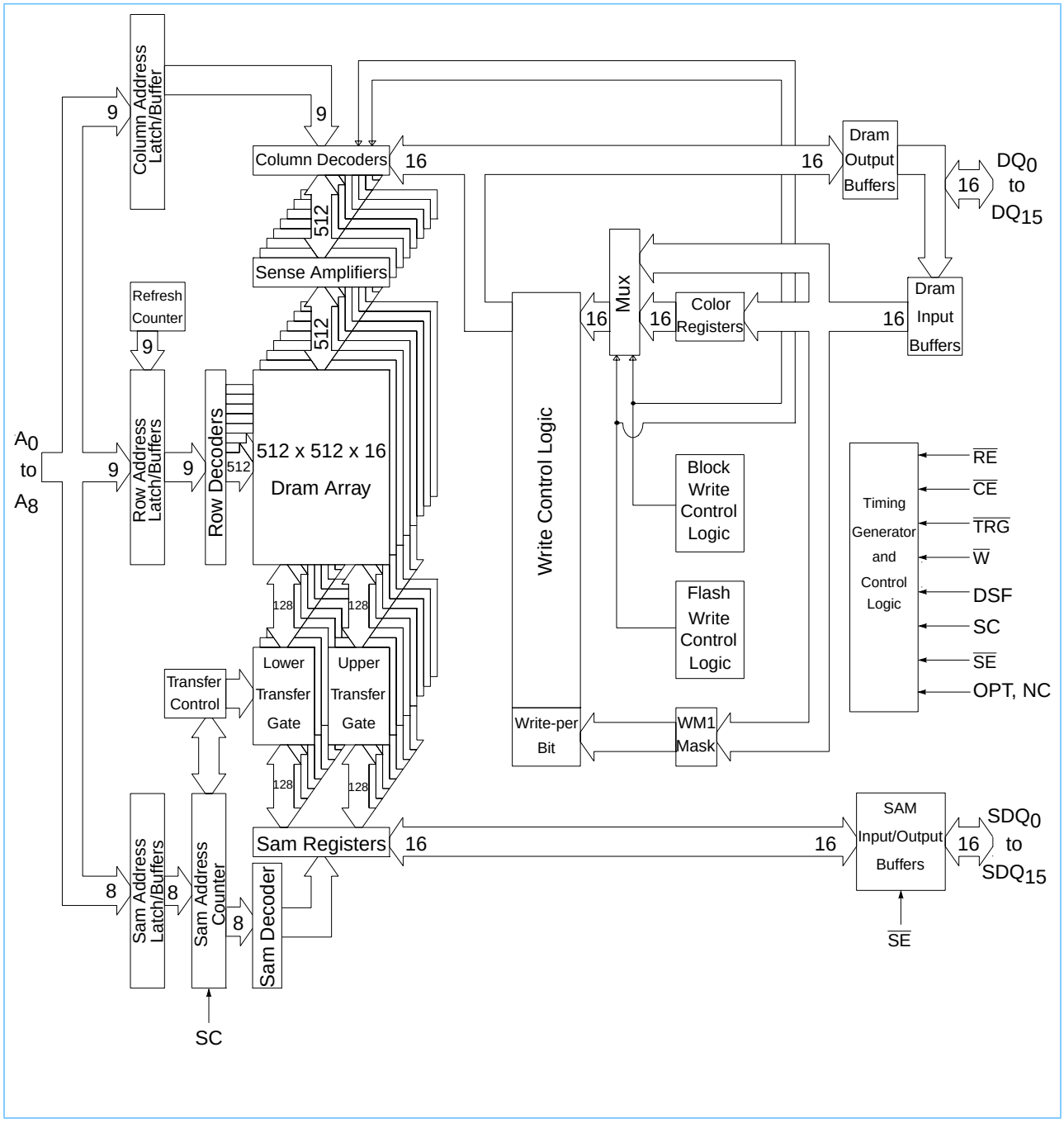
NC implies that the pin(s) should not be grounded or connected to any other signal. These pins might be used for testing some modes at factory. Consult factory before using any one of NC pins.

Ordering Information

Part Number	Features	Voltage	Speed	Package	Notes
IBM025160LG5D-60	Dual $\overline{CE}$, Fast Page	5.0V	60ns	.472" SSOG	
IBM025160LG5D-70			70ns		
IBM025170LG5D-60	Dual $\overline{W}$, Fast Page		60ns		
IBM025170LG5D-70			70ns		
IBM025161LG5D-6H	Dual $\overline{CE}$, Extended Data		<60ns		1
IBM025161LG5D-60			60ns		
IBM025161LG5D-70			70ns		
IBM025171LG5D-6H	Dual $\overline{W}$, Extended Data		<60ns		1
IBM025171LG5D-60			60ns		
IBM025171LG5D-70			70ns		
IBM025160NG5D-60	Dual $\overline{CE}$, Fast Page	3.3V	60ns		
IBM025160NG5D-70			70ns		
BM025170NG5D-60	Dual $\overline{W}$, Fast Page		60ns		
IBM025170NG5D-70			70ns		
IBM025161NG5D-6H	Dual $\overline{CE}$, Extended Data		<60ns		1
IBM025161NG5D-60			60ns		
IBM025161NG5D-70			70ns		
IBM025171NG5D-6H	Dual $\overline{W}$, Extended Data		<60ns		1
IBM025171NG5D-60			60ns		
IBM025171NG5D-70			70ns		

1. The -6H means 60ns High Performance Parts.

Block Diagram



Truth Table

MNE Code	$\overline{RE}$				$\overline{CE}$	Address		DQ_0 - DQ_{15}		Function
	$\overline{CE}$	$\overline{TRG}$	$\overline{W}$	DSF	DSF	$\overline{RE}$	$\overline{CE}$	$\overline{RE}$	$\overline{CE}$, $\overline{W}$	
CBR	0(5)	X	1(4)	0	-	X	-	X	-	$\overline{CE}$ before $\overline{RE}$ Refresh (RESET) (9)
CBRS	0(5)	X	0(3)	1	-	STOP(6) Point	-	X	-	$\overline{CE}$ Before $\overline{RE}$ Refresh stop point set (2)
CBRN	0(5)	X	1(4)	1	-	X	-	X	-	$\overline{CE}$ Before $\overline{RE}$ Refresh without mode reset (10)
ROR	1	1	X	0	-	Row(1)	-	X	-	$\overline{RE}$ Only Refresh (11)
	1	1	1	X	-	Row(1)	-	X	-	
LCR	1	1	1(4)	1	1	Row(1)	X	X	Color	Load Color Register
LMR	1	1	1(4)	1	0	Row(1)	X	X	Mask	Load Mask Register (13)
RW	1	1	1(4)	0	0	Row	Column	X	Valid Data Input	Read/Write Cycle (No Mask)
RWM	1	1	0(3)	0	0	Row	Column	WPBM (7)	Valid Data Input	Read/Write Cycle (Masked)
BW	1	1	1(4)	0	1	Row	Column A_3-A_8	X	Column mask	Block Write Cycle (No Mask)
BWM	1	1	0(3)	0	1	Row	Column A_3-A_8	WPBM (7)	Column mask	Block Write Cycle (Masked)
FWM	1	1	0(3)	1	X	Row	X	WPBM (7)	X	Flash Write Cycle (Masked) (8)
RT	1	0	1(4)	0	X	Row	TAP	X	X	Full - Register Read Transfer
MWT	1	0	0(3)	0	X	Row	TAP (12)	WPBM (7)	X	Masked Full - Register Write Transfer
SRT	1	0	1(4)	1	X	Row	TAP	X	X	Split Read Transfer
MSWT	1	0	0(3)	1	X	Row	TAP	WPBM (7)	X	Masked Split Write Transfer

1. Row address needed only for refresh operation to the selected row. Otherwise this is a don't care.
2. This cycle is used to put the chip into special modes. The Address at $\overline{RE}$ fall becomes the Serial port STOP address. CBRS cycle(s) should be performed immediately after the power up initialization cycles.
3. Either $\overline{W}$ is 0.
4. Both $\overline{W}$ are 1.
5. Either $\overline{CE}$ is 0 on Dual $\overline{CE}$ parts.
6. STOP defines the Serial port address on which shift out moves to the other half of the SAM.
7. After LMR, WPBM is only changed by LMR. CBR resets the persistent mask.
8. No byte select, both bytes are written.
9. CBR mode will reset all the unknown modes at power up. It will also clear persistent Write-per-Bit mode.
10. CBRN mode will not clear persistent Write-per-Bit mode.
11. ROR will not clear inadvertent modes at power up time.
12. A_0-A_7 define the tap point for the Serial Data input after the transfer. A_8 defines the particular half of the DRAM row in which the SAM data will be transferred.
13. LMR cycle will set the persistent Write-per-Bit mode. The persistent Write-per-Bit mode is reset by CBR cycle only.
14. DQ_0 - DQ_{15} are latched on either the first $\overline{WEX}$ falling edge or the falling edge of $\overline{CAS}$, whichever occurs later.

Legend: 'X' = Don't Care; '-' = Not Applicable

Absolute Maximum Ratings

Symbol	Item	Rating		Units	Notes
		5.0 Volt	3.3 Volt		
V_{CC}	Power Supply Voltage	-1.0 to +6.0	-0.5 to +4.6	V	1
T_A	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.3	1.3	W	1
I_{OUT}	Short Circuit Output Current	50	33	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A= 0 to +70°C)

Symbol	Parameter	5.0 Volt			3.3 Volt			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}+0.5	2.0	—	V_{CC}+0.3	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A= 25°C, f= 1.0 MHz)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (Addresses)	—	5	pF	
C_{I2}	$\overline{RE}$, $\overline{CE}$, $\overline{W}$, $\overline{TRG}$, DSF, SC, $\overline{SE}$	—	7	pF	
C_O	Output Capacitance (DQ_i, SDQ_i)	—	7	pF	

Output Drivers

Driver	Impedance	Output Voltage, Low (Max)	Output Voltage, High (Min)
Serial Port	60±15 Ω	I_{OUT}=2.0 mA, V=0.4	I_{OUT}=-1 mA, V=2.4
Parallel Port	45±15 Ω	I_{OUT}=2.0 mA, V=0.4	I_{OUT}=-1 mA, V=2.4

AC Measurement Conditions

Port	Detect	Load
Parallel Port Output Detect Level	2.0V / 0.8V	—
Serial Port Output Detect Level	2.0V / 0.8V	—
Parallel Port Output Load	—	1 TTL + 50 PF
Serial Port Output Load	—	1 TTL + 30 PF

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter		5.0 Volt		3.3 Volt		Units	Notes
			Min.	Max.	Min.	Max.		
I_{CC1}	Operating Current (Random) Average Power Supply Operating Current ($\overline{RE}$ and $\overline{CE}$ Cycling, t_{RC} =120ns for -60 and -6H, t_{RC} =130ns for -70, SC = 0)	-6H	—	135	—	135	mA	1, 2, 3, 6
		-60	—	135	—	135		
		-70	—	130	—	130		
I_{CC2}	Operating Current (Serial) Average Power Supply Current (t_{SCC} = 20ns for -60 and -6H, t_{SCC} = 23ns for -70)	-6H	—	40	—	40	mA	1, 2, 7
		-60	—	40	—	40		
		-70	—	35	—	35		
I_{CC3}	Operating Current (Both Port) Average Power Supply Current ($\overline{RE}$ and $\overline{CE}$ Cycling, t_{RC} =120ns & t_{SCC} = 20ns for -60 and -6H, t_{RC} =130ns & t_{SCC} = 23ns for -70)	-6H	—	160	—	160	mA	1, 2, 3, 6, 7
		-60	—	160	—	16 0		
		-70	—	150	—	150		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RE}$ V_{IL} Min., $\overline{CE}$ Cycling, t_{PC} = 40ns for -60 and -6H, t_{PC}=45ns for -70)	-6H	—	80	—	80	mA	1, 2, 4, 6, 7
		-60	—	80	—	80		
		-70	—	70	—	70		
I_{CC5}	Fast Page Mode Current (Serial) Average Power Supply Current, Fast Page/Serial ($\overline{RE} \le V_{IL}$ Min., $\overline{CE}$ Cycling, t_{PC} = 40ns & t_{SCC} = 20ns for -60 and -6H, t_{PC} = 45ns & t_{SCC} = 23ns for -70)	-6H	—	85	—	85	mA	1, 2, 7
		-60	—	85	—	85		
		-70	—	75	—	75		
I_{CC6}	Standby Supply Current Power Supply Standby Current ($\overline{RE}$ = $\overline{CE}$ = V_{CC}, SC = 0V)		—	5	—	5	mA	
I_{CC7}	Data Transfer Current Average Power Supply Current (t_{RC} =120ns for -60 and -6H, t_{RC} = 130ns for -70, SC = 0V)	-6H	—	130	—	130	mA	
		-60	—	130	—	130		
		-70	—	120	—	120		
I_{CC8}	Data Transfer Current Average Power Supply Current (t_{SCC} = 20ns for -60 and -6H, t_{SCC} = 23ns for -70)	-6H	—	140	—	140	mA	
		-60	—	140	—	140		
		-70	—	130	—	130		
$I_{I(L)}$	Input Leakage Current, any input ($0.0 \le V_{IN} \le (V_{CC} + 1.0V)$), All Other Pins Not Under Test = 0V		-10	+10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, $0.0 \le V_{OUT} \le V_{CC}$(max))		-10	+10	-10	10	µA	
V_{OH}	Output Level (TTL) Output “H” Level Voltage (I_{OUT} = -1mA, Random and Serial)		2.4	—	2.4	—	V	4
V_{OL}	Output Level (TTL) Output “L” Level Voltage (I_{OUT} = +2.0mA, Random and Serial)		—	0.4	—	0.4	V	4

1. I_{CC1}, I_{CC2}, I_{CC3}, I_{CC4}, I_{CC5}, I_{CC7} and I_{CC8} depend on cycle rate.
2. I_{CC1}, I_{CC2}, I_{CC3}, I_{CC4}, I_{CC5}, I_{CC7} and I_{CC8} depend on output loading. Specified values are obtained with the output open.
3. Measured with one address change per $\overline{RE}$ cycle.
4. Measured with one column address change per page cycle.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Measured with $\overline{TRG}$ = V_{IH} when $\overline{CE}$ = V_{IL}.
7. Measured with $\overline{SE}$ = V_{IH}.

AC Characteristics (T_A= 0 to +70°C)

Read, Write, Read-Modify-Write and Refresh. Cycles (Part 1 of 2) (Common Parameters)

Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{ASC}	Column address setup time	0	—	0	—	0	—	ns	
t_{ASR}	Row address setup time	0	—	0	—	0	—	ns	
t_{AR}	Column address hold time after $\overline{RE}$ low	15	—	20	—	25	—	ns	
t_{CAH}	Column address hold time after $\overline{CE}$ low	6	—	6	—	8	—	ns	5
t_{CAS}	$\overline{CE}$ pulse width	12	16K	15	16K	17	16K	ns	
t_{CHCL}	First $\overline{CE}$ to return high to last $\overline{CE}$ going low	6	—	6	—	8	—	ns	
t_{CLCH}	Last $\overline{CE}$ going low to first $\overline{CE}$ to return high	6	—	6	—	8	—	ns	
t_{CP}	$\overline{CE}$ precharge time	6	—	6	—	8	—	ns	
t_{CRP}	$\overline{CE}$ high before $\overline{RE}$ low precharge	5	—	5	—	10	—	ns	8
t_{CSH}	$\overline{CE}$ hold time	60	—	60	—	70	—	ns	
$t_{H(SFC)}$	DSF hold time after $\overline{CE}$ low	6	—	6	—	8	—	ns	
$t_{H(SFR)}$	DSF hold time after $\overline{RE}$ low	6	—	6	—	8	—	ns	
t_{MH}	Write mask hold time after $\overline{RE}$ low	6	—	6	—	8	—	ns	
t_{MS}	Data-in setup before $\overline{RE}$ low	0	—	0	—	0	—	ns	
t_{RAD}	$\overline{RE}$ to column address delay time	11	35	11	35	13	40	ns	4
t_{RAH}	Row address hold time after $\overline{RE}$ low	6	—	6	—	8	—	ns	
t_{RAS}	$\overline{RE}$ pulse width	60	100K	60	100K	70	100K	ns	
t_{RC},t_{WC}	Random read or write cycle time	95	—	95	—	110	—	ns	1, 2
t_{RCD}	Delay from $\overline{RE}$ low to $\overline{CE}$ low	16	45	16	45	18	53	ns	3, 5, 9
t_{RP}	$\overline{RE}$ precharge time	25	—	25	—	30	—	ns	1, 6, 7
t_{RSH}	$\overline{RE}$ hold time	15	—	15	—	17	—	ns	
t_{RWH}	$\overline{W}$ hold time after $\overline{RE}$ low	6	—	6	—	8	—	ns	
$t_{SU(SFC)}$	DSF setup time before $\overline{CE}$ low	0	—	0	—	0	—	ns	

1. An initial pause of 100µs is required after power up followed by 8 $\overline{CE}$ before $\overline{RE}$ refresh cycles for proper device operation
2. AC measurements assume t_T = 5ns.
3. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
4. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
5. t_{RCD} and t_{CAH} cannot be at minimum values simultaneously. t_{RCD} + t_{CAH} ≥ 45ns (60ns t_{RAC} product), t_{RCD} + t_{CAH} ≥ 50ns (70ns t_{RAC} product).
6. t_{RWL} and t_{RP} cannot be at minimum values simultaneously. t_{RWL} + t_{RP} ≥ 60ns (60ns t_{RAC} product), t_{RWL} + t_{RP} ≥ 70ns (70ns t_{RAC} product).
7. t_{CWL} and t_{RP} cannot be at minimum values simultaneously. t_{CWL} + t_{RP} ≥ 60ns (60ns t_{RAC} product), t_{CWL} + t_{RP} ≥ 70ns (70ns t_{RAC} product).
8. t_{CRP} must be 15ns (60ns t_{RAC}) or 17ns (70ns t_{RAC}) if a write-per-bit mask is used on the following $\overline{RE}$ cycle due to the fact that t_{OFF} must be met.
9. During Serial port write transfer t_{RCD} (max) = 100ns.

Read, Write, Read-Modify-Write and Refresh. Cycles (Part 2 of 2) (Common Parameters)

Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{SU(SFR)}$	DSF setup time before $\overline{RE}$ low	0	—	0	—	0	—	ns	
t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	
t_{TLH}	$\overline{TRG}$ hold time after $\overline{RE}$ low	6	—	6	—	8	—	ns	
t_{TLS}	$\overline{TRG}$ setup time before $\overline{RE}$ low	0	—	0	—	0	—	ns	
t_{WSR}	Write setup time before $\overline{RE}$ low	0	—	0	—	0	—	ns	
t_{WCR}	Write hold time after $\overline{RE}$ low	20	—	20	—	25	—	ns	

1. An initial pause of 100µs is required after power up followed by 8 $\overline{CE}$ before $\overline{RE}$ refresh cycles for proper device operation
2. AC measurements assume t_T = 5ns.
3. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
4. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
5. t_{RCD} and t_{CAH} cannot be at minimum values simultaneously. $t_{RCD} + t_{CAH} \geq 45$ns (60ns t_{RAC} product), $t_{RCD} + t_{CAH} \geq 50$ns (70ns t_{RAC} product).
6. t_{RWL} and t_{RP} cannot be at minimum values simultaneously. $t_{RWL} + t_{RP} \geq 60$ns (60ns t_{RAC} product), $t_{RWL} + t_{RP} \geq 70$ns (70ns t_{RAC} product).
7. t_{CWL} and t_{RP} cannot be at minimum values simultaneously. $t_{CWL} + t_{RP} \geq 60$ns (60ns t_{RAC} product), $t_{CWL} + t_{RP} \geq 70$ns (70ns t_{RAC} product).
8. t_{CRP} must be 15ns (60ns t_{RAC}) or 17ns (70ns t_{RAC}) if a write-per-bit mask is used on the following $\overline{RE}$ cycle due to the fact that t_{OFF} must be met.
9. During Serial port write transfer t_{RCD} (max) = 100ns.

Write Cycle

Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CWL}	Write Command setup before $\overline{CE}$ high	10	—	15	—	17	—	ns	4
t_{DH}	Data-in hold time after $\overline{CE}$ or $\overline{W}$ low, whichever is later	6	—	8	—	8	—	ns	1
t_{DHR}	Data-in hold time after $\overline{RE}$ low	20	—	20	—	25	—	ns	
t_{DSC}	Data-in setup before $\overline{CE}$ low	0	—	0	—	0	—	ns	
t_{DSW}	Data-in setup before $\overline{W}$ low	0	—	0	—	0	—	ns	
t_{GHD}	$\overline{TRG}$ high before data-in applied on primary port data pins	10	—	15	—	17	—	ns	
t_{RWL}	Write setup time before $\overline{RE}$ high	10	—	15	—	17	—	ns	3
t_{WCH}	Write hold time after $\overline{CE}$ low	6	—	6	—	8	—	ns	
t_{WCS}	Early write command setup before $\overline{CE}$ Low	0	—	0	—	0	—	ns	1, 2
t_{WP}	Write command pulse width	6	—	6	—	8	—	ns	

1. Data-in setup and hold is measured from the later of the two timings - $\overline{CE}$ / $\overline{UCE}$ / $\overline{LCE}$ or $\overline{W}$ / $\overline{UW}$ / $\overline{LW}$.
2. t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive parameters. They are included as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{CPW} \geq t_{CPW}$ (min) (Fast Page) mode, the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
3. t_{RWL} and t_{RP} cannot be at minimum values simultaneously. $t_{RWL} + t_{RP} \geq 60$ns (60ns t_{RAC} product), $t_{RWL} + t_{RP} \geq 70$ns (70ns t_{RAC} product).
4. t_{CWL} and t_{RP} cannot be at minimum values simultaneously. $t_{CWL} + t_{RP} \geq 60$ns (60ns t_{RAC} product), $t_{CWL} + t_{RP} \geq 70$ns (70ns t_{RAC} product).

Read-Modify-Write Cycle

Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AWD}	Column address to $\overline{W}$ low	50	—	50	—	60	—	ns	1
t_{CWD}	$\overline{CE}$ low before $\overline{W}$ low	35	—	35	—	40	—	ns	1
t_{OEH}	Output disable ($\overline{TRG}$ high) hold time from $\overline{W}$ low	15	—	15	—	17	—	ns	
t_{RWC}	Read-modify-write cycle time	135	—	135	—	155	—	ns	
t_{RWD}	$\overline{RE}$ low to $\overline{W}$ low	80	—	80	—	95	—	ns	1

1. t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive parameters. They are included as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{CPW} \geq t_{CPW}$ (min) (Fast Page) mode, the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

Read Cycle

Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AA}	Access time from column address	—	25	—	30	—	35	ns	2, 3
t_{CAC}	Access time from $\overline{CE}$	—	15	—	15	—	17	ns	1, 2, 3
t_{OEA}	Access time from $\overline{TRG}$	—	15	—	15	—	17	ns	
t_{OES}	Output enable setup ($\overline{TRG}$ low) before $\overline{RE}$ high	10	—	10	—	10	—	ns	
t_{OEZ}	Primary output disable from $\overline{TRG}$ high	0	10	0	15	0	17	ns	
t_{OFF}	Primary output disable from $\overline{CE}$	0	10	0	15	0	17	ns	5
t_{RAC}	Access time from $\overline{RE}$	—	60	—	60	—	70	ns	1, 2, 3
t_{RAL}	Column address to $\overline{RE}$ high	25	—	30	—	35	—	ns	
t_{RCH}	Read hold time after $\overline{CE}$ goes high	0	—	0	—	0	—	ns	4
t_{RCS}	Read command setup time	0	—	0	—	0	—	ns	
t_{RRH}	Read command hold time to $\overline{RAS}$ high	0	—	0	—	0	—	ns	4

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current and 50 pF load for the primary port. Output referenced levels: V_{OH} = 2.0V and V_{OL} = 0.8V.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Read-Modify-Write-Cycle

Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWCP}	Fast page mode read-modify-write Cycle Time	74	—	74	—	84	—	ns	

Page Mode Cycle

Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{ACP}	Access time from $\overline{CE}$ precharge	—	28	—	35	—	40	ns	
t_{HPC}	Extended data out cycle time	20	—	25	—	30	—	ns	
t_{PC}	Fast page mode cycle time	30	—	35	—	40	—	ns	

Refresh Cycle

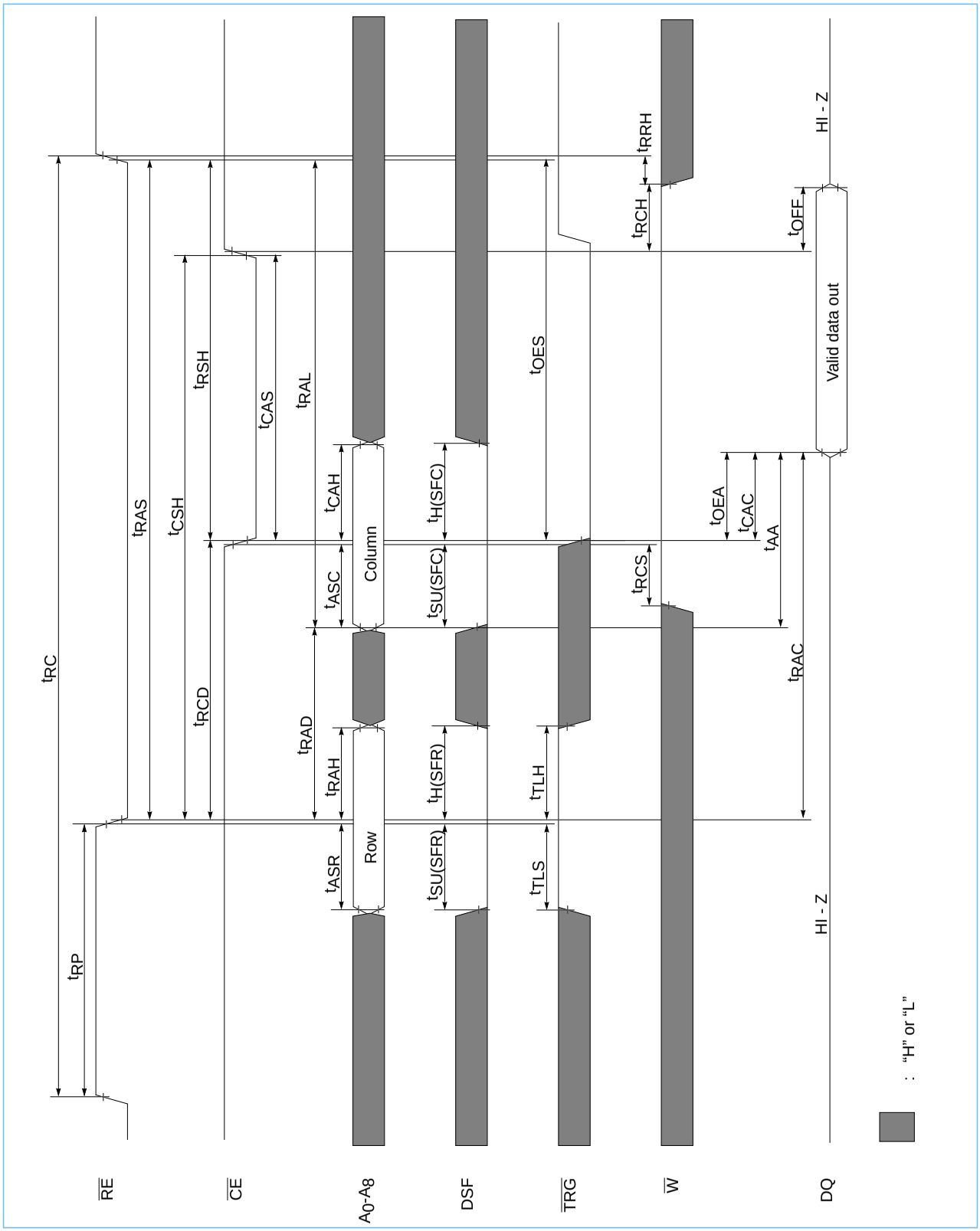
Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CHR}	$\overline{CE}$ held low after $\overline{RE}$ low ($\overline{CE}$ before $\overline{RE}$ refresh)	6	—	6	—	8	—	ns	
t_{CSR}	$\overline{CE}$ low setup before $\overline{RE}$ low ($\overline{CE}$ before $\overline{RE}$ refresh)	5	—	5	—	5	—	ns	
t_{REF}	Refresh period	—	32	—	32	—	32	ms	
t_{RPC}	$\overline{RE}$ high to $\overline{CE}$ low precharge	0	—	0	—	0	—	ns	

Serial Read, Write and Transfer Cycle

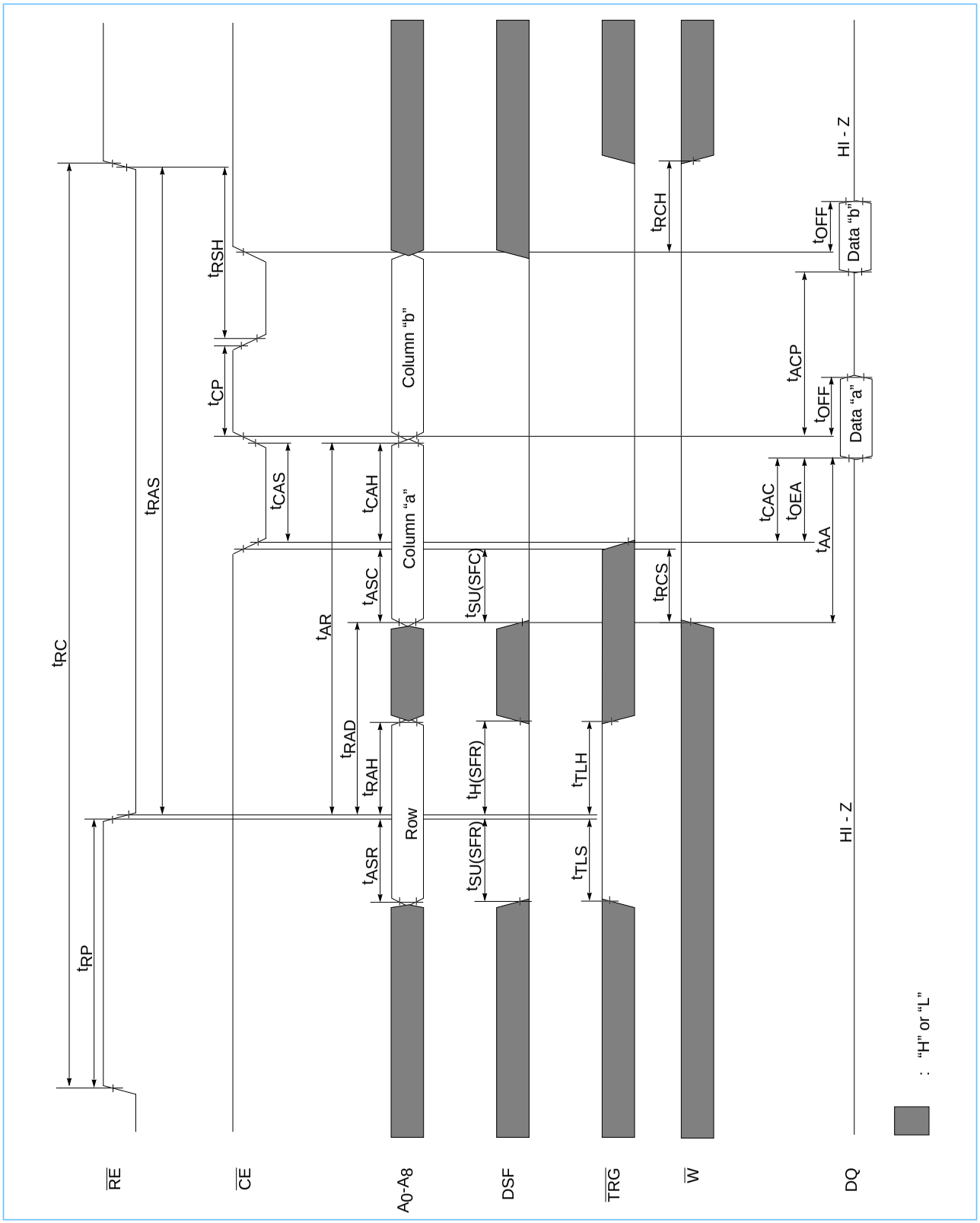
Symbol	Parameter	-6H		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSD}	$\overline{CE}$ low to first SC high after $\overline{TRG}$ goes high	15	—	15	—	17	—	ns	
t_{CTH}	Delay time from $\overline{CE}$ low to $\overline{TRG}$ high	15	—	15	—	15	—	ns	
$t_{d(RHMS)}$	Delay time, $\overline{RE}$ high to last (most significant rising edge of SC before boundary switch during split read transfer Cycles	20	—	20	—	20	—	ns	
t_{DTH}	$\overline{TRG}$ hold after $\overline{RE}$ high	5	—	5	—	5	—	ns	
$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RE}$ low during split read transfer cycles	15	—	15	—	17	—	ns	
t_{ESR}	$\overline{SE}$ setup before $\overline{RE}$ low	0	—	0	—	0	—	ns	
t_{RSD}	$\overline{RE}$ low to first SC high after $\overline{TRG}$ goes high	60	—	60	—	70	—	ns	
t_{RTH}	$\overline{RE}$ low to $\overline{TRG}$ high	45	—	45	—	55	—	ns	
t_{SC}	Width of SC high	4	—	6	—	7	—	ns	
t_{SCA}	Access time from SC going high	3	12	3	15	3	17	ns	1
t_{SCC}	Serial clock cycle time	12	—	18	—	20	—	ns	
t_{SCP}	Width of SC low	4	—	6	—	7	—	ns	
t_{SDH}	Serial data-in hold time after SC high	5	—	5	—	5	—	ns	
t_{SDS}	Serial data-in setup time to SC high	2	—	2	—	2	—	ns	
t_{SEA}	Access time from $\overline{SE}$ going low	—	10	—	12	—	15	ns	
t_{SFD}	Serial enable setup time to SC high	3	—	3	—	3	—	ns	
t_{SEZ}	Serial output disable from $\overline{SE}$ high	0	8	0	8	0	10	ns	
t_{SOH}	Old Serial data out hold time after SC high	3	—	3	—	3	—	ns	
t_{SRS}	SC going high to $\overline{RE}$ low	8	—	8	—	10	—	ns	
t_{SWS}	$\overline{TRG}$ high to SC high (first serial clock after real time transfer)	8	—	8	—	10	—	ns	
t_{TCH}	$\overline{TRG}$ hold time to $\overline{CE}$ high	8	—	8	—	10	—	ns	
t_{TRH}	$\overline{TRG}$ hold to $\overline{RE}$ high	8	—	8	—	10	—	ns	
t_{TRP}	$\overline{RE}$ high to SC high (Serial write transfer)	15	—	15	—	20	—	ns	
t_{TSL}	SC high delay to $\overline{TRG}$ high during a real time read transfer	5	—	5	—	5	—	ns	

1. Measured with the specified current and 30 pF load for the Serial port. Output referenced levels: V_{OH} = 2.0V and V_{OL} = 0.8V.

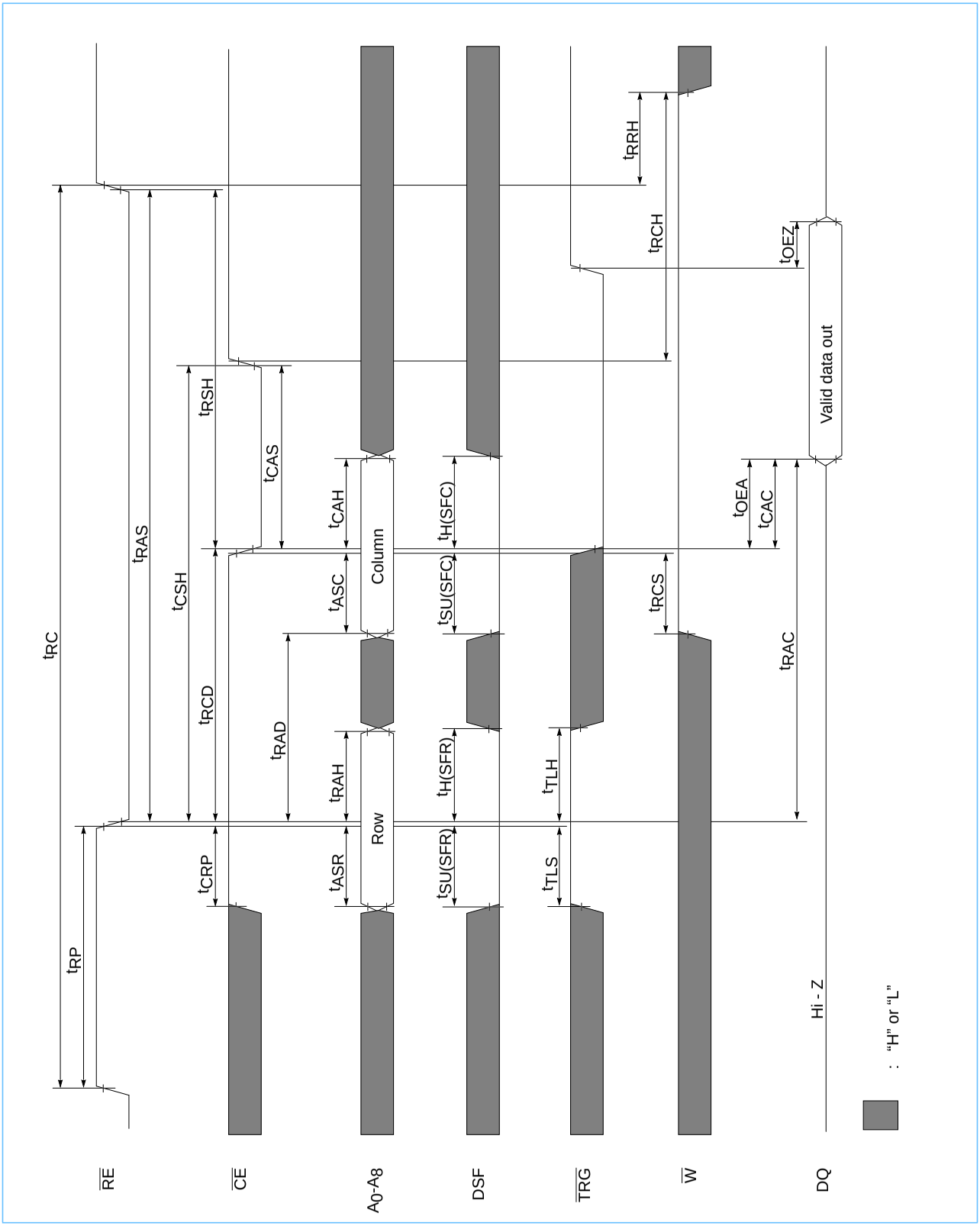
Fast Page (FP) Read Cycle



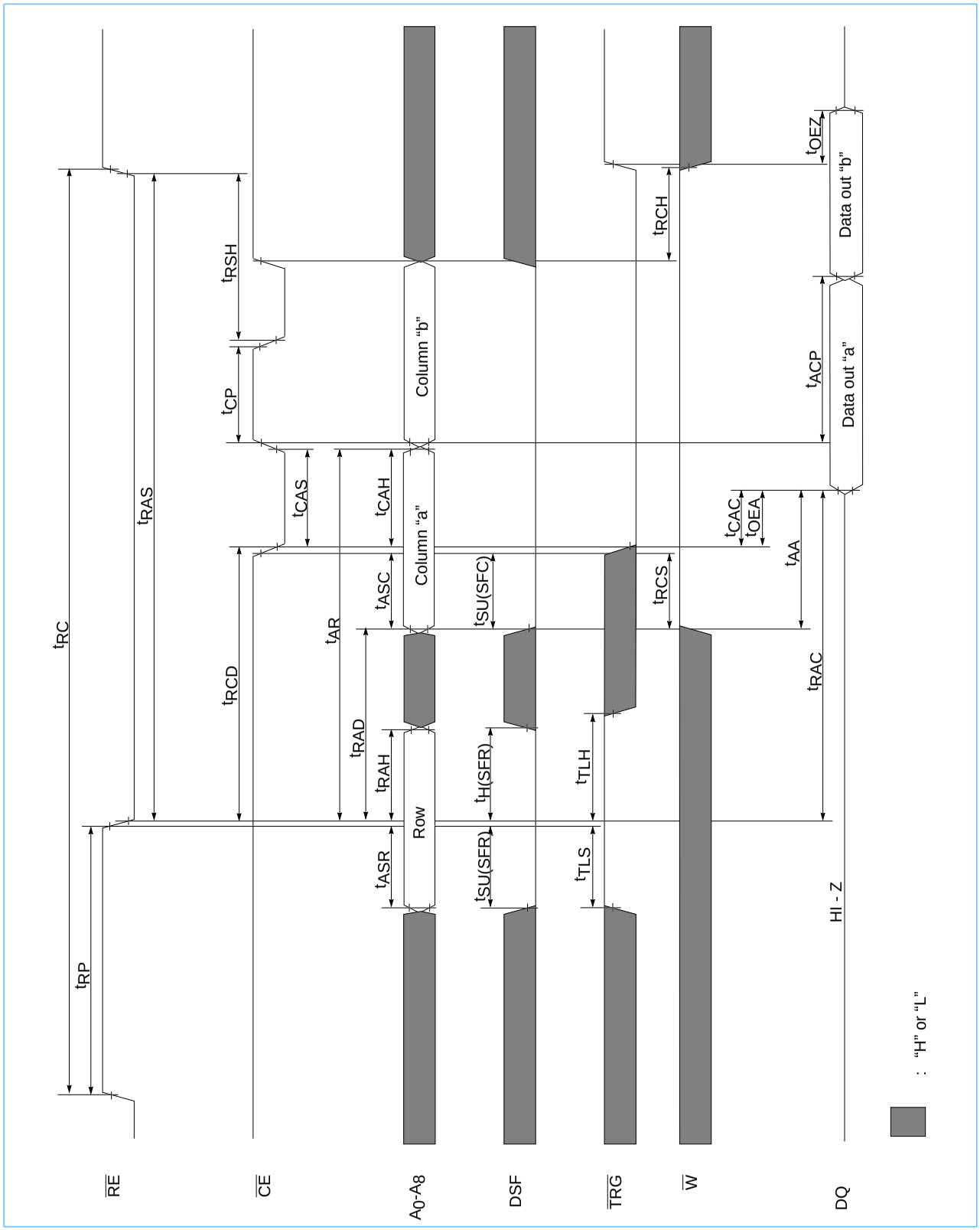
Fast Page Read Operation



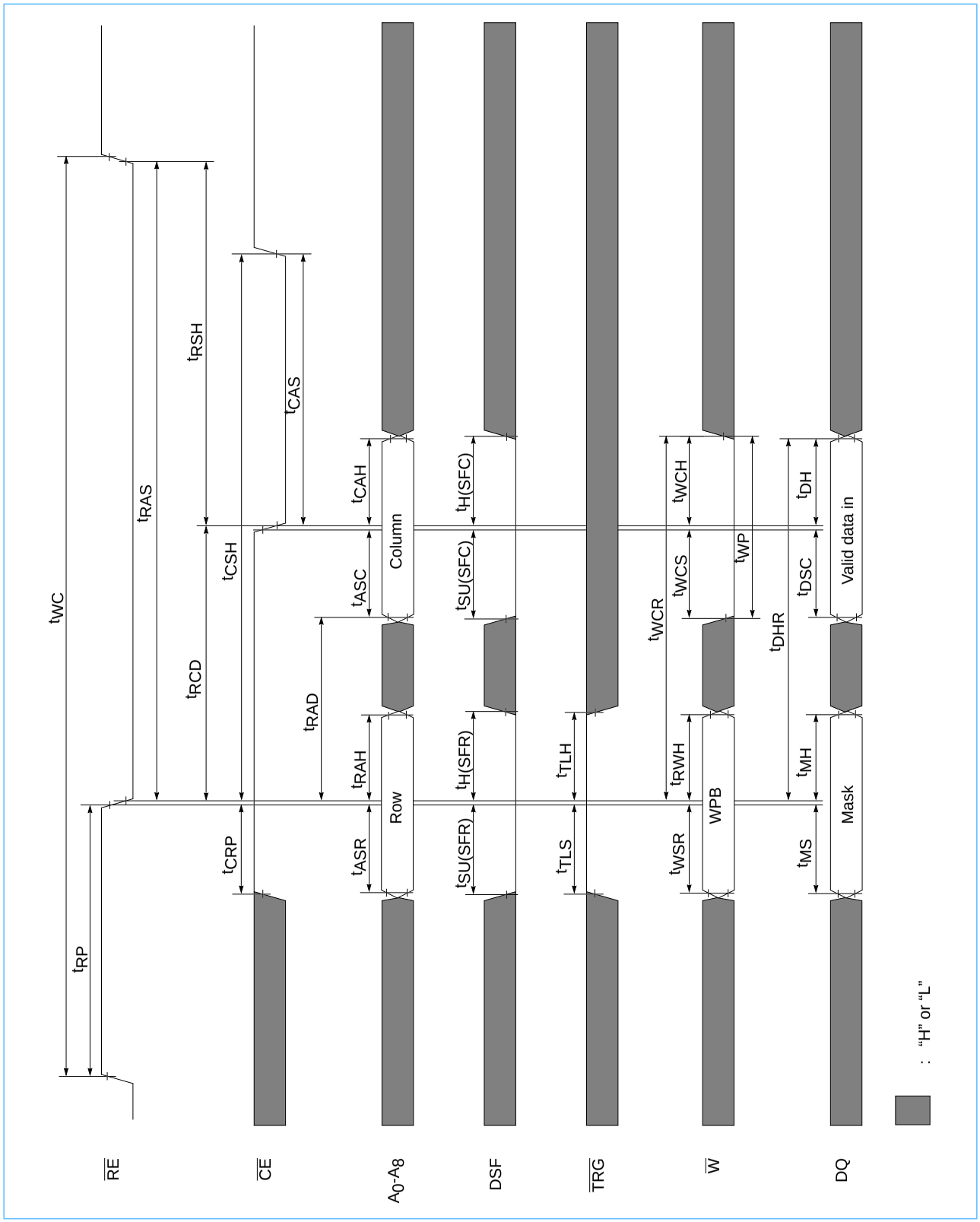
EDO Page Read Cycle



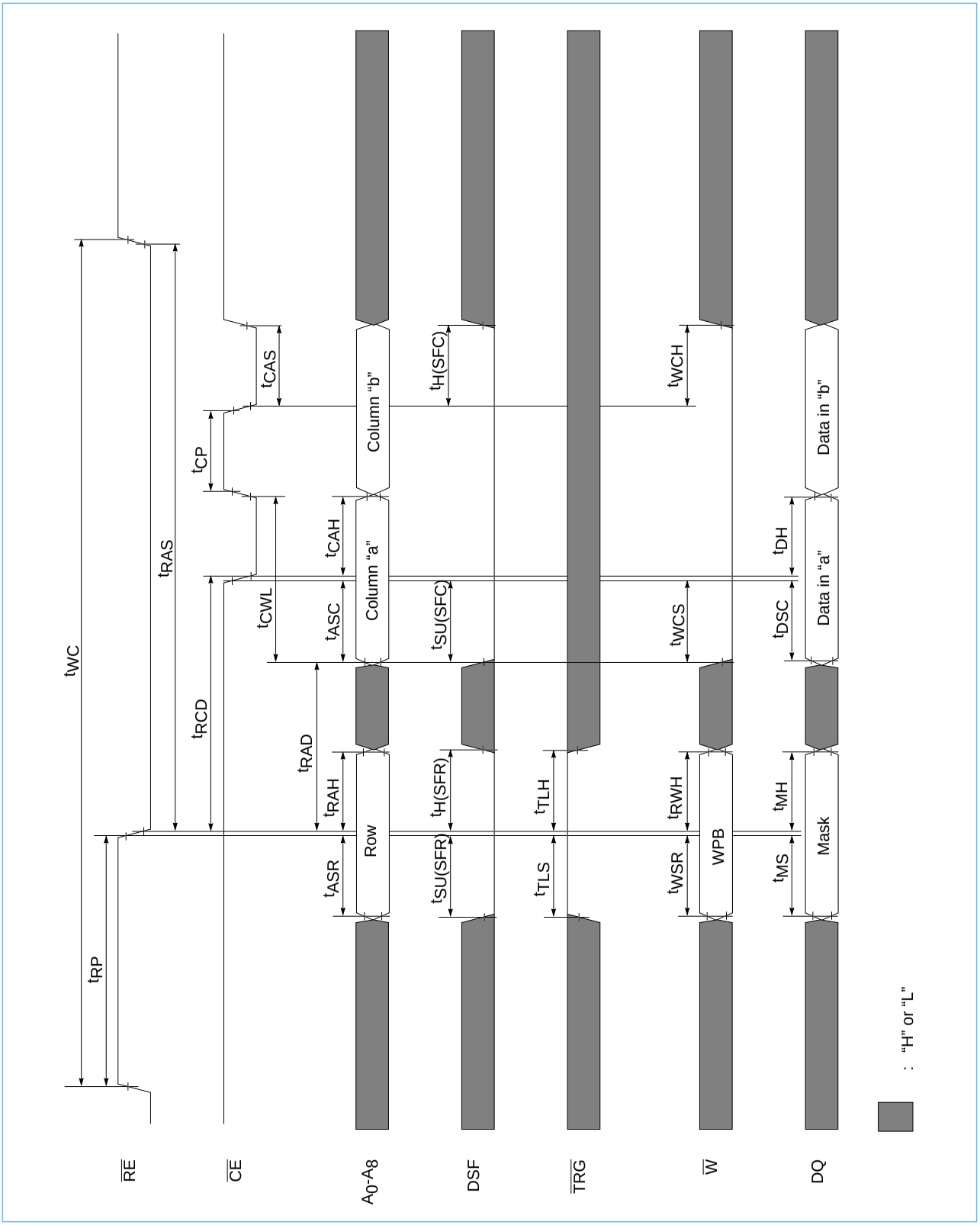
EDO Page Read Operation



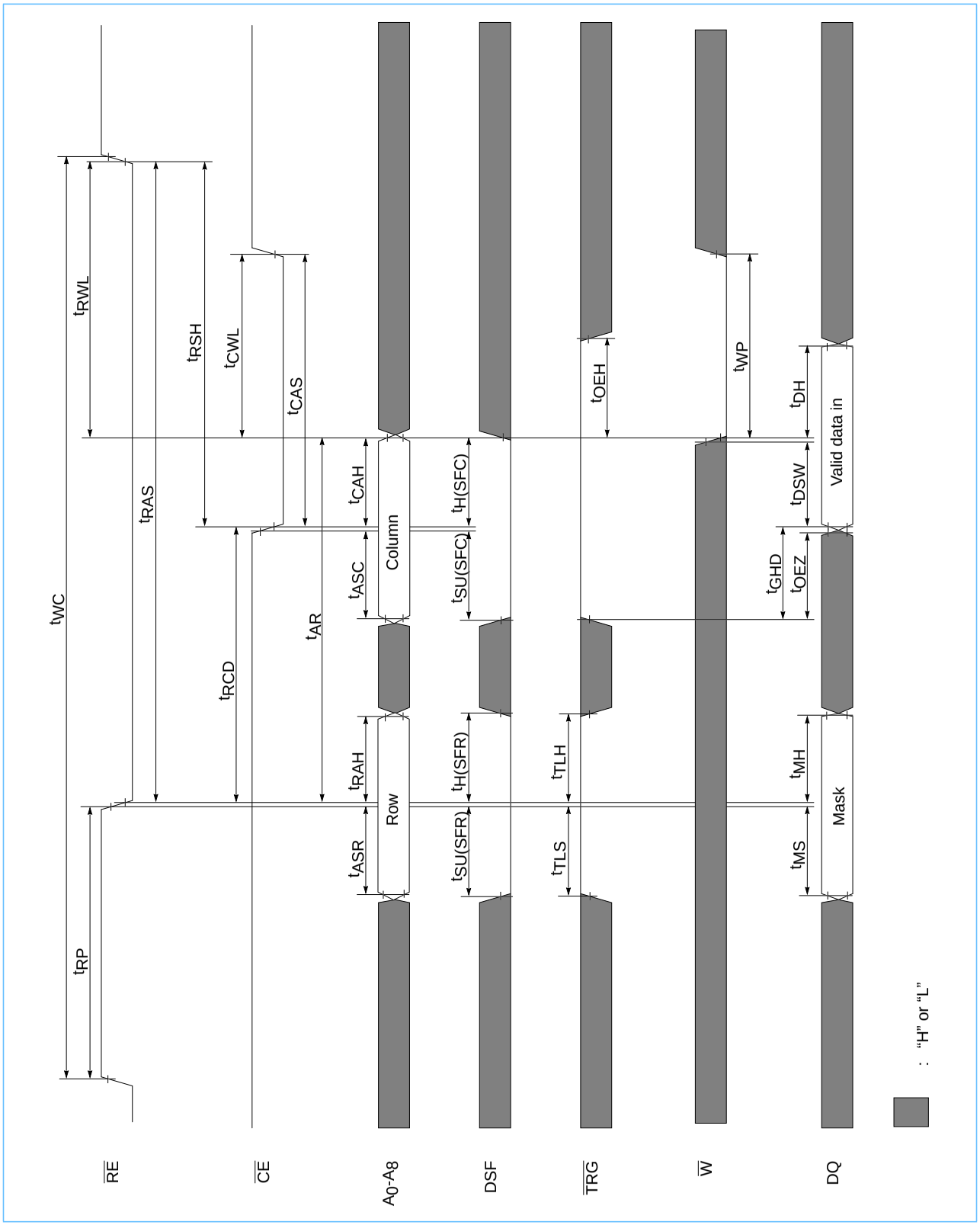
Write Cycle (Early Write)



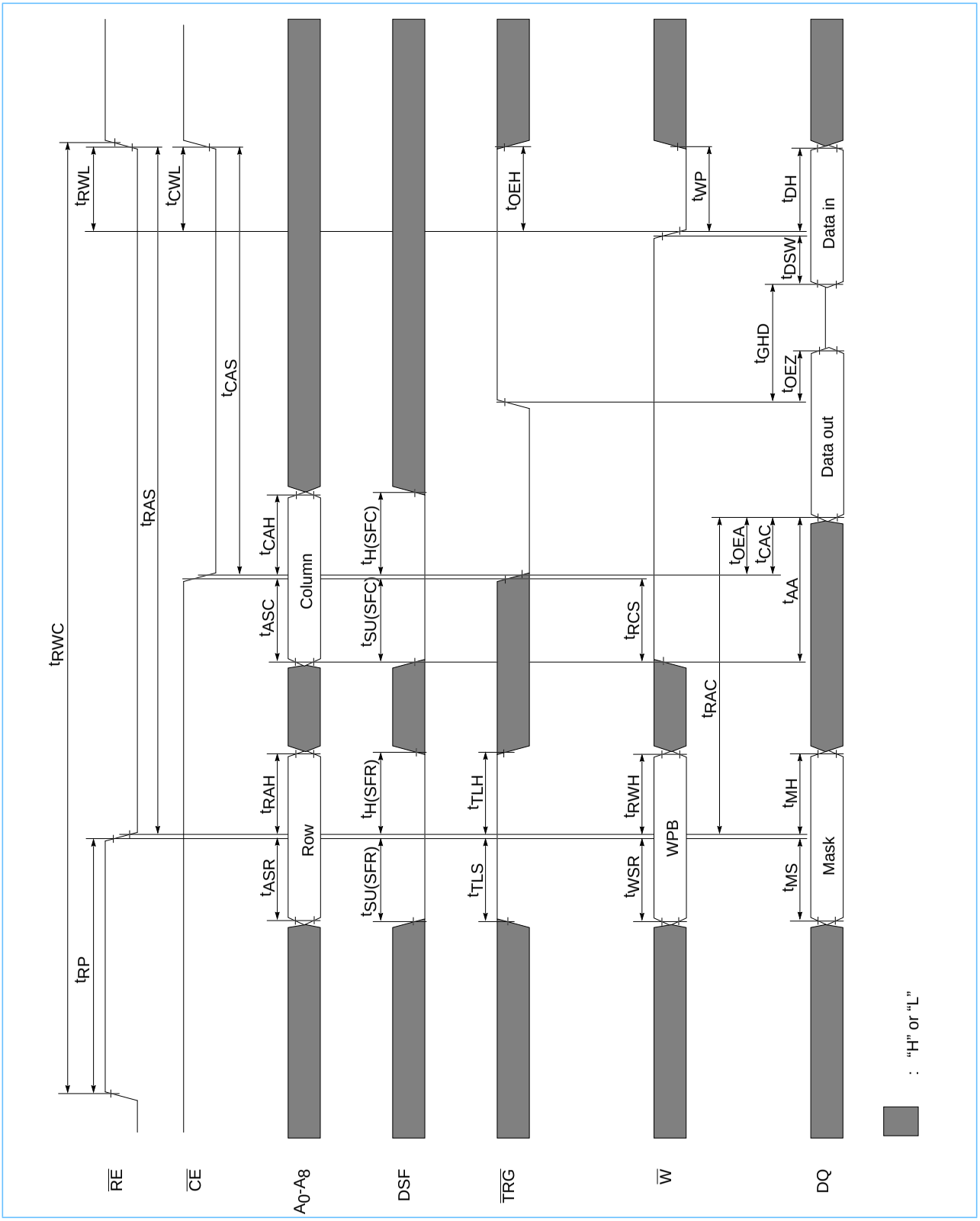
Fast Page Mode (Early Write)



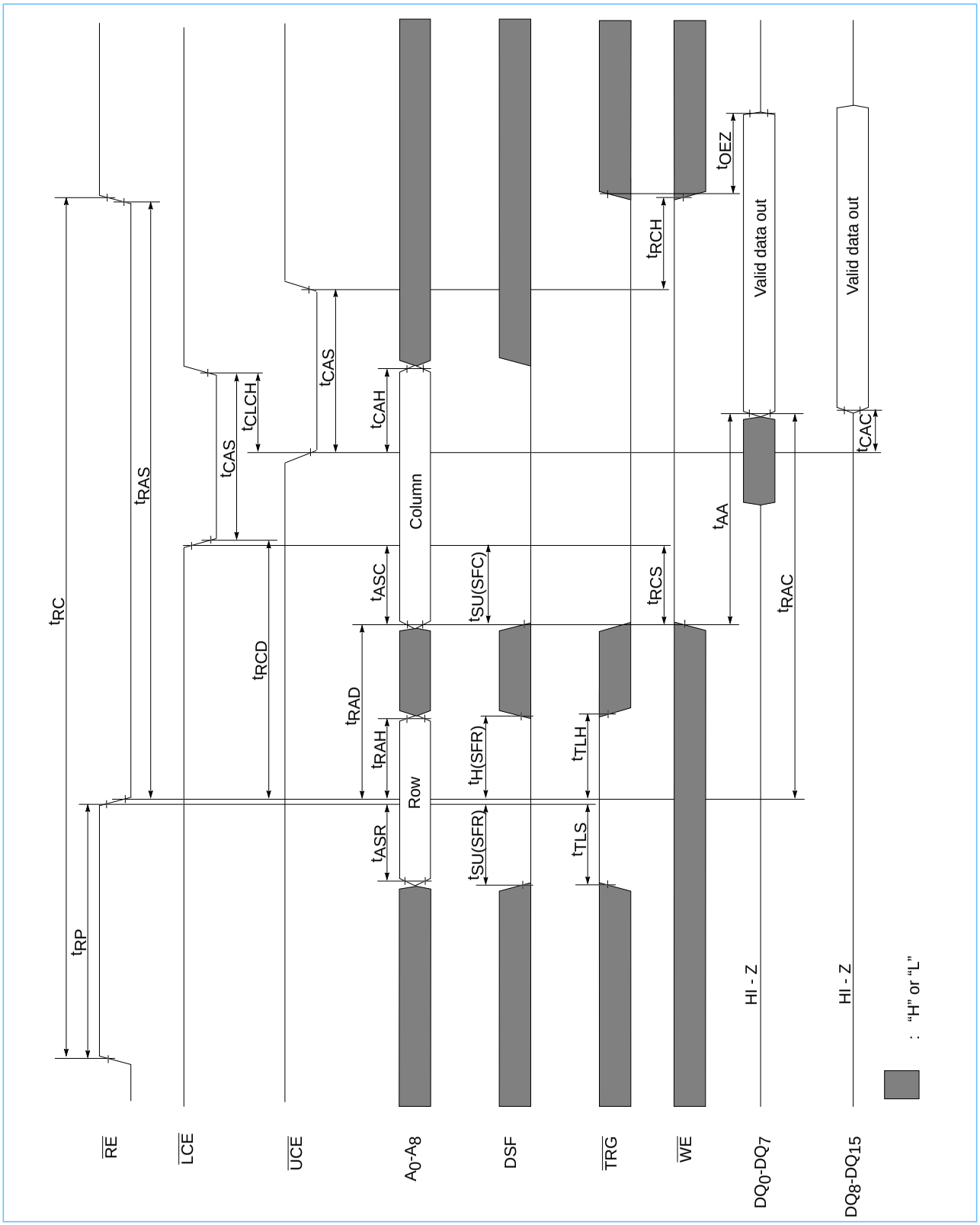
Write Cycle (Late Write)



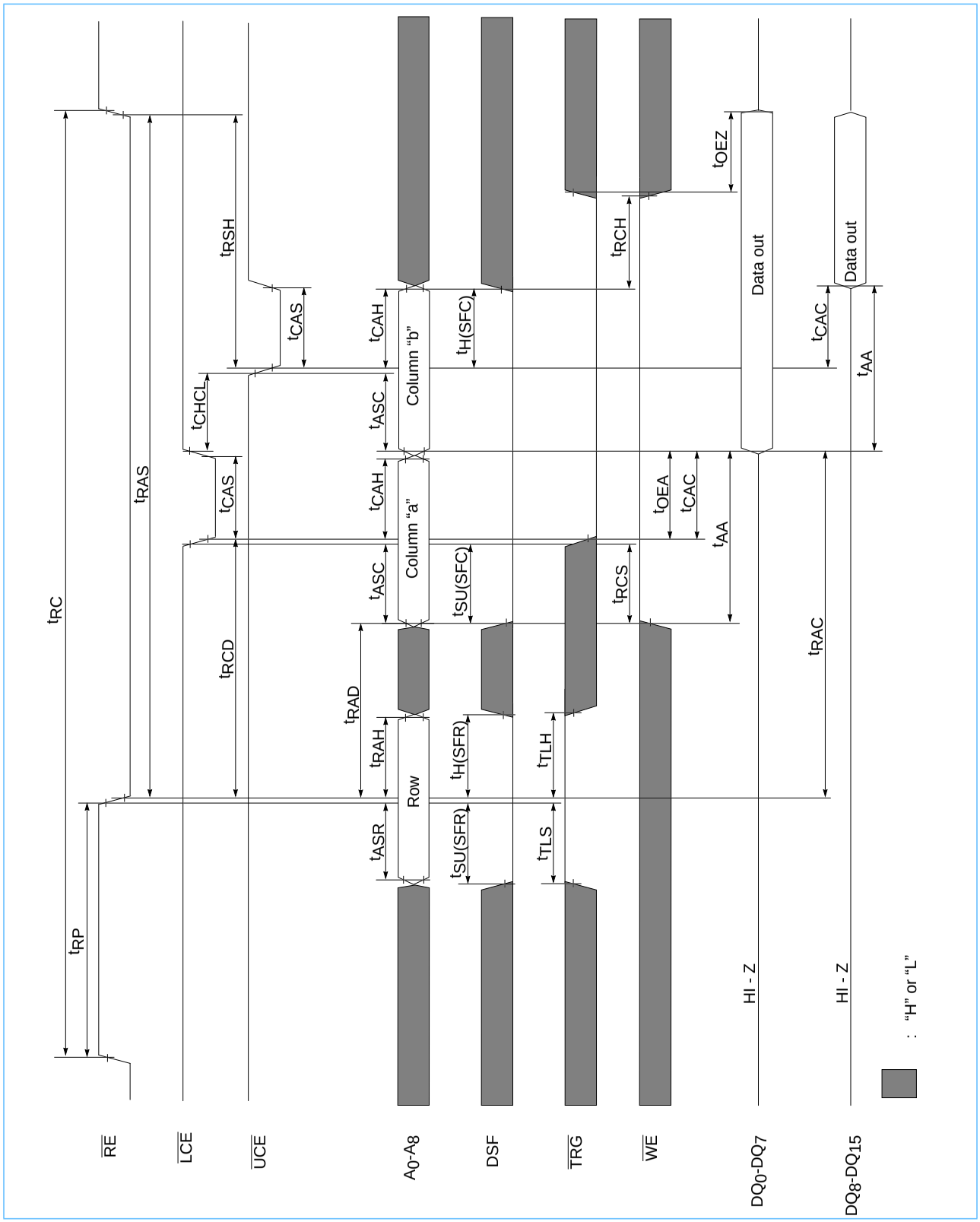
Read-Modify-Write Cycle



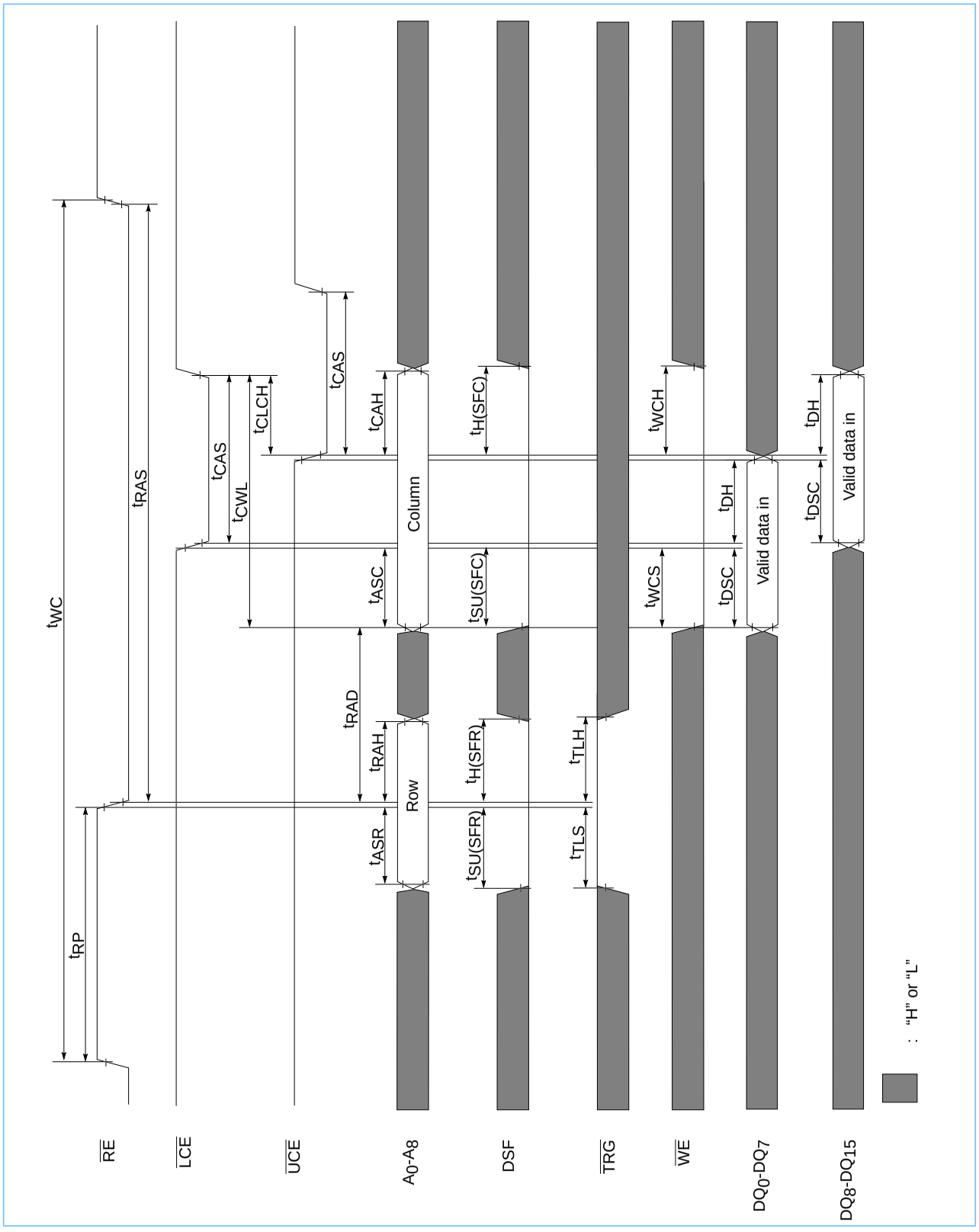
Skewed $\overline{CE}$ (Overlapping $\overline{CE}$) EDO Read Operation



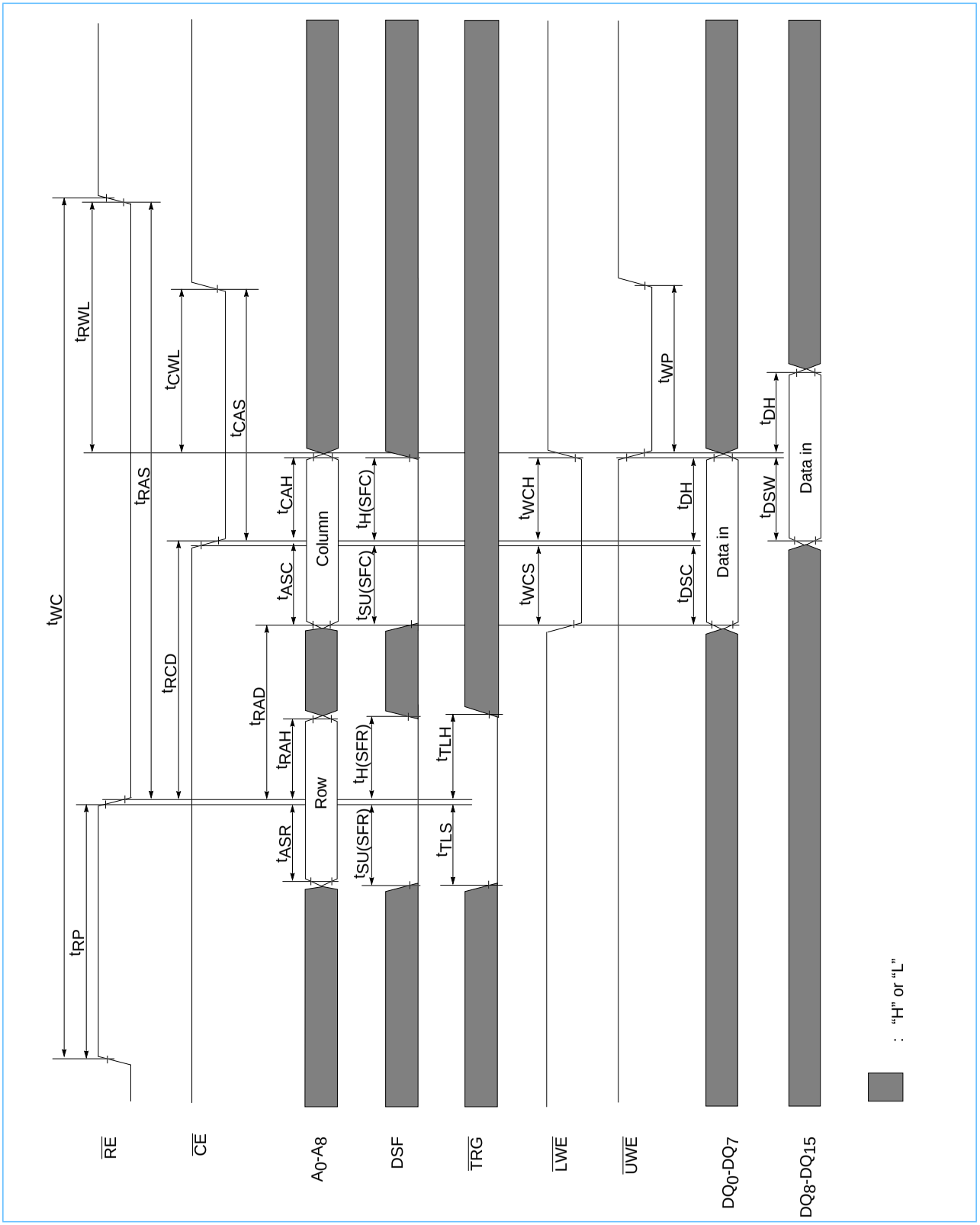
Skewed $\overline{CE}$ (Non-Overlapping $\overline{CE}$) EDO Read Operation



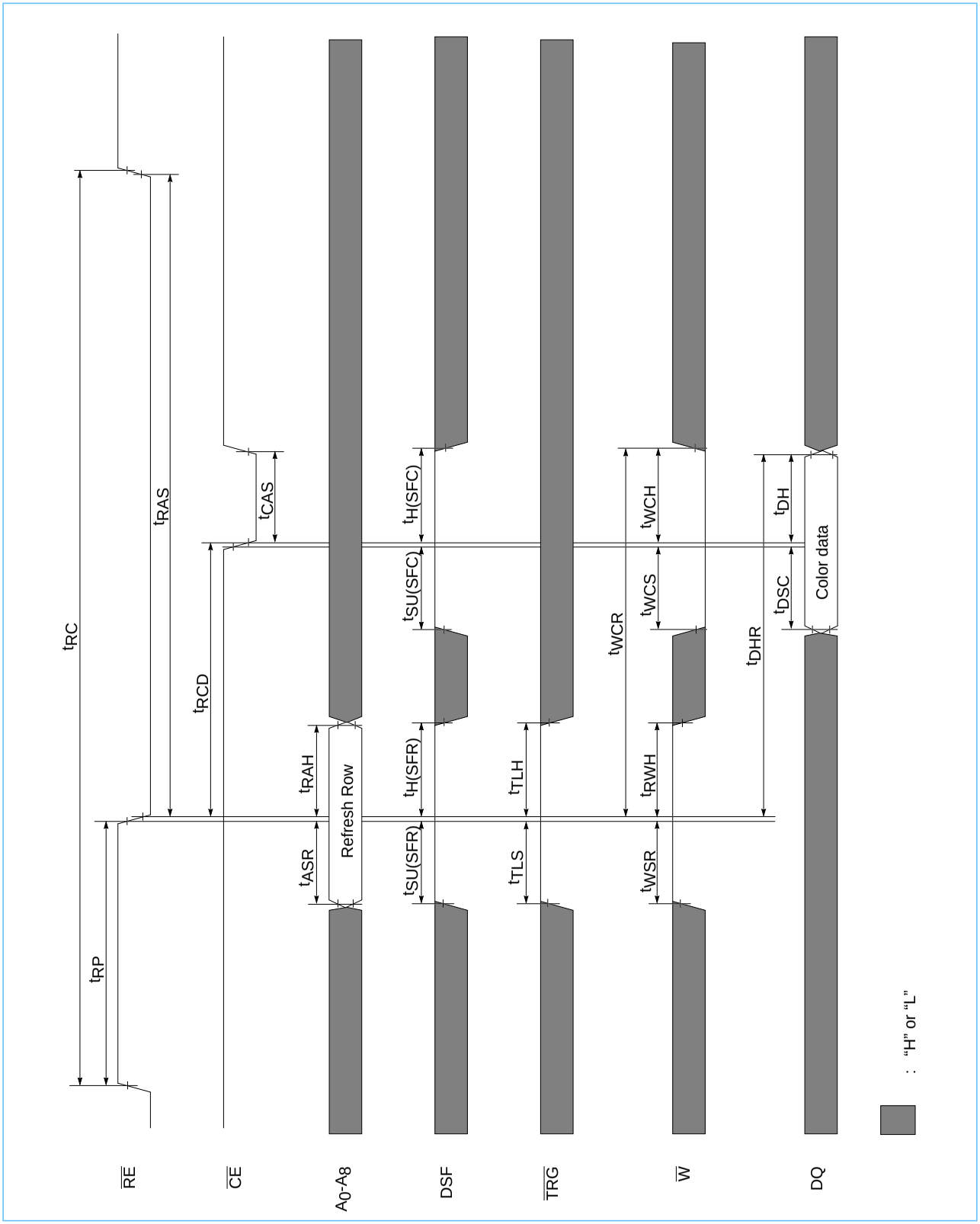
2 $\overline{CE}$ Byte Write Operation ($\overline{CE}$ Overlapping)



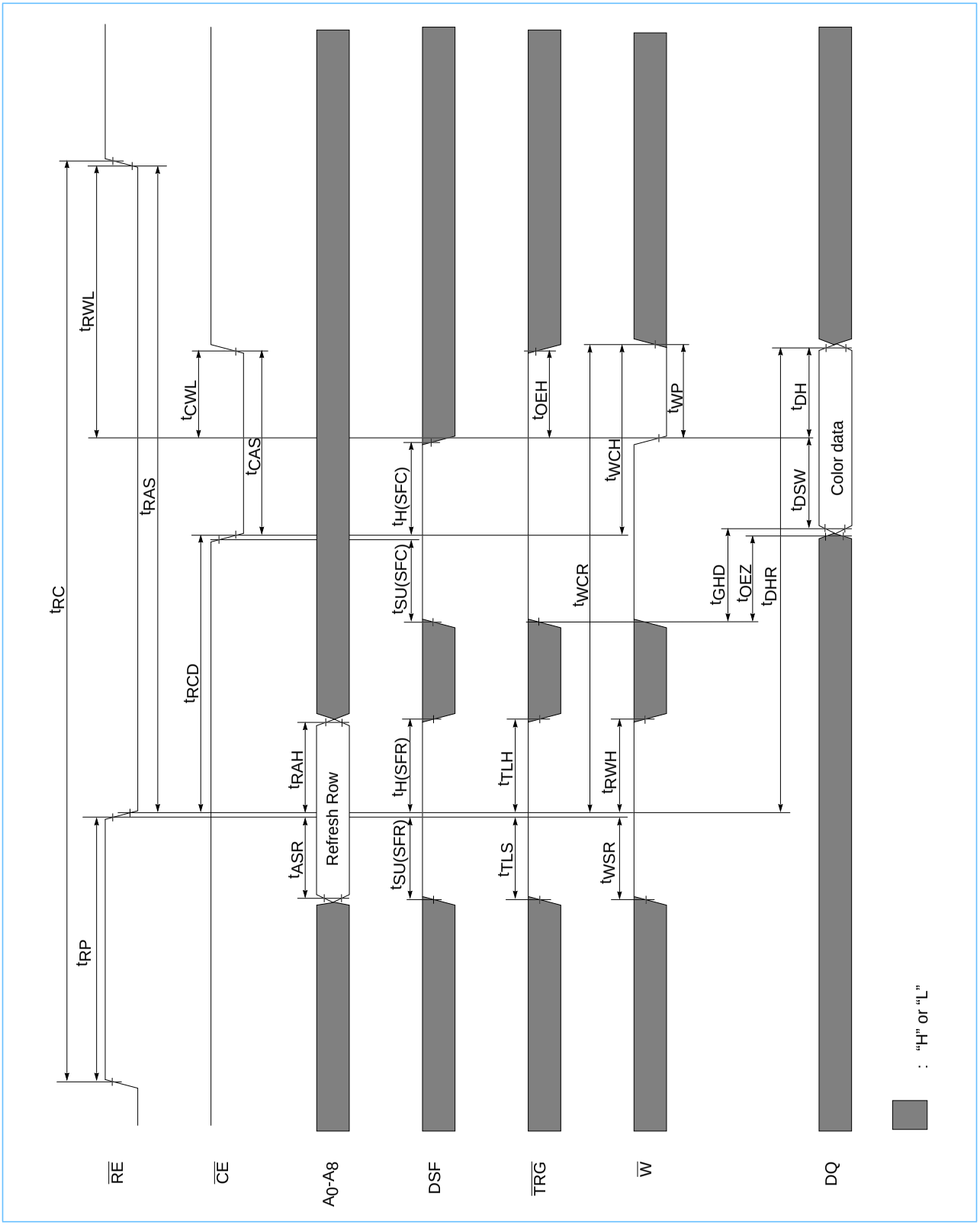
Skewed $\overline{W}$ Operation



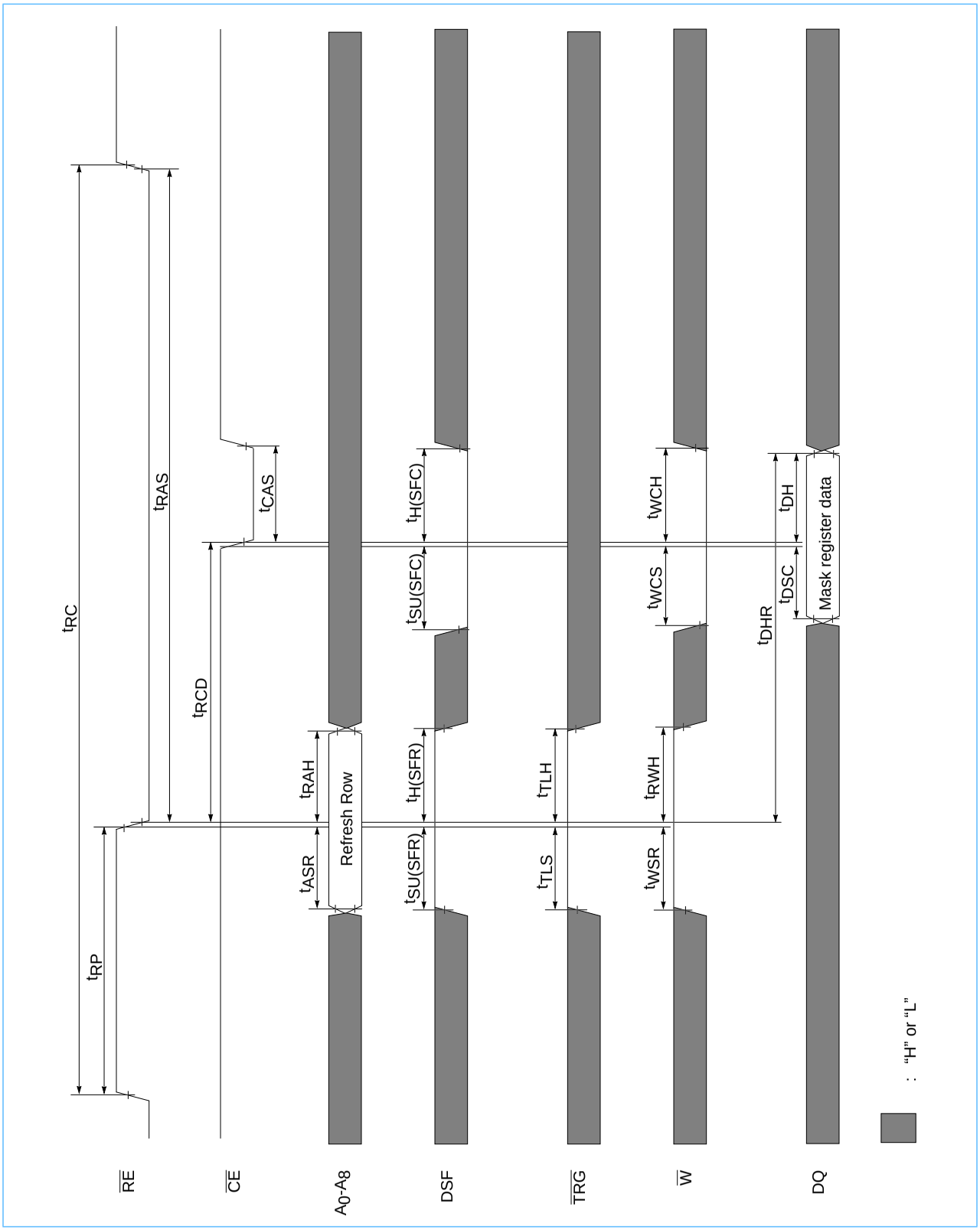
Load Color Register Cycle (Early Load)



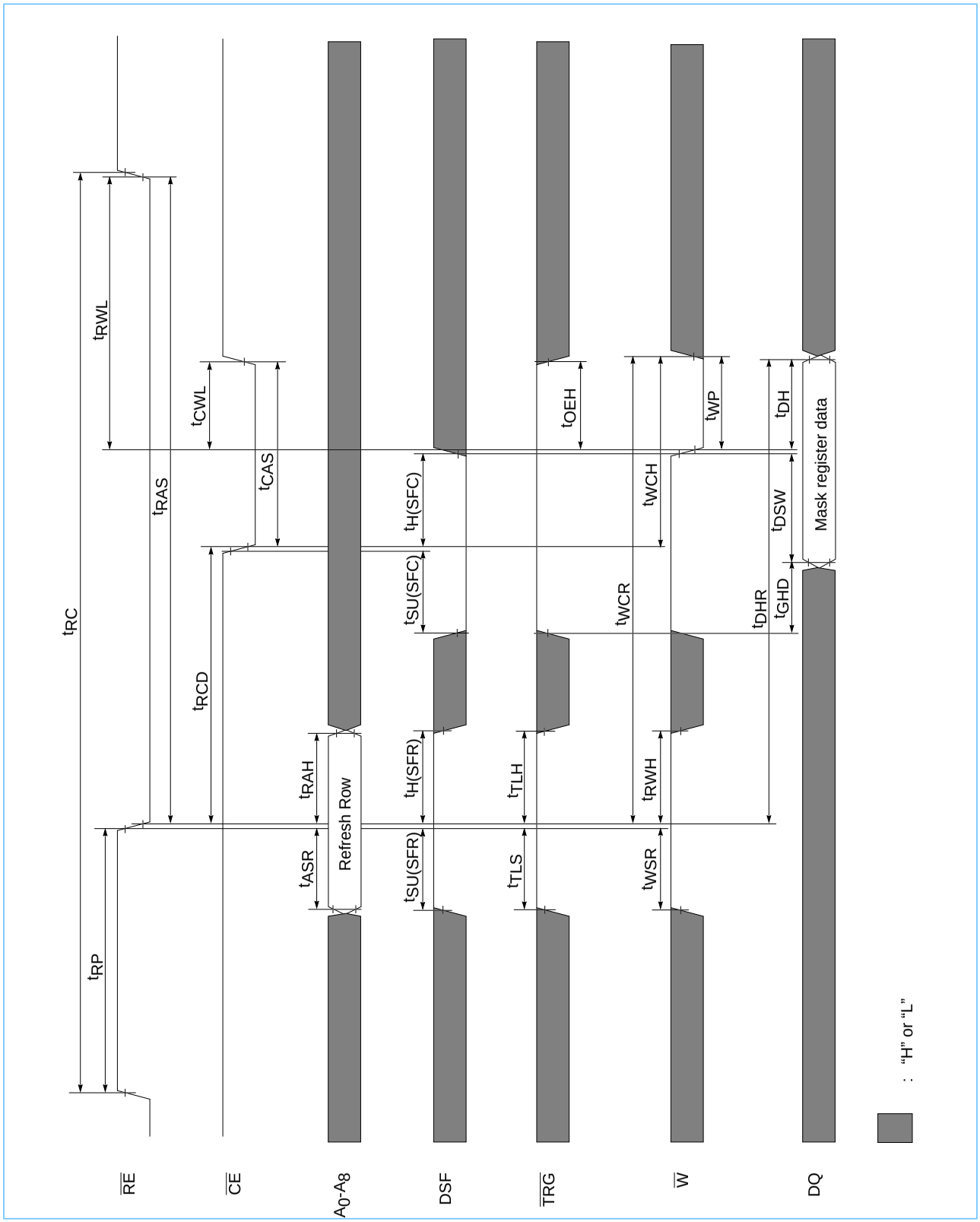
Load Color Register Cycle (Late Load)



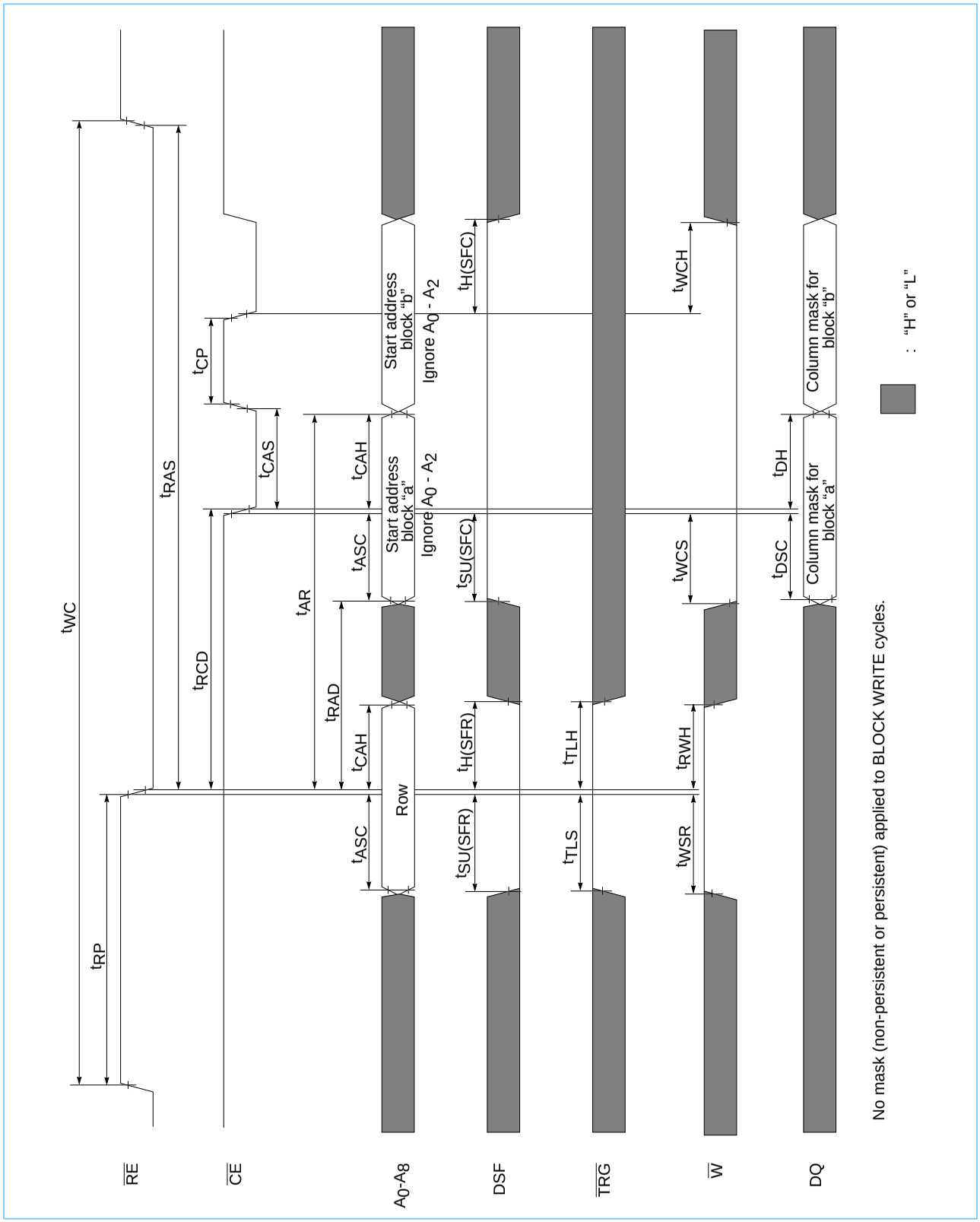
Load Mask Register (Early Load)



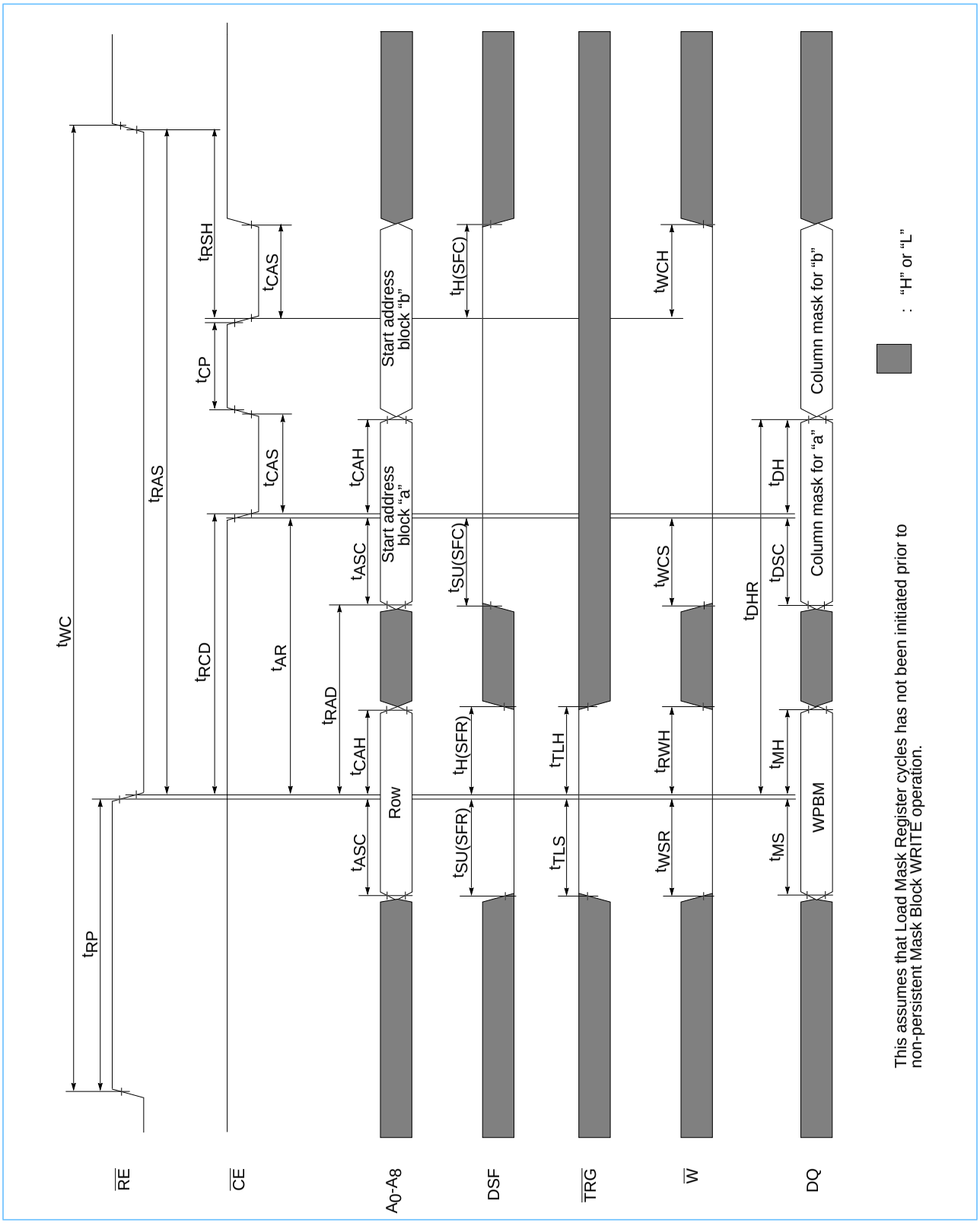
Load Mask Register (Late Load)



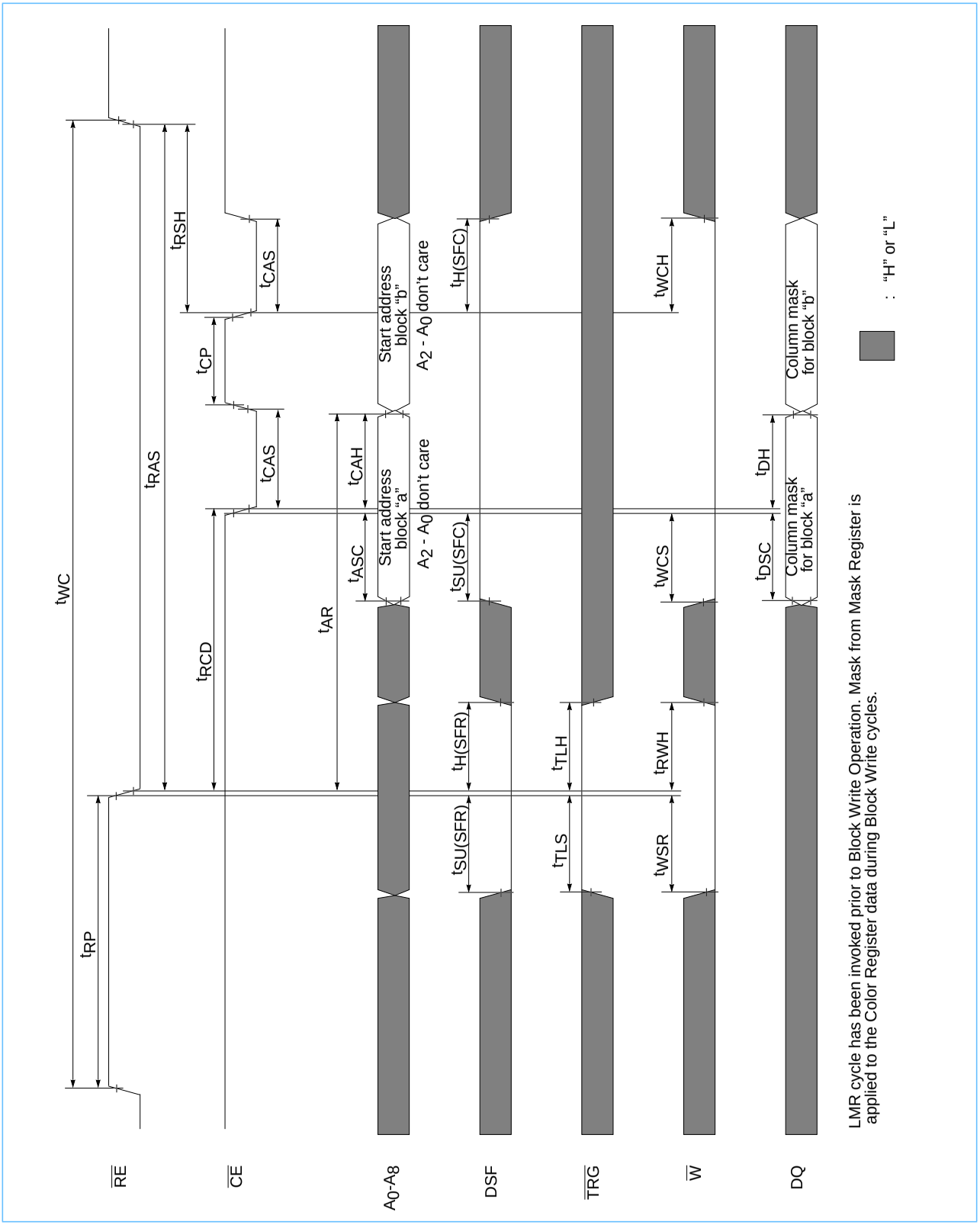
Block Write (No Mask) Operation (Early Write)



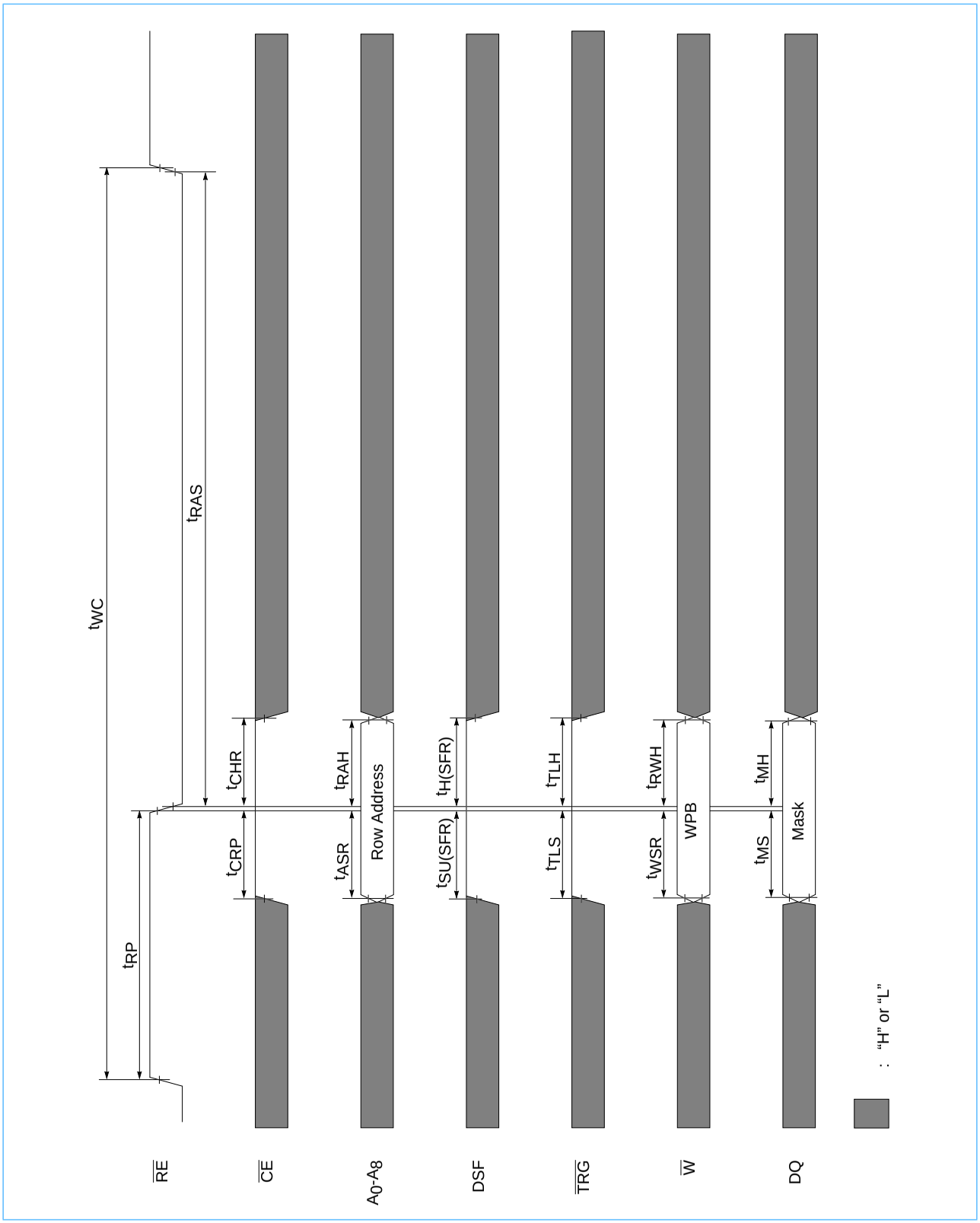
Non-Persistent Mask Block Write Operation (Early Write)



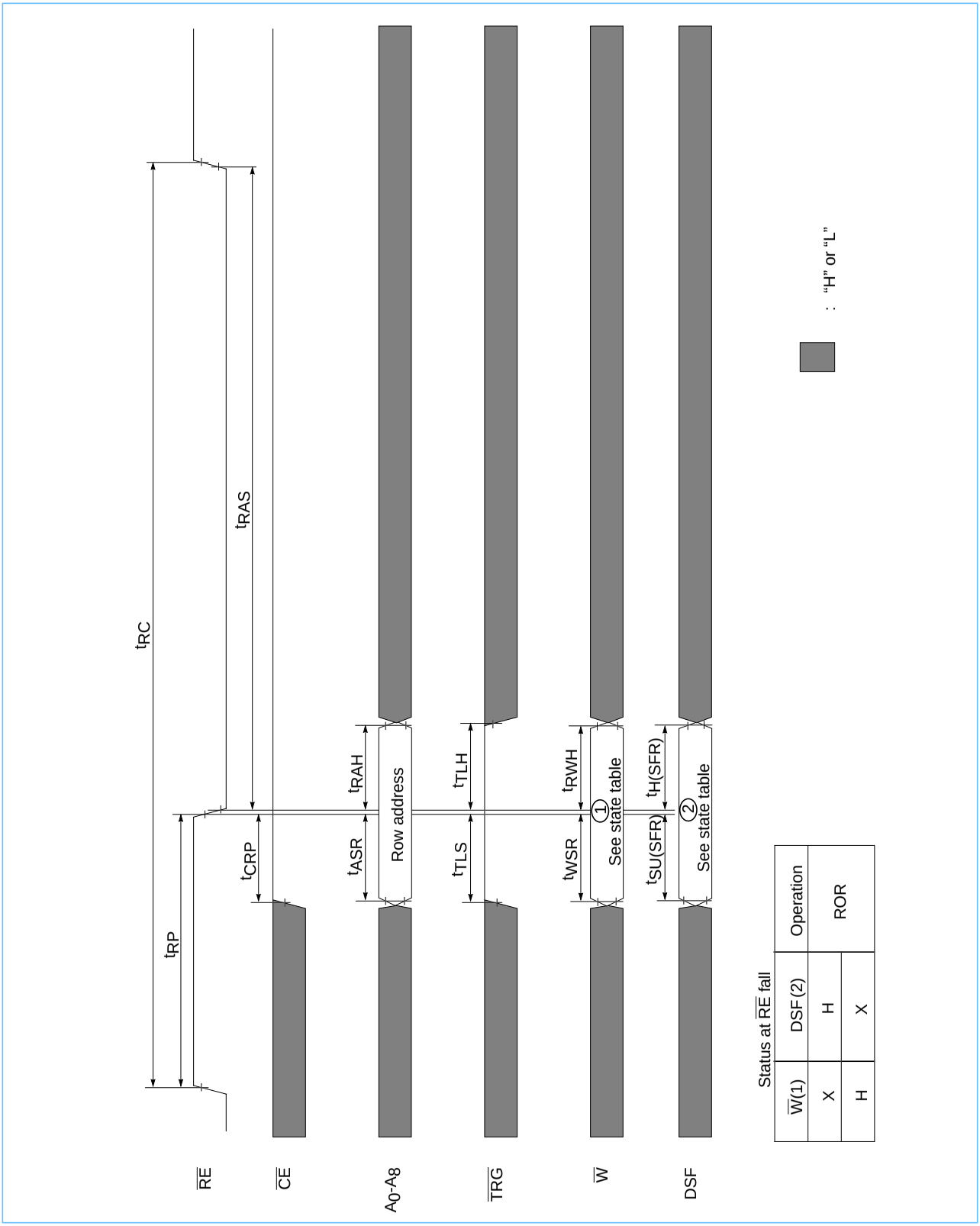
Persistent Mask Block Write Operation (Early Write)



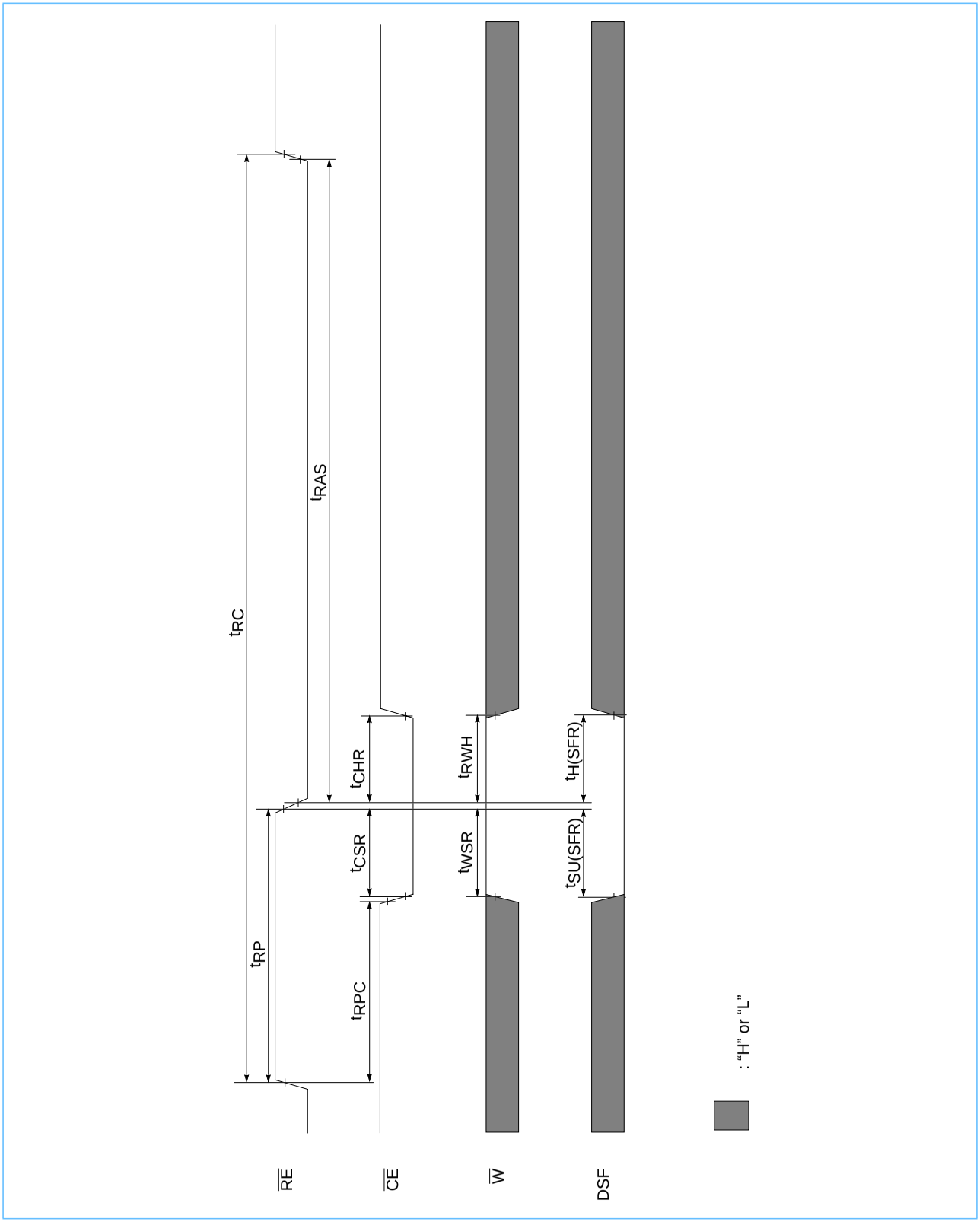
Flash Write Cycle



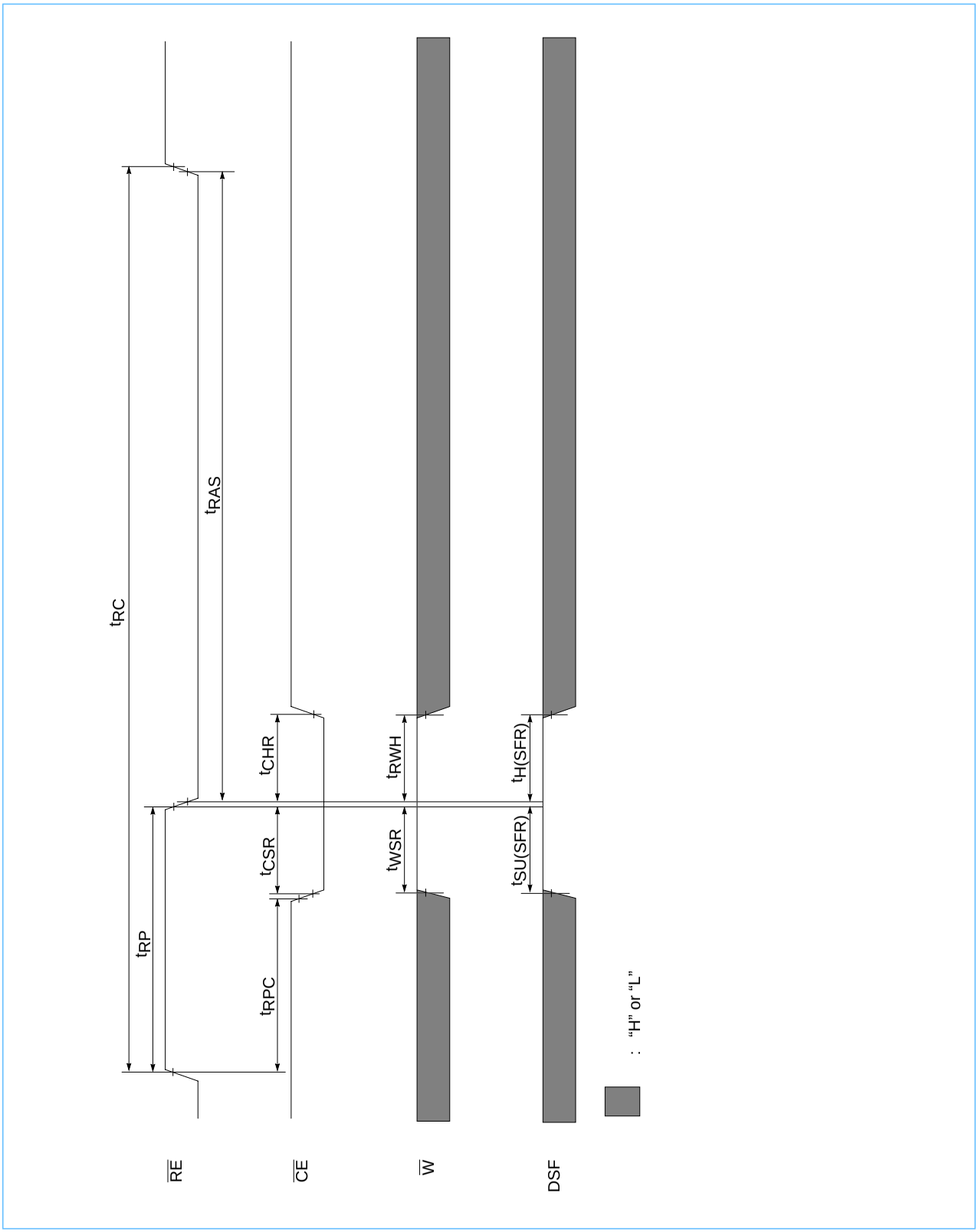
$\overline{RE}$ Only Refresh (ROR)



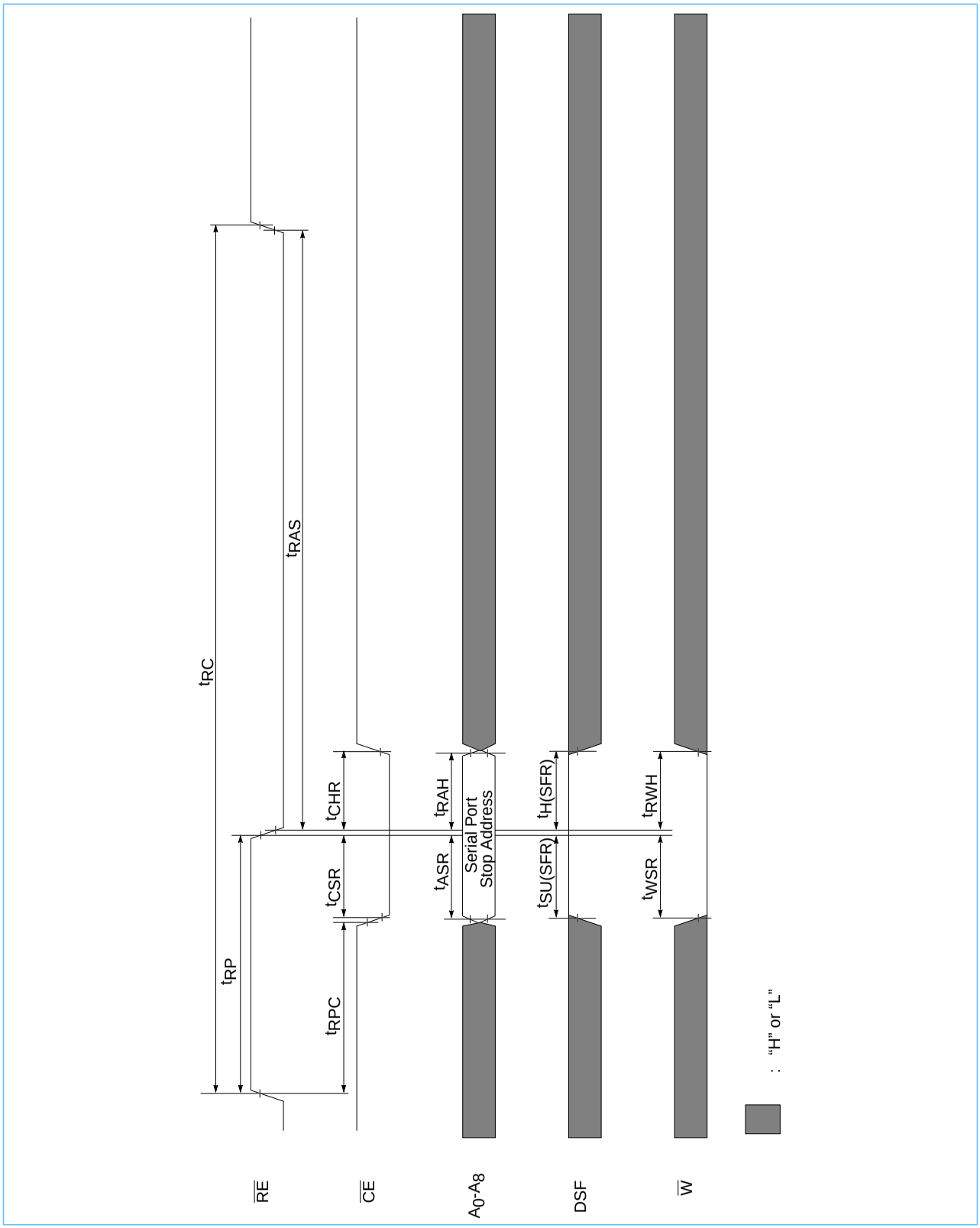
$\overline{CE}$ Before $\overline{RE}$ Refresh (CBR-With Mode Reset)



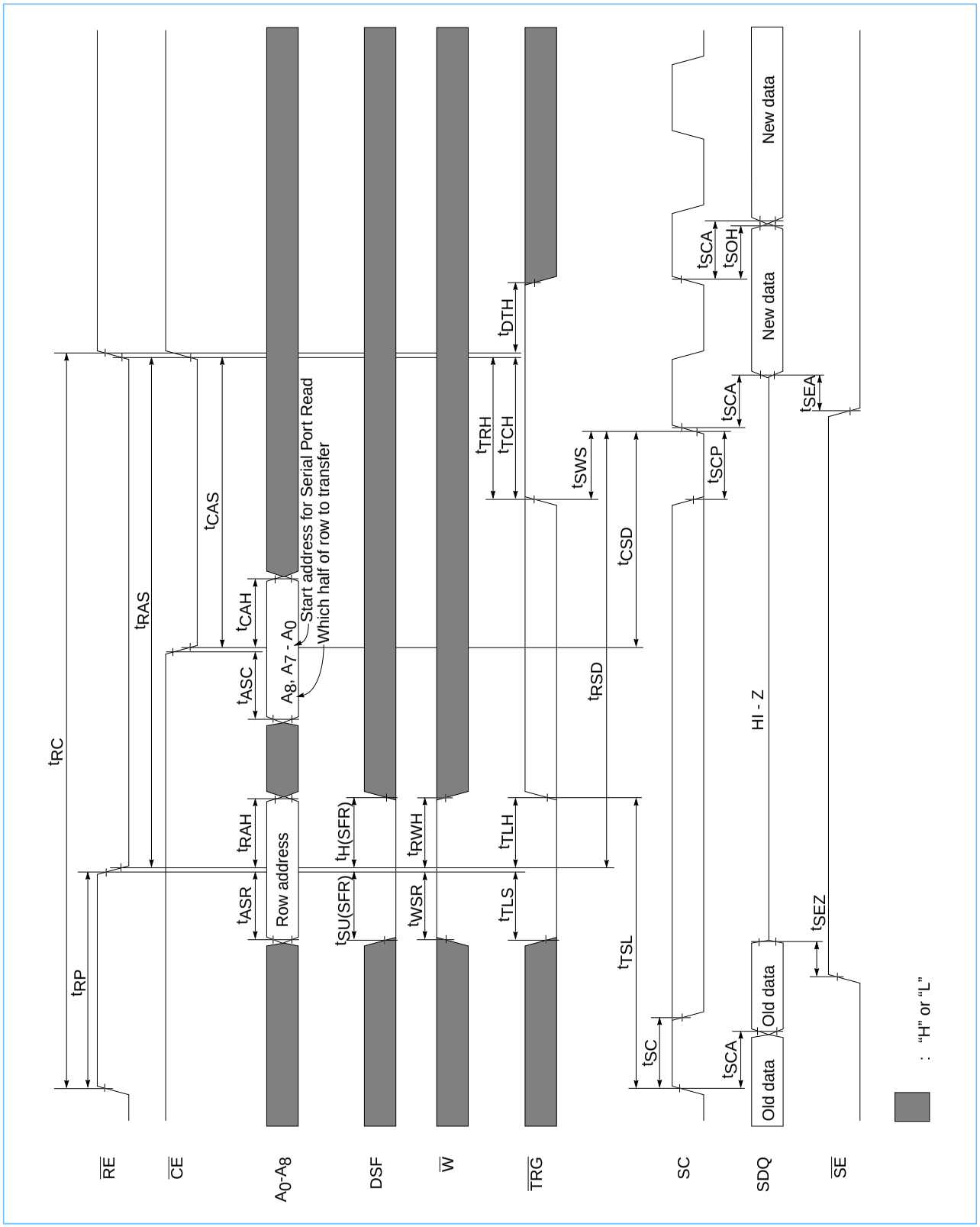
$\overline{CE}$ Before $\overline{RE}$ Refresh (CBRN-No Mode Reset)



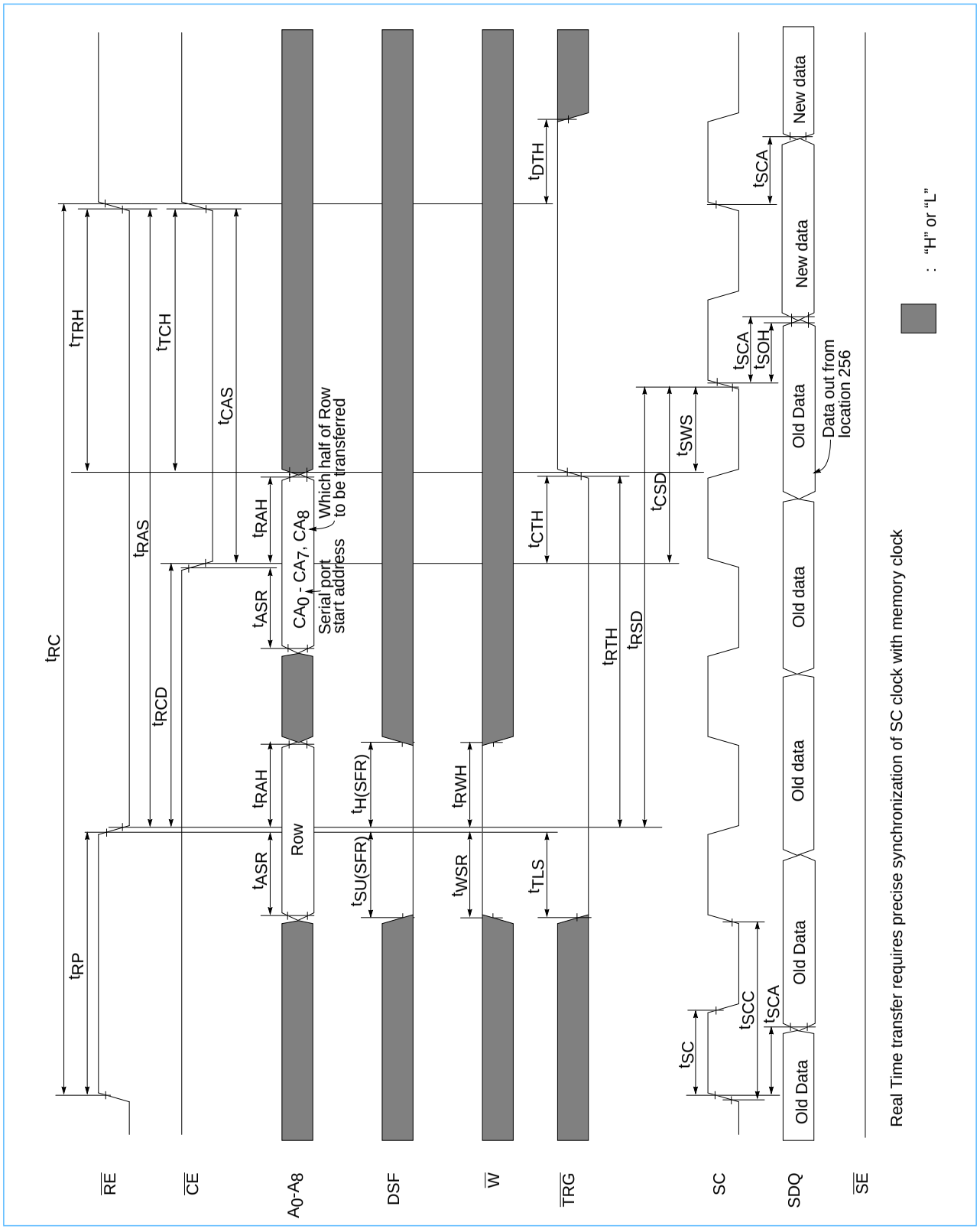
$\overline{CE}$ Before $\overline{RE}$ Refresh (CBRS) Cycle With Stop Register Set



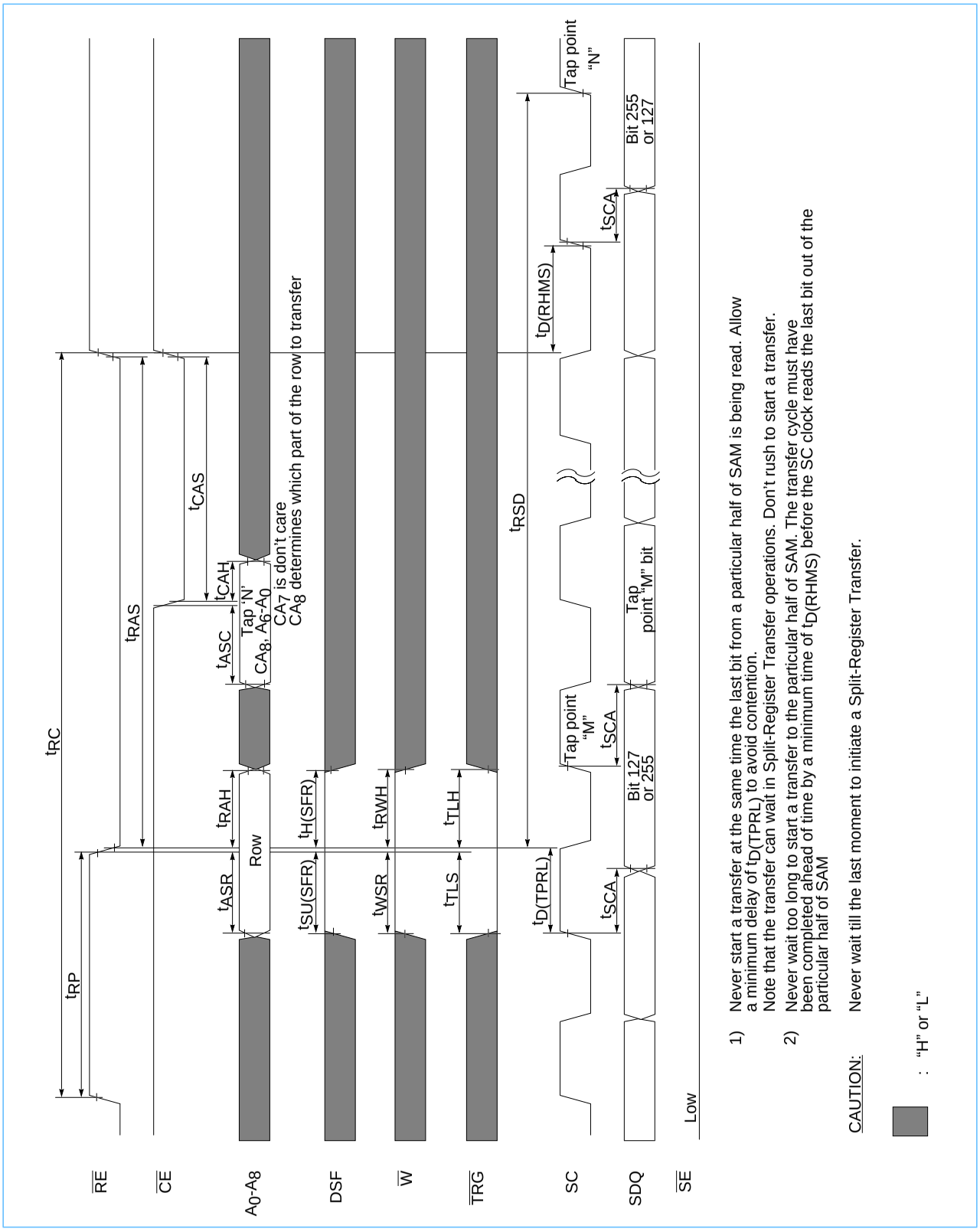
RAM ----> SAM (Full Register Read Transfer)



RAM---->SAM (Real Time) Full Register Read Transfer



Split Register Read Transfer

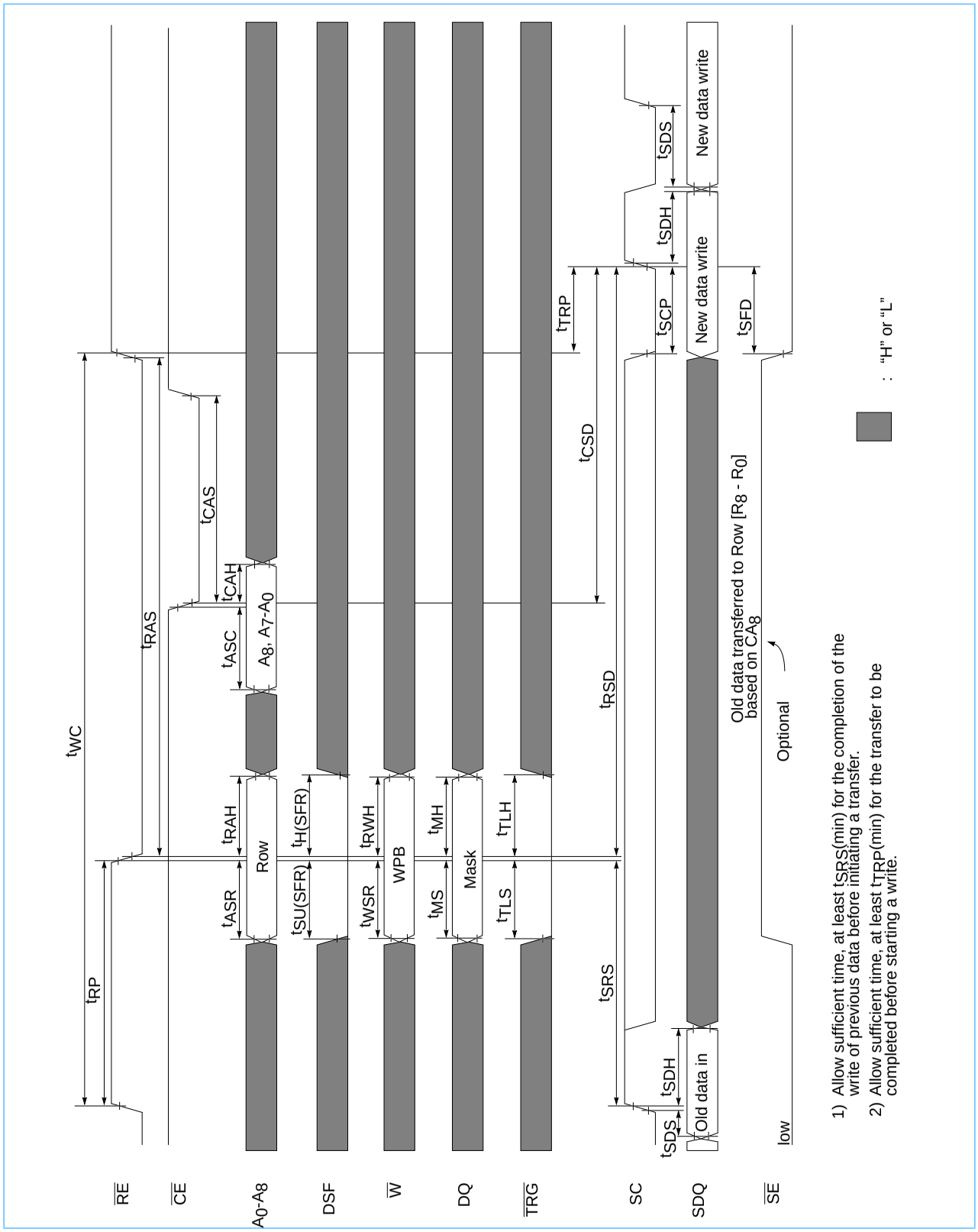


1) Never start a transfer at the same time the last bit from a particular half of SAM is being read. Allow a minimum delay of $t_{D(TPRL)}$ to avoid contention.
Note that the transfer can wait in Split-Register Transfer operations. Don't rush to start a transfer.

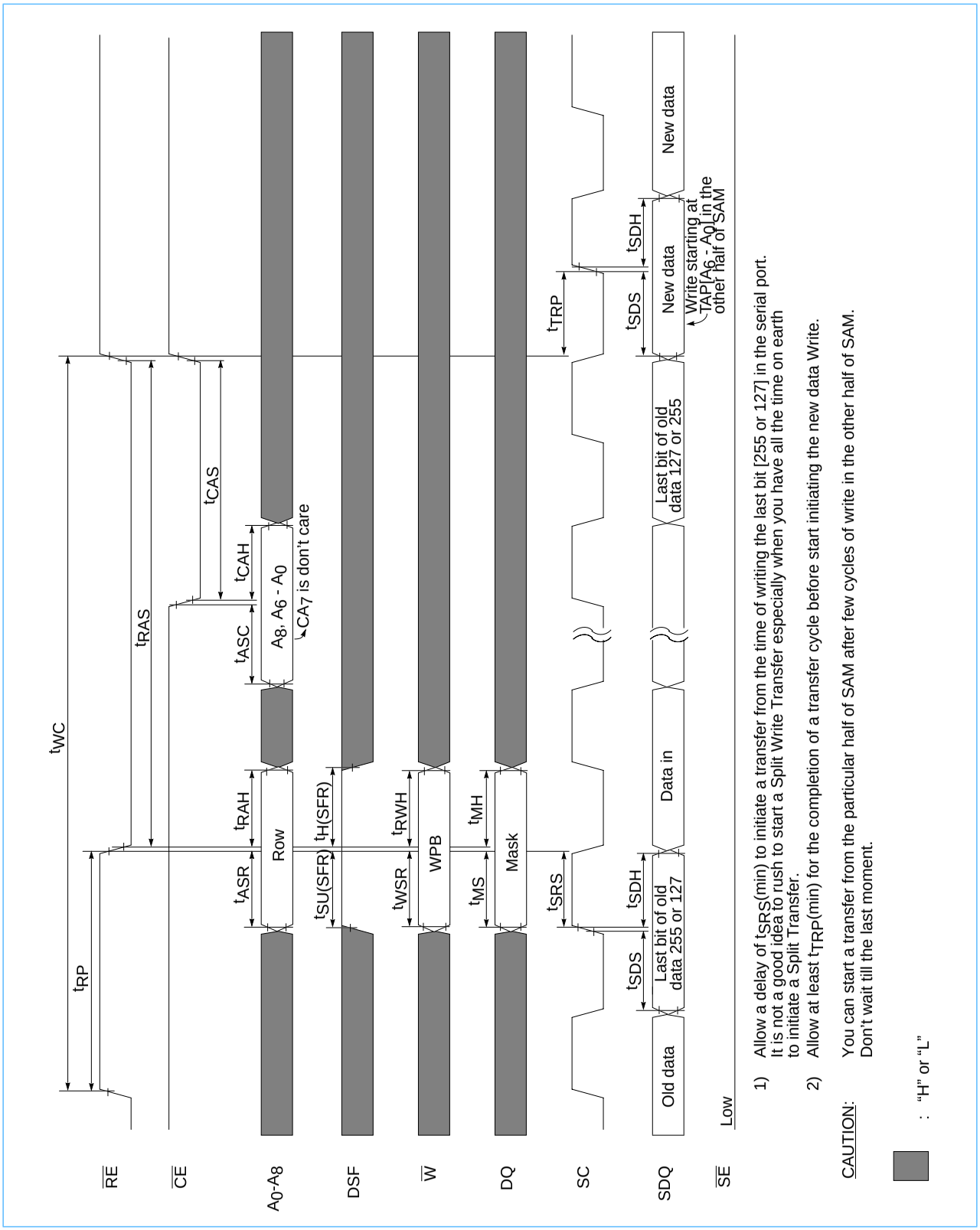
2) Never wait too long to start a transfer to the particular half of SAM. The transfer cycle must have been completed ahead of time by a minimum time of $t_{D(RHMS)}$ before the SC clock reads the last bit out of the particular half of SAM

CAUTION: Never wait till the last moment to initiate a Split-Register Transfer.

Full Register Write Transfer



Split Register Write Transfer



Functional Description

The DRAM array is organized as 512 rows x 512 columns x 16 bit wide. The device is capable of performing normal Read/Write operations similar to a DRAM. Besides fast page Read/Write, the 4-Mb VRAM has the following added functions:

- Full Register Read Transfer
- Split Register Read Transfer
- Full Register Write Transfer
- Split Register Write Transfer
- 8 Column Block Write
- Full Row Flash Write
- Extended Data Out (EDO)
- Serial Port Read
- Serial Port Write

Power Up or VRAM Initialize Process

After V_{CC} has reached its regulated value, allow at least 100µs for build up of N-well voltage inside the chip. Perform at least 8 $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) refresh cycles to reset unwanted mode(s) which may be set during power up. For more details refer to the Application Note, “Designing with 4-Mb VRAM”. ***The Serial port will be initialized with the jump address of 128 bit at power up, thereby requiring no STOP address setting by the user for split Read or split Write in normal mode operations***.

DRAM Refresh Operation

DRAM array consists of volatile cells, therefore these cells need to be refreshed periodically. The minimum rate for VRAM is 512 refresh cycles every 32ms. Every cell therefore gets a chance to be refreshed every 32 ms. The SAM Registers memory is static in nature and therefore requires no refresh.

The following refresh modes are available in IBM's 4-Mb VRAM:

$\overline{RE}$ Only Refresh (ROR)

A cycle having only $\overline{RE}$ active refreshes all cells in one row of the storage array. A high $\overline{CE}$ is maintained while $\overline{RE}$ is active to keep DQs in high impedance.

Note that the row address for refresh is supplied by the user. ***$\overline{RE}$ only Refresh mode will not clear any unknown modes at power up. Therefore, CBR cycles at power up must be performed to clear any unknown modes***. The timing diagram on page 37 shows a $\overline{RE}$ only Refresh mode.

$\overline{CE}$ before $\overline{RE}$ Refresh (CBR)

The CBR Refresh mode is selected by bringing the $\overline{CE}$ low before $\overline{RE}$ is brought low and keeping DSF low as shown in the timing diagram on page 38. An internal address counter selects the row to be refreshed. ***CBR cycle will reset any special modes set by CBRS or any persistent mask***. Note that DQs are in high-Z state during CBR cycle.

$\overline{CE}$ before $\overline{RE}$ Refresh without mode Reset (CBRN)

CBRN mode is set by bringing $\overline{CE}$ low before $\overline{RE}$ is brought low and keeping $\overline{W}$ and DSF high at the falling edge of $\overline{RE}$. The internal counter selects the row to be refreshed**. *CBRN will neither clear any special modes set by the CBRS cycle nor any masks*.**

$\overline{CE}$ before $\overline{RE}$ Refresh with Stop Register Set (CBRS)

The CBRS operation is selected by bringing $\overline{W}$ and $\overline{CE}$ low before $\overline{RE}$ is brought low and keeping DSF high as shown in the timing diagram on page 40. An internal address counter selects the row to be refreshed. This cycle is also used to set the chip into Serial Register Stop mode (SRS). Full compatibility is provided between Half Depth SAM and Full Depth SAM by performing Split Transfer in SRS mode using STOP address of 127 or less. For more details, refer to Application Note, “Half SAM and Full SAM Compatibility”.

Recommended CBR, CBRS, and CBRN Cycles

To ensure that the device has not entered unwanted register modes at power up, at least ***eight CBR cycles must be executed before normal operation of the device is resumed***. A CBR after each vertical retrace is recommended. This fail-safe routine is for cases where a system misoperation causes entry into an unwanted mode. If the STOP Register function is used, then a CBRS must be invoked following every CBR cycle. If the STOP register function is not required and Persistent Write masking is employed, then use a CBRN. CBRN does not clear the old mask.

Byte Control

The 4-Mb VRAM is available with either Dual $\overline{W}$ or Dual $\overline{CE}$. A dual $\overline{CE}$ part has lower and upper byte control. The $\overline{LCE}$ controls the DQ_0 -DQ_7 while $\overline{UCE}$ controls DQ_8 - DQ_{15}. Individual byte control can be applied during read and write operations on the primary port.

A dual $\overline{W}$ part has a lower and upper $\overline{W}$. The $\overline{LW}$ and $\overline{UW}$ allow individual byte control of the DQs during write operations. The $\overline{LW}$ controls DQ_0 -DQ_7 and $\overline{UW}$ controls DQ_8 - DQ_{15}. Individual byte control can be applied to the DRAM Read, Write, Block Write, Load Mask Register and Load Color Register cycles.

Read Cycle

A Read cycle is executed by activating $\overline{RE}$, $\overline{CE}$, and $\overline{TRG}$ and by maintaining $\overline{W}$ high while $\overline{CE}$ is active. The DQs remain in high-Z until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the four calculated intervals:

- t_{RAC} Access time from $\overline{RE}$ falling edge
- t_{RCD} ($\overline{RE}$ to $\overline{CE}$ delay) + t_{CAC} (Access time from $\overline{CE}$ falling edge)
- t_{RAD} ($\overline{RE}$ to Column Address delay) + t_{AA} (Access time from column Address)
- $\overline{RE}$ to $\overline{TRG}$ delay + t_{OEA} (Access time from $\overline{TRG}$)

Device dependent parameters are: t_{RAC}, t_{CAC}, t_{AA} and t_{OEA}. System dependent parameters are: t_{RCD}, t_{RAD} and $\overline{RE}$ to $\overline{TRG}$ delay. Output becomes valid after the access time has elapsed. It remains valid while $\overline{CE}$ and $\overline{TRG}$ are low (Fast Page parts only). It remains valid while $\overline{TRG}$ is low (EDO parts only). Either $\overline{CE}$ or $\overline{TRG}$ high returns the output pins to high-Z (Fast Page parts only). $\overline{TRG}$ high returns the output pins to high-Z (EDO parts only).

Write Cycle

A Write cycle is executed by bringing $\overline{W}$ low during $\overline{RE}$/$\overline{CE}$ cycle. The falling edge of $\overline{CE}$ or $\overline{W}$ whichever occurs later strobes the data on DQ pins into the on-chip data latch.

Early Write Cycle

An early Write cycle is executed by bringing $\overline{W}$ low before $\overline{CE}$ falls. Data is strobed by $\overline{CE}$ with setup and hold times referenced to this signal. This is the mode that is generally used for graphics applications. $\overline{TRG}$ can be in any state while $\overline{W}$ is active.

Late Write Cycle

A late Write is executed by bringing $\overline{W}$ low after $\overline{CE}$ goes low. The input data is strobed by $\overline{W}$ with setup and hold times referenced to $\overline{W}$ signal. The late Write cycle is used for Read-Modify-Write operations.

Write-per-Bit Mask (WPBM) Cycle

A Write-Per-Bit Mask cycle uses an I/O mask function to allow the system designer the flexibility of writing or not writing any combinations of DQ_0 through DQ_{15}. Two types of masking are possible:

1. ***Non-persistent Mask or New mask***

   This mask has to be loaded at each $\overline{RE}$ fall time as shown in the timing diagram on page 34. $\overline{W}$ must be low as $\overline{RE}$ falls. The DQs latched at $\overline{RE}$ fall time are used as mask bits for Write cycle(s) for the particular $\overline{RE}$ cycle. If mask bit is “1”, the corresponding DQ input bit is written. If mask bit is “0”, the corresponding DQ input is not written.

2. ***Persistent Mask or Old Mask***

   If a Load Mask Register cycle has been performed and has not been cleared by a CBR refresh cycle prior to a Write cycle, and $\overline{W}$ is low at $\overline{RE}$ fall time, data at DQ pins at $\overline{RE}$ fall time will be ignored and the data from Mask Register is applied to the following:

   a. ***DQ inputs during Write cycles if $\overline{W}$ is low at $\overline{RE}$ fall time.***

   b. ***Color Register data during Block Write and Flash Write cycles if $\overline{W}$ is low at $\overline{RE}$ fall time.***

Read-Write/Read-Modify-Write Cycle

A Read-Modify-Write is performed by first performing a normal Read, then tri-stating the DQ pins with $\overline{TRG}$, placing data to be written on the DQ pins, and then executing a Write operation. A WPBM can be loaded at the falling edge of $\overline{RE}$. The input data is strobed in reference to $\overline{W}$. This operation is illustrated in the timing diagram on page 24.

Load Mask Register Cycle

In this cycle, data on DQ pins is written to a 16-bit write mask register, where it is retained and used by subsequent masked Write and masked Block Write cycles. This mask can be cleared by executing CBR cycle or by turning the power off. The mask data in the Mask Register can be changed by issuing another Load Mask Register cycle.

Load Color Register Cycle

The load color register cycle is used to load the 16 bit color register, where it is retained to be used for data during Block Write and Flash Write operations.

Block Write Operation

The Block Write Cycles are useful for clearing windows and for accelerating polygon fill operations. In all Block Write operations, the data is always supplied by the color register which is loaded by invoking a Load Color Register operation prior to the Block Write cycle(s). The color register data bits can individually be masked by either loading the mask at $\overline{RE}$ fall time (non-persistent mask) provided that no Load Mask Register operation has been performed prior to invoking Block Write cycle(s). If a Load Mask Register operation has been performed and $\overline{W}$ is low at $\overline{RE}$ fall time, WPBM mask at $\overline{RE}$ time will be ignored and the mask from the Mask Register (persistent mask) will be applied to the color data bits during Block Write cycle(s). ***lower or upper or both bytes can be written during Block Write cycle(s)***. Also a feature known as “individual Column masking” can be used to mask all or any of the 8 columns by loading the column mask at DQ pins at $\overline{CE}$ fall time. This operation is illustrated in and the Application Note, “8 Column Block Write”.

DQ data at $\overline{CE}$ fall time during Block Write cycle(s)

DQ_i = 0, Mask the selected column in the block
DQ_i = 1, Write the data in the selected column in the block

DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8	DQ9	DQ10	DQ11	DQ12	DQ13	DQ14	DQ15
1L	2L	3L	4L	5L	6L	7L	8L	1U	2U	3U	4U	5U	6U	7U	8U

For example, if DQ_0 is “0”, mask the lower byte of column 1 in the block. If DQ_8 is “1”, write in the upper byte of column 1

1L = Lower byte of column 1.

1U = Upper byte of column 1.

Block Write (No Mask)

The data from the color register is written to any or all of the eight columns starting with the column address A_8-A_3 (A_2, A_1, A_0 are don't care). Any column or columns in a block of 8 columns can be masked by latching the DQ data at $\overline{CE}$ fall time during Block Write page cycles in a way as illustrated in the timing diagram on page 33. ***Both $\overline{W}$ should be kept high at $\overline{RE}$ fall time so that no mask is used at Block Write cycle time***.

Block Write (Non-persistent Mask)

The WPBM is loaded by bringing $\overline{W}$ low at $\overline{RE}$ fall time and latching the data present at DQ pins. This mask is applied to the data from Color Register during Block Write page cycles. Note that the masked data is written to all or any of the non-masked columns in the selected block. The WPBM so latched at $\overline{RE}$ fall time is applicable during that particular $\overline{RE}$ active cycle time only.

Block Write (Persistent Mask or Old Mask)

An LMR cycle is initiated to load the Mask Register prior to executing a Block Write operation with persistent mask. The 16-bit Mask Register supplies the bit mask for color register data during page mode Block Write cycles. This masked data is then written to all or any of the non-masked columns in the 8-column block. ***$\overline{W}$ is low at $\overline{RE}$ time and any data on DQ pins at $\overline{RE}$ fall time will be ignored. To clear the persistent mask, a CBR cycle is initiated***.

Flash Write

The Flash Write operation causes an entire row (512 x 16 bits) of data to be written with the contents of the color register. The color register must be loaded on a previous Load Color Register (LCR) cycle. The Flash Write operation can be without Mask, with new mask WPBM or old mask WPBM as explained in mask write operations. The only difference is that the mask is applied for the data in the whole row. ***Note that there is no provision for individual byte control, therefore both the bytes will be written or masked***.

Fast Page Cycle Operation

Fast page mode cycles allow faster memory access by using the same row address while successive column addresses are strobed onto the chip. The $\overline{RE}$ signal is kept low while successive $\overline{CE}$ cycles are executed. The data rate is faster because row addresses are maintained internally and do not have to be reapplied. In fast page mode operation, Read, Write, Read-modify-Write cycles may be executed. During a Fast-page read cycle, the DQ pins stay in high-Z until valid data appears at the output pins at access time. The access time in this cycle will be the longest of the following intervals.

t_{ACP} = Access time from start of column precharge
$t_{CP} + t_T + t_{CAC}$ = Column precharge time + transition time + Access time from $\overline{CE}$ fall time
= $\overline{CE}$ high to column address delay + t_{AA}

Extended Data Out (EDO)

In extended data out mode, the primary port output drivers are not turned off by the rising edge of $\overline{CE}$. As rising edge of $\overline{CE}$ does not turn off the data, the resulting longer data valid time allows speedup of the fast page cycle time. ***Fast page mode applications that try to run at minimum cycle times find that timing skews and propagation delays make the data valid time so narrow that reliable sampling is impossible.*** EDO solves this problem by providing longer data valid time. The device access time is the longest of the following intervals:

- t_{ACP}
- t_{AA}
- t_{CAC}

The detailed explanation of EDO and Fast Page is given in the Application Note, “EDO for Higher Bandwidth”.

Serial Port Operation

The Serial port is always in either Read or Write mode. To switch the Serial port from Read to Write or vice versa, a Transfer operation of the appropriate type must be executed. A Read Transfer operation will put the Serial port into Read mode if it is not already in Read mode. A Write Transfer will switch the Serial port into Write mode if it is not already in Write mode. ***To prevent storing of the current contents of the SAM when first switching to Write mode, a Write transfer operation with the WPBM set to block all 16 bits should be performed***. when $\overline{SE}$ is low, each serial clock will cause a Read/Write of the SAM location addressed by the internal Serial port address counter. When $\overline{SE}$ is high, the Serial port is disabled for Read/Write, and the SDQs are in high-Z state. ***Note that Each SC clock causes the internal address counter to increment independent of the state of $\overline{SE}$***.

Transfer Modes

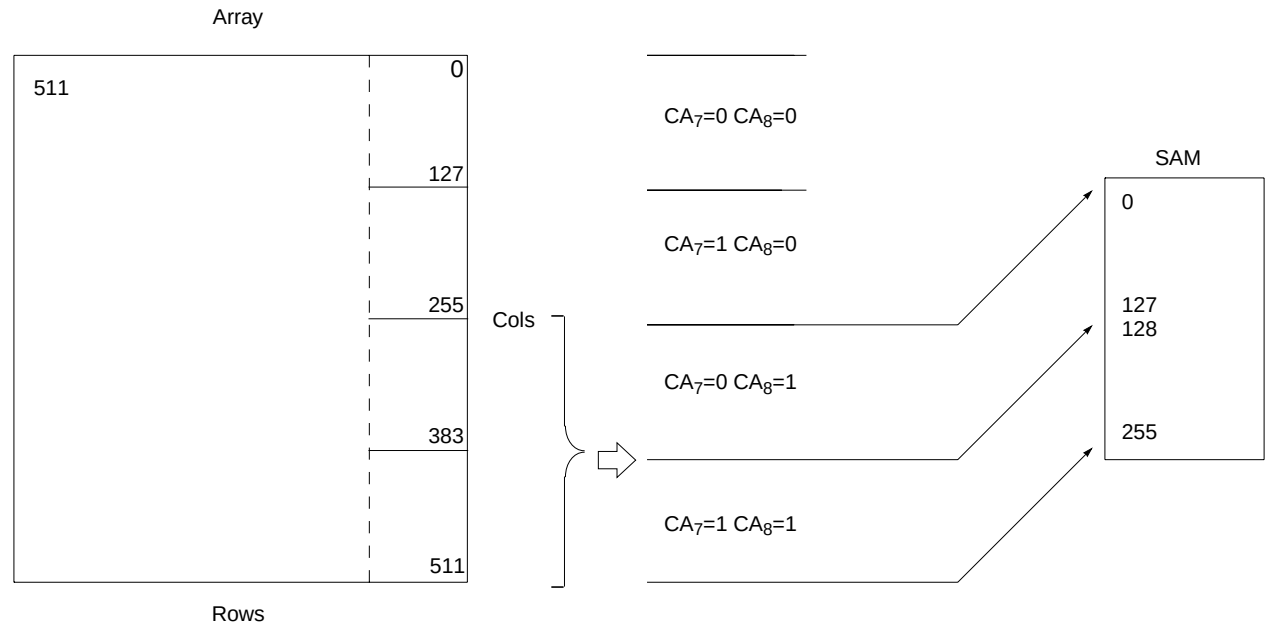
The following Transfer Modes are available:

1. Full Read Transfer (Normal) Mode.
2. Split Read Transfer (Normal) Mode.
3. Full Read Transfer (SRS) Mode.
4. Split Read Transfer (SRS) Mode.
5. Full Write Transfer (Normal) Mode.
6. Split Write Transfer (Normal) Mode.
7. Full Write Transfer (SRS) Mode.
8. Split Write Transfer (SRS) Mode.

Full Register Read Transfer (Normal) Mode

The Full Register Read Transfer operation is illustrated in the timing diagram on page 41. This operation will load the entire SAM (256 x16 bits) from the selected segment of the row. CA_8 controls which half of the selected row needs to be transferred. If CA_8 at $\overline{CE}$ fall time is “0”, the lower half of the selected row is transferred. If CA_8 at $\overline{CE}$ fall time is “1”, the upper half of the selected row is transferred. CA_7-CA_0 address supplied by the user at $\overline{CE}$ fall time is used to provide the starting address for reading of data from the Serial port. The SAM has 256 locations to be addressed starting from 0 to 255. During the Full Read Transfer cycle the Start Address Register as well as the Serial port counter will be loaded, with the user supplied address CA_7-CA_0. CA_7 equals “0” is associated with the lower half of the SAM and CA_7 equals “1” is associated with the upper half of the SAM. A Full Register Read Transfer from the selected row to SAM is shown in the timing diagram on page 51. The example shows a transfer based on user supplied CA_8 equals “1”. The Serial port counter is set to the address CA_7-CA_0 specified by the user at $\overline{CE}$ fall time during the Full Read Transfer cycle. The next SC cycle following the transfer will start reading data from this point in the SAM. Reading will continue until the end of the SAM location 256 and will wrap around. To keep Serial data out continuous, either a Split Read Transfer or a Full Read Transfer must be executed as the SAM runs out of new data. See the timing diagrams for the necessary timing requirements for either method of loading the SAM

Full Register Read Transfer (Normal) Mode



Split Register Read Transfer (Normal) Mode

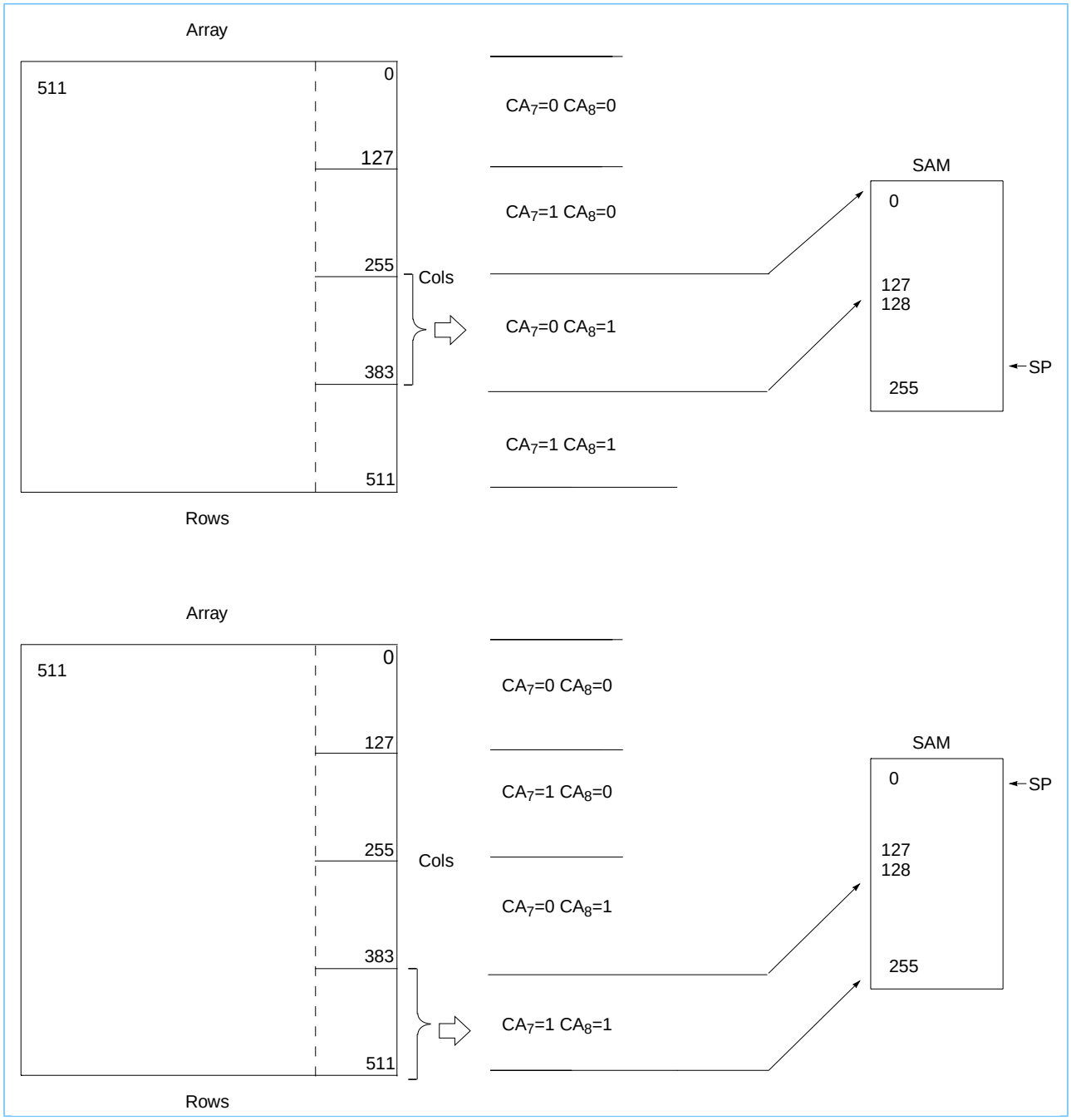
The Split Read Transfer is used to read data continuously from the Serial port without having to worry about synchronizing the SC clock with the operation of the primary port. This transfer operation loads 128 x16 bits of a wordline into half of the SAM. The user supplied column address bit "CA_8" and an internally generated "CA_7" determines which quarter of the word line is transferred to the SAM.

Note the user supplied "CA_7" at $\overline{CE}$ fall time during transfer cycle is a don't care and is internally generated based on which half of the SAM is active. This way, the inactive half of SAM can be loaded with the new data while data is being read out of the other active half. The start address is given by CA_6 - CA_0 but is held in a TAP address pointer register until the serial counter reaches the jump address (127/255). At that point, the start address register is loaded with the address from the TAP address register. The Serial port counter will also be loaded with this address at the same time. The reading of data will start from this address in the other half of SAM that was previously inactive at the next SC clock. The Split Read Transfer in normal mode is illustrated in the timing diagram on page 43.

The example in the timing diagram on page 53 illustrates a Split Read Transfer between DRAM and SAM based on user supplied CA_8 during Split Read Transfer cycle and an internally generated CA_7. In the first example (CA_8 = 1), the Serial port is active reading data from the upper half of the SAM while the lower half of SAM is idling. Therefore, CA_7 is internally changed to "0" and the transfer is forced to lower half of SAM. In the second example, the Serial port is active reading data from the lower half of SAM, the transfer is therefore forced to the upper half of SAM.

Note: There must be a Full Read Transfer prior to any Split Read Transfer. After the Full Read Transfer, any number of Split Read Transfers can be performed. The Split Read Transfer can be initiated to the idling part of SAM at any time while the active half is being read. It is generally a good practice to perform a Split Read Transfer to the idle half of SAM at any time way ahead of the last data being read out of the active half of SAM.

Split Register Read Transfer (Normal) Mode



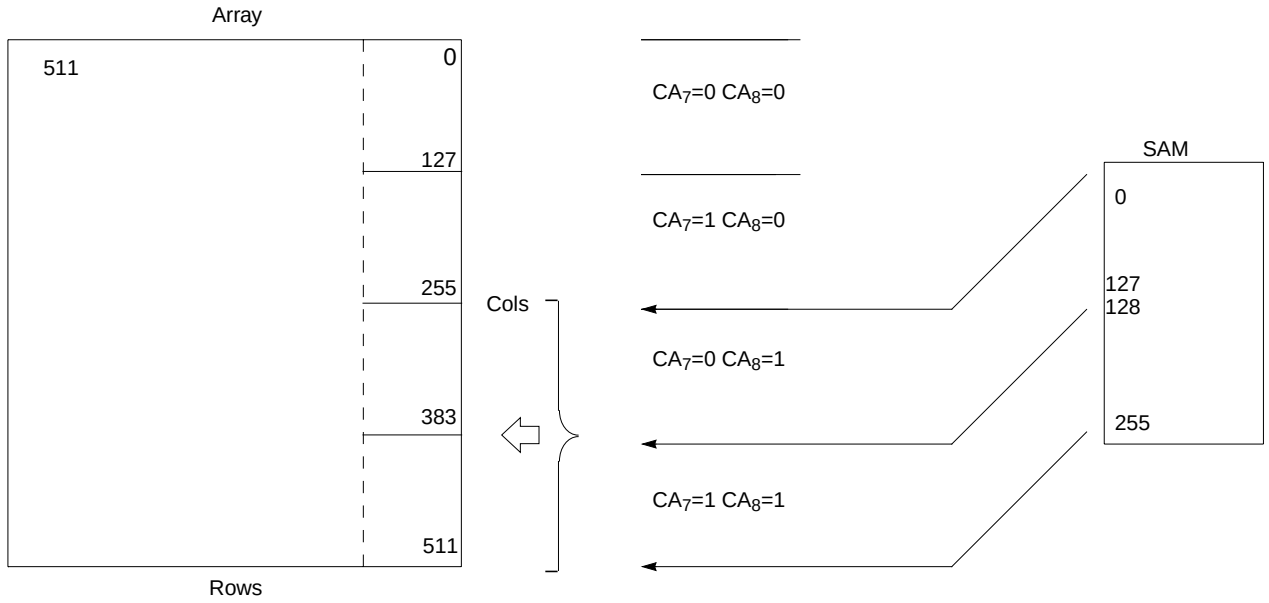
Full Register Write Transfer (Normal) Mode

The Full Write Transfer operation is illustrated in the timing diagram on page 44. This operation will store the contents of the SAM at the address specified by row address (RA_8 - RA_0) and CA_8.

CA_8 controls the transfer of data to the particular half of the row. If CA_8 at $\overline{CE}$ fall time is “0”, the data from SAM is stored in the lower half of the row. If CA_8 at $\overline{CE}$ fall time is “1”, the upper half of the selected row is loaded. CA_7-CA_0 address supplied by the user at $\overline{CE}$ fall time in a transfer cycle is used to provide the starting location for writing the data in the Serial port on the next SC clock following the transfer. During the Full Write Transfer cycle, a WPBM can be loaded at $\overline{RE}$ fall time to mask the selected data bits at transfer time. ***Generally, it is a good practice to mask all the data bits at the first Full Write Transfer cycle to prevent transferring of old data left over from previous Read Transfer operations.***

A Full Register Write Transfer from SAM to DRAM is shown in the timing diagram on page 54. The example shows a transfer based on user supplied CA_8 equals “1”. The Serial port counter is set to the address CA_7-CA_0 specified by the user at $\overline{CE}$ fall time during the Full Register Write Transfer cycle. The next SC clock following the transfer will start writing data from this point in the SAM.

Full Register Write Transfer (Normal) Mode



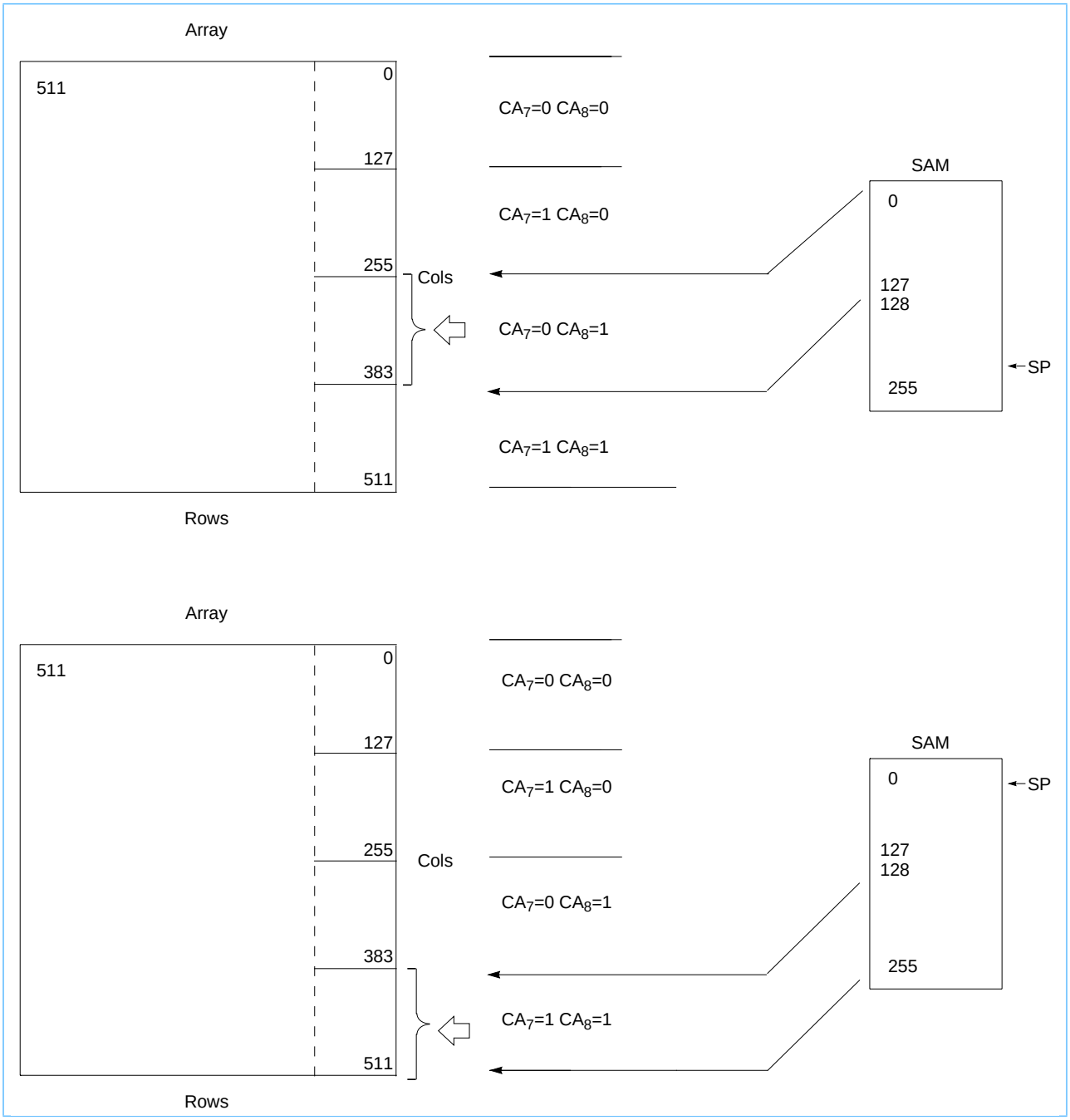
Split Register Write Transfer (Normal) Mode

The Split Write Transfer is used to write data continuously in the Serial port without having to worry about synchronizing the SC clock with the operation of the primary port. This transfer operation stores 128x16 bits from SAM in the selected row segment. CA_8 at $\overline{CE}$ fall time during a Split Write Transfer cycle determines to which half of the row the data from SAM is going to be stored. ***CA_7 is a don't care and is internally generated based on which half of the SAM is active***. This way, the data from the idle part of SAM can be transferred to the selected row in DRAM while the new data is being written in the active half of SAM. The start address is given by CA_6 -CA_0 but is held in the TAP address register until the Serial port counter reaches the jump address. At that point, the start address register is loaded with the address from the TAP address register and the Serial port counter will also be loaded with this address at the same time. The writing of data in the previous inactive half of SAM will start at this address at the next SC clock. The Split Write Transfer in normal mode is illustrated in the timing diagram on page 45.

The example in the timing diagram on page 56 illustrates a Split Write Transfer between SAM and DRAM based on user supplied address CA_8 at $\overline{CE}$ fall during transfer cycle and an internally generated CA_7. In the first example, the Serial port is active writing data in the upper half of the SAM while the lower half of SAM is idling. Therefore, CA_7 is internally changed to “0” and the transfer is forced to lower quarter of the upper half of the selected row based on CA_8 = 1. In the second example, user supplies bit CA_8 is “1” and the Serial port is active writing data in the lower half of SAM, the transfer is therefore forced to the uppermost quarter of the selected row.

Note: A Full Write Transfer with WPBM must be performed before the start of any Split Write Transfer. After the Full Write Transfer, any number of Split Write Transfers can be performed. The Split Write Transfer can be initiated from the idling part of SAM at any time while the active half is being written. It is generally a good practice to perform a Split Write Transfer from the idle half of the SAM at any time which is way ahead of the last data being written into the active half of the SAM.

Split Register Write Transfer (Normal) Mode



Serial Register Stop (SRS) Mode

The SRS mode is very useful in applications where the DRAM data is arranged in the form of tiles and the Serial port is read out in scan line order. A typical case is that of vectors that cross many scan lines on the screen. The pixels for vector(s) can be written in a single row or minimum number of rows depending on the tile width using page mode cycles. A detailed explanation is given in the Application Note, “Read/Write Transfer Operation”. The SRS mode is set by executing CBRS cycle just after power up. The 4-Mb VRAM has an 8-bit Stop Register. The Stop Register value is latched at the falling edge of $\overline{RE}$ during CBRS cycle using address inputs A_4-A_7 (A_0-A_3 and A_8 are don't care). Up to eight different stop positions or boundaries can be specified for each half of SAM as shown in the Stop Register Set table on page 57 by invoking a CBRS cycle.

Stop Register Set

Address by User A_8 - A_0	Stop Register Value: A_7 - A_0	If the Serial port counter is less than 128, the STOP address is equal to whichever occurs first
X 1111 XXXX X 0111 XXXX X 0011 XXXX X 0001 XXXX	0111 1111 0011 1111 0001 1111 0000 1111	127 63,127 31,63,95,127 15,31,47,63,79,95,111,127

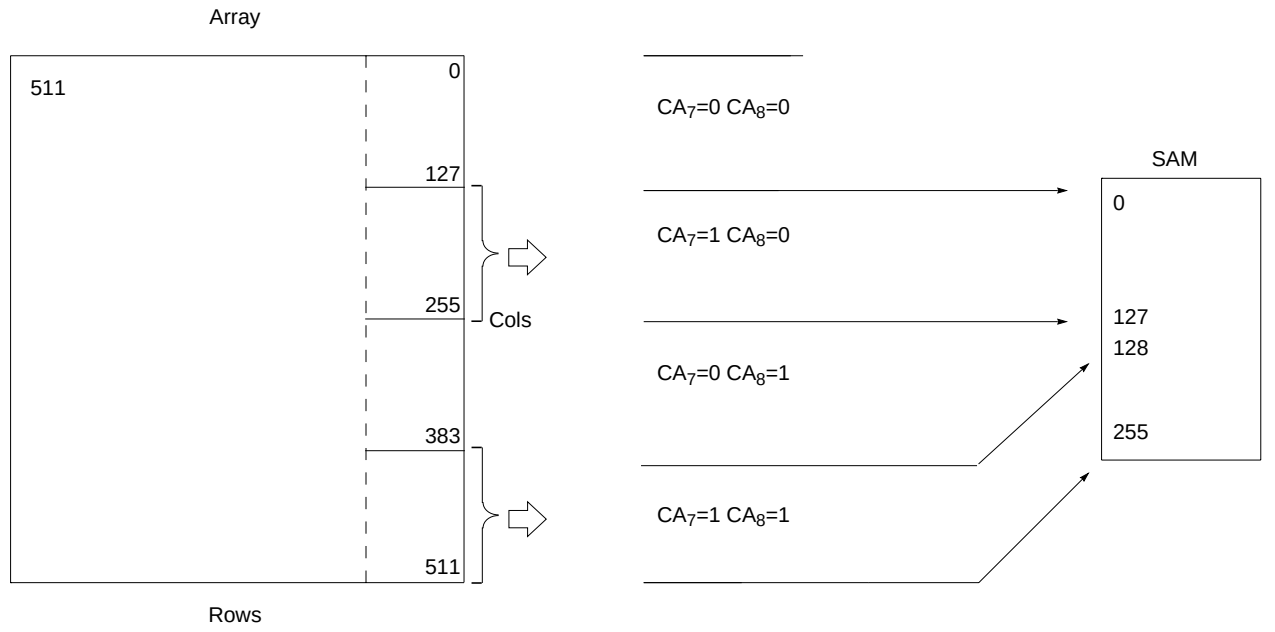
Note: ***If the Serial port counter is between 128 and 255, the STOP address is equal to 128 plus the number(s) specified in column 3 of the Stop Register Set table on page 57. When the counter reaches the STOP address, the counter is loaded with the TAP point register address that was saved during the Split Transfer cycle.***

For more details of the Stop Column control for the Serial Port, refer to the Application Note, “Read/Write Transfer Operation”. Another application of SRS mode is to make “Half Depth SAM” VRAM part compatible to “Full Depth SAM” VRAM parts. Full compatibility is provided between Half Depth SAM and Full Depth SAM by performing split transfer in SRS mode using STOP address of 127 or less. For more details, refer to Application Note, “Half SAM and Full SAM Compatibility”.

Full Register Read Transfer (SRS) Mode

A Full Read Transfer in SRS mode will transfer 256 x16 bits from the selected row based on CA_7 at $\overline{CE}$ fall time during the Full Read Transfer cycle. CA_8 is a don't care. If CA_7 is “0”, data from locations in the selected row having physical address CA_7 equal to “0” is transferred to SAM. If CA_7 is “1”, data from locations that have a physical address CA_7 equal to “1” is transferred to SAM. Note that the data corresponding to physical address CA_8 equal to “0” is associated with the lower half of SAM while the data corresponding to physical address CA_8 equal to “1" in a row is associated with the upper half of SAM. The timing diagram on page 58 illustrates a Full Read Transfer in SRS mode between DRAM and SAM.

Full Register Read Transfer (SRS) Mode

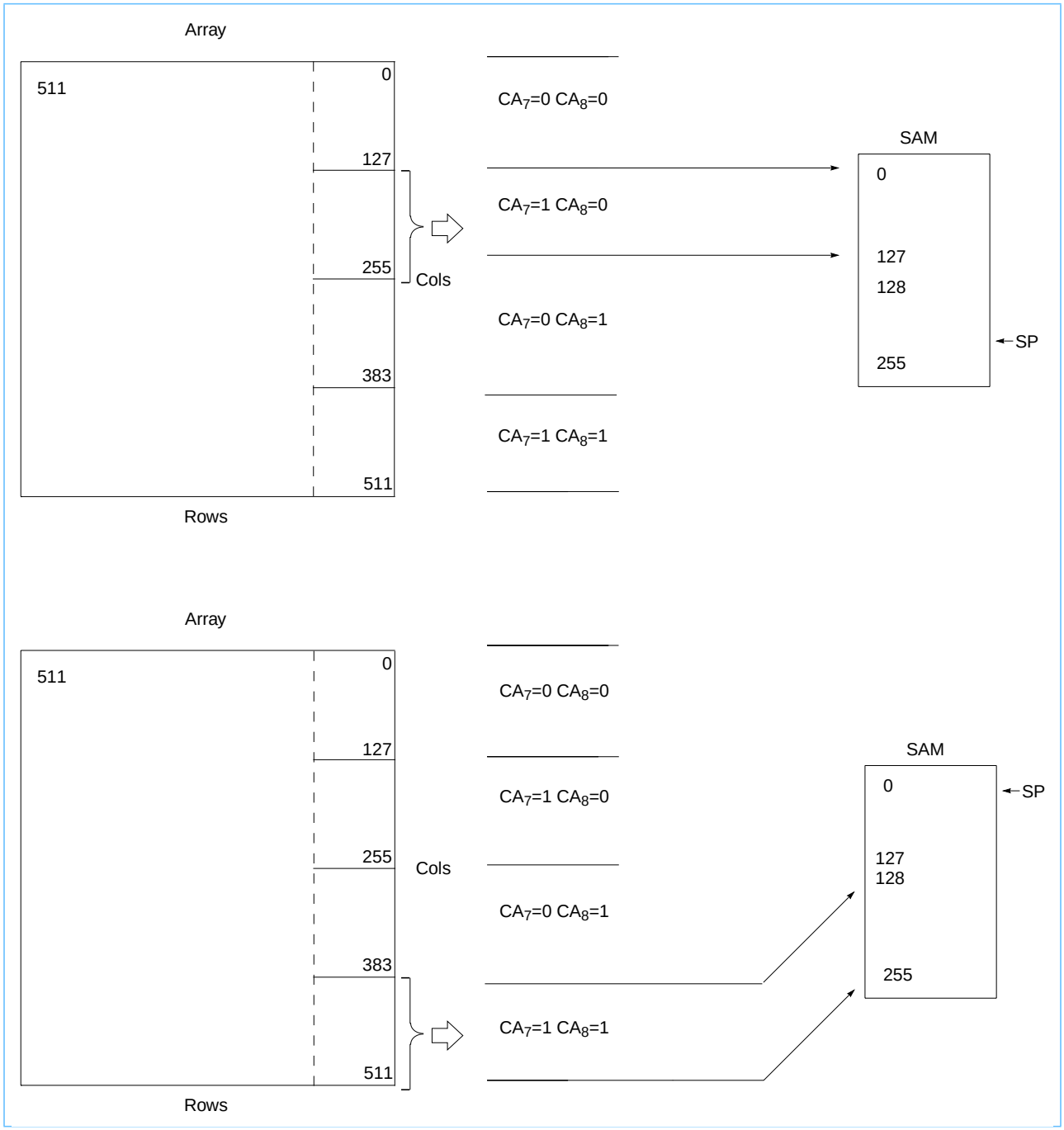


The example illustrates a full transfer in SRS mode based on CA_7=1.

Split Register Read Transfer (SRS) Mode

The Split Read Transfer in SRS mode is used to read data continuously from the Serial port without synchronizing the SC clock with the operation of the primary port. This mode is most useful for tiling applications. It is also used to make Half depth SAM VRAM parts compatible to Full depth SAM VRAM parts. When the Split Read Transfer in SRS mode is invoked, 128 x16 bits are transferred from a selected row based on user supplied column address "CA_7" at $\overline{CE}$ fall time and the Serial port counter reading. For example if the upper half of SAM is being read and user supplied CA_7 is "1", then the data having physical addresses "CA_7 =1 and CA_8 = 0" from the selected row is transferred to the lower half of SAM. If the lower half of SAM is being read and the user supplied column address CA_7 is "1", the data having physical addresses "CA_7 = 1 and CA_8 =1" from the selected row is transferred to the upper half of SAM. This is illustrated in the timing diagram on page 59. The user supplied column address "CA_6 - CA_0" is held in a TAP address register until the Serial port counter reaches the STOP address. At that point, the start address register is loaded with the contents of the TAP address register. The Serial port counter is updated with this address at the same time. The reading of data from the Serial port will commence from this address in the previously inactive half of SAM at the next SC clock.

Split Register Read Transfer (SRS) Mode

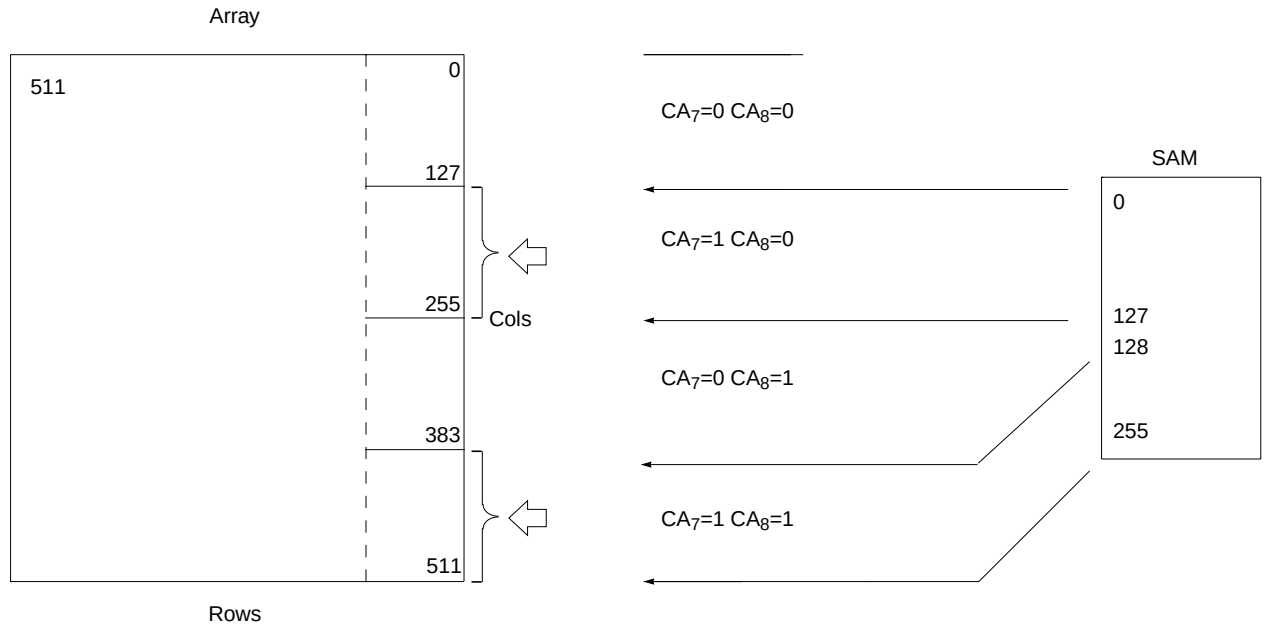


Write Transfer (SRS) Modes

Full Register Write Transfer (SRS) Mode

The Full Register Write Transfer operation in SRS mode is illustrated in the timing diagram on page 60. This operation will store the entire contents of the SAM in the row specified by row address (RA_8 - RA_0) at $\overline{RE}$ fall time and CA_7 at $\overline{CE}$ fall time during the Full Register Write Transfer cycle in SRS mode. CA_7 controls the transfer of data to the particular segments of the row. If CA_7 at $\overline{CE}$ fall time during a Full Register Transfer cycle is “1”, the data from SAM is stored in those segments of the row whose physical address bit “CA_7” equals to “1”. Data from the lower half of SAM is transferred to locations in the row that have physical address CA_8 equal to “0”, data from the upper half of SAM is transferred to locations in the row that have physical address CA_8 equal to “1”. CA_7-CA_0 address supplied by the user at $\overline{CE}$ fall time is loaded in the start address register to be used as starting location for writing the data in the Serial port on the next SC clock following the transfer. During the Full Register Write Transfer cycle, a WPBM can be loaded at $\overline{RE}$ fall time to mask the selected data bits at transfer time. ***Generally, it is a good practice to mask all the data bits at the first Full Register Write Transfer cycle to prevent writing of old data left over from previous Read Transfer operations.***

Full Register Write Transfer (SRS) Mode

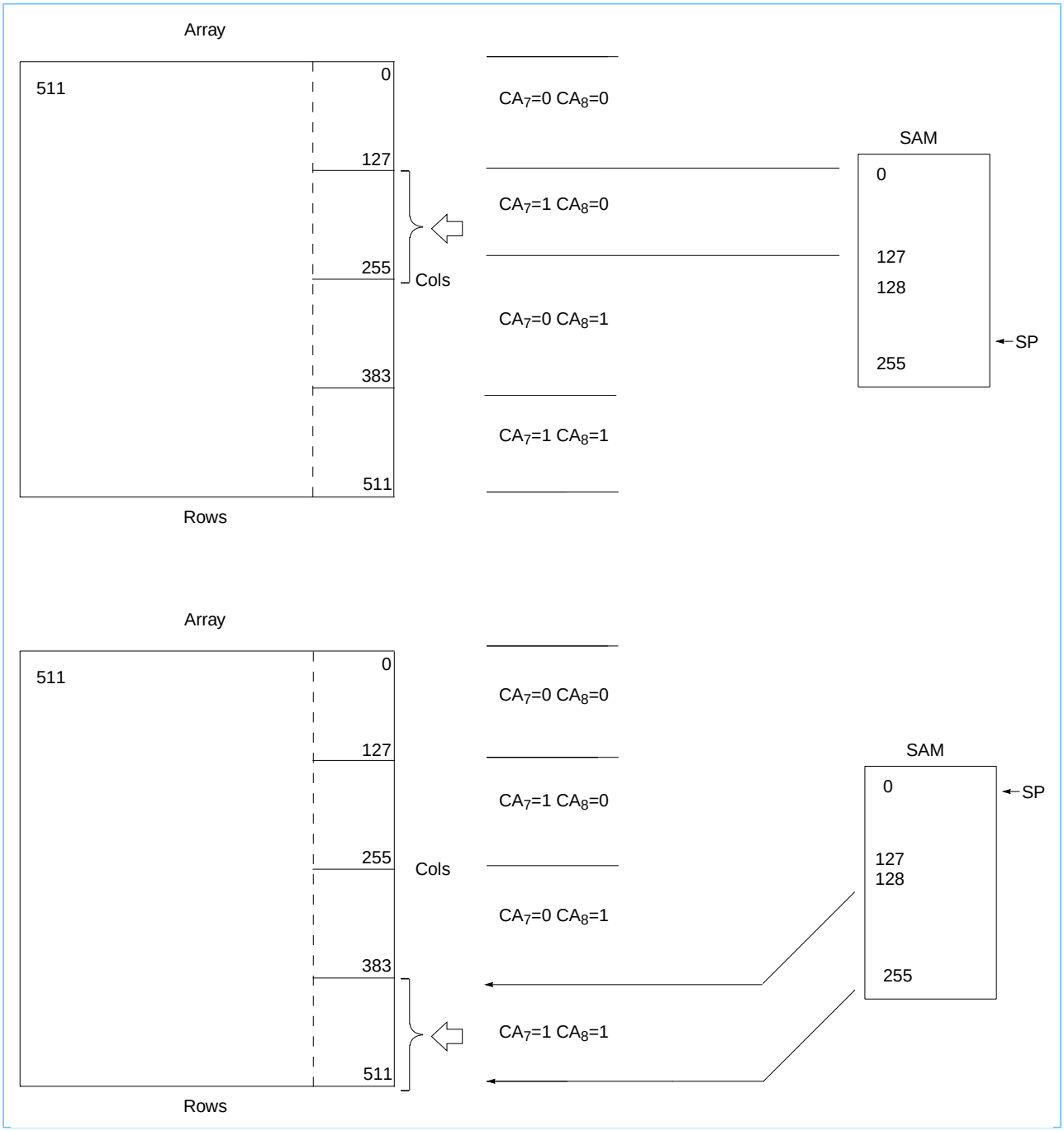


The example illustrates a full transfer in SRS mode based on CA_7=1.

Split Register Write Transfer (SRS) Mode

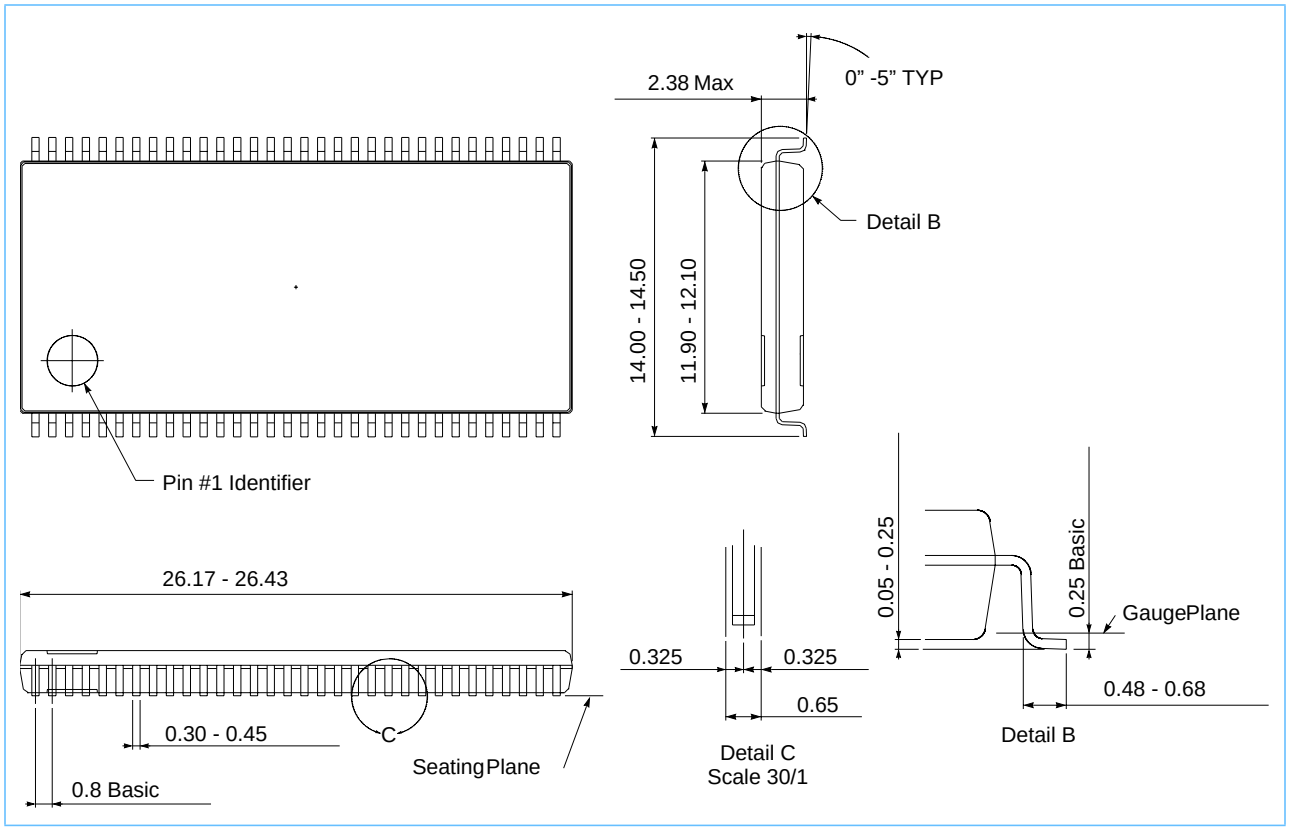
The Split Register Write Transfer is used to write data continuously in the Serial port. This transfer operation stores 128 x16 bits from SAM to the selected segment in a row specified by (RA_8 -RA_0) at $\overline{RE}$ fall time and CA_7 at $\overline{CE}$ fall time during the transfer cycle.The Serial port counter reading at the time of transfer determines the location of the segment in the selected row for the data transfer. The Split Register Write Transfer in SRS mode is illustrated in the timing diagram on page 62. The first example illustrates a Split Register Write Transfer between SAM and DRAM based on CA_7 and the status of which half of SAM is active and which half is inactive. In the example, user supplied address bit CA_7 is “1” and the upper half of SAM is active (data being written in that half) while the lower half of SAM is idling. Therefore, data from the lower half of SAM is forced to the upper quarter of the lower half of the selected row. ***Note that the data in the lower half of SAM is associated with row locations that have physical address bit CA_8 equal to “0”, while the data in the upper half of SAM is associated with the row locations that have physical address bit CA_8 equal to “1”***. The user supplied address bits CA_6 - CA_0 are stored in the TAP address register during the transfer cycle. When the Serial port counter reaches the STOP address, the start address is loaded with the contents of TAP address register. At the same time, the Serial port counter is updated with the new start address. The writing of data in the previously inactive half of SAM will start from this new start address at the next SC clock.

Split Register Write Transfer (SRS) Mode



Package Diagram

Dwg. SSOG (Dimensions in millimeters)



Revision Log

Rev	Contents of Modification
12/93	1. New mechanical drawings. 2. Description on how IBM's half depth SAM is compatible to a full depth SAM. 3. Another Pin Configuration diagram in the section title Module Pin Definitions.
2/94	1. Added note to Ordering Information section. 2. Remove t_{TRG} parameter from timing table and Read Cycle timing. 3. In extended data out diagram, the $\overline{W}$ is changed from HIGH to DON'T CARE at $\overline{RE}$ fall. 4. Changed DC currents for 5.0 V and 3.3 V. 5. Change SSOG size from .500" to .472" in Pin Configuration and Module Pin Definition.
9/94	Updated and added timing notes.
4/95	Major revision to update to Die Revision D preliminary specifications.
10/95	Die Rev 'D' specifications and update of timing diagrams.
3/98	Deleted QSF part numbers.

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