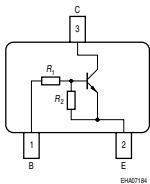


NPN Silicon Digital Transistor

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ($R_1 = 100k\Omega$, $R_2 = 100k\Omega$)



BCR101F/L3 BCR101T



Type	Marking	Pin Configuration						Package
BCR101F*	UCs	1=B	2=E	3=C	-	-	-	TSFP-3
BCR101L3*	UC	1=B	2=E	3=C	-	-	-	TSLP-3-4
BCR101T*	UCs	1=B	2=E	3=C	-	-	-	SC75

*Preliminary

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Emitter-base voltage	V_{EBO}	10	
Input on voltage	$V_{i(on)}$	50	
Collector current	I_C	50	mA
Total power dissipation- BCR101F, $T_S \leq 128^\circ\text{C}$ BCR101L3, $T_S \leq 135^\circ\text{C}$ BCR101T, $T_S \leq 109^\circ\text{C}$	P_{tot}	250 250 250	mW
Junction temperature	T_j	150	
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}		K/W
BCR101F		≤ 90	
BCR101L3		≤ 60	
BCR101T		≤ 165	

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}$, $I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}$, $I_E = 0$	$V_{(BR)CBO}$	50	-	-	
Collector-base cutoff current $V_{CB} = 40 \text{ V}$, $I_E = 0$	I_{CBO}	-	-	100	nA
Emitter-base cutoff current $V_{EB} = 10 \text{ V}$, $I_C = 0$	I_{EBO}	-	-	75	μA
DC current gain ²⁾ $I_C = 5 \text{ mA}$, $V_{CE} = 5 \text{ V}$	h_{FE}	70	-	-	-
Collector-emitter saturation voltage ²⁾ $I_C = 5 \text{ mA}$, $I_B = 0.25 \text{ mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}$, $V_{CE} = 5 \text{ V}$	$V_{i(off)}$	0.5	-	1.8	
Input on voltage $I_C = 1 \text{ mA}$, $V_{CE} = 0.3 \text{ V}$	$V_{i(on)}$	1	-	3	
Input resistor	R_1	70	100	130	k Ω
Resistor ratio	R_1/R_2	0.9	1	1.1	-

AC Characteristics

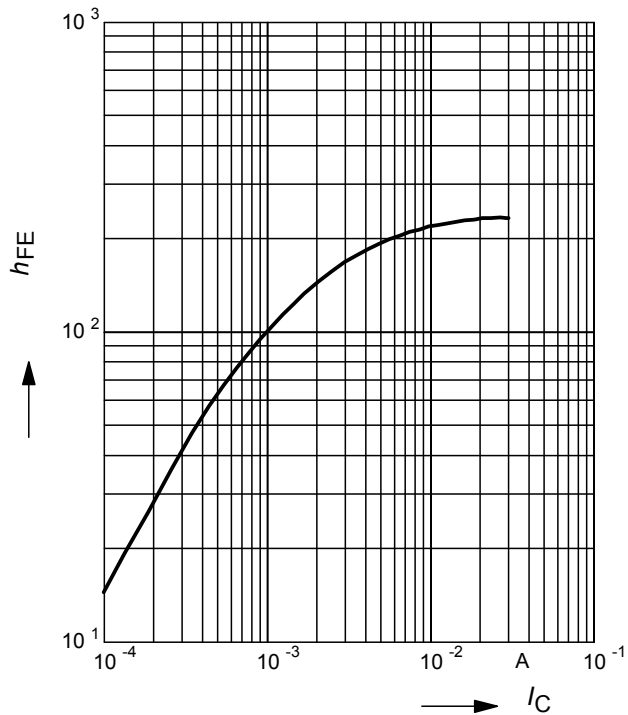
Transition frequency $I_C = 10 \text{ mA}$, $V_{CE} = 5 \text{ V}$, $f = 100 \text{ MHz}$	f_T	-	100	-	MHz
Collector-base capacitance $V_{CB} = 10 \text{ V}$, $f = 1 \text{ MHz}$	C_{cb}	-	3	-	pF

¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

²⁾Pulse test: $t < 300 \mu\text{s}$; $D < 2\%$

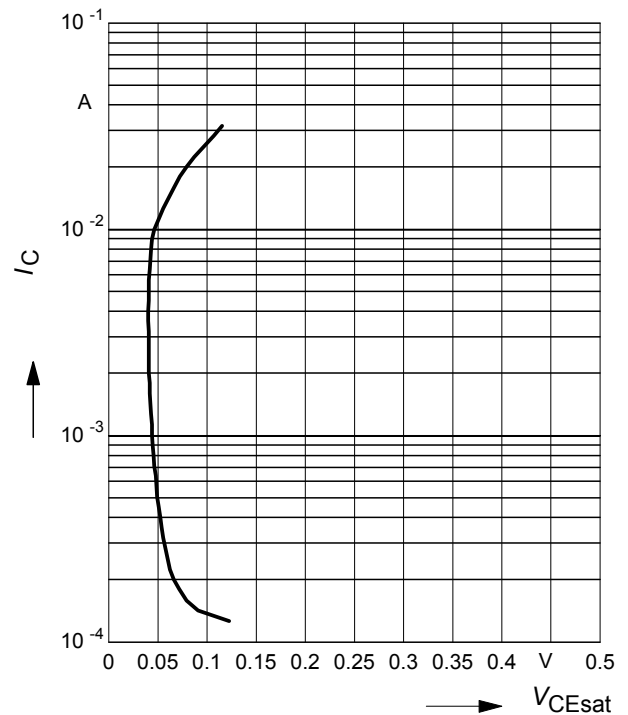
DC current gain $h_{FE} = f(I_C)$

$V_{CE} = 5\text{ V}$ (common emitter configuration)



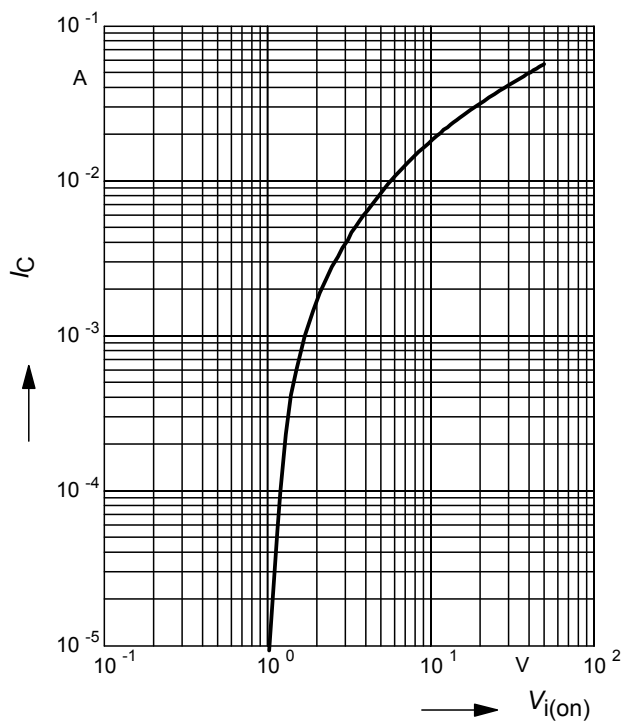
Collector-emitter saturation voltage

$V_{CEsat} = f(I_C), h_{FE} = 20$



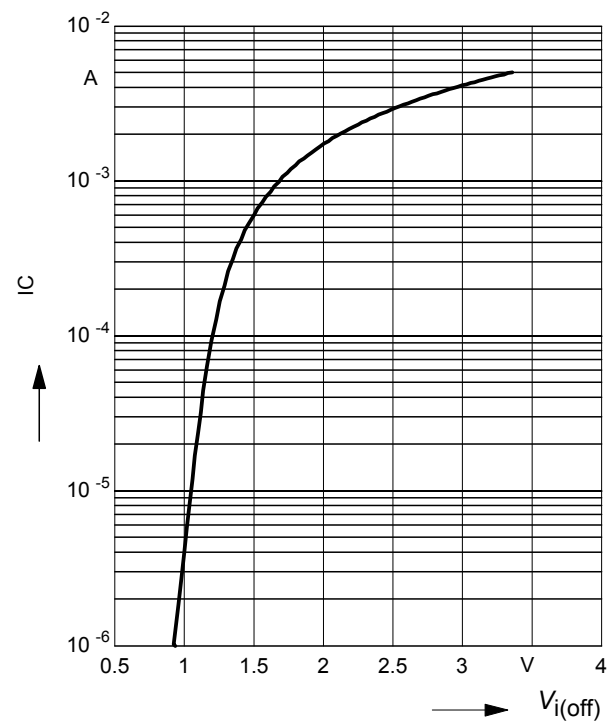
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3\text{ V}$ (common emitter configuration)



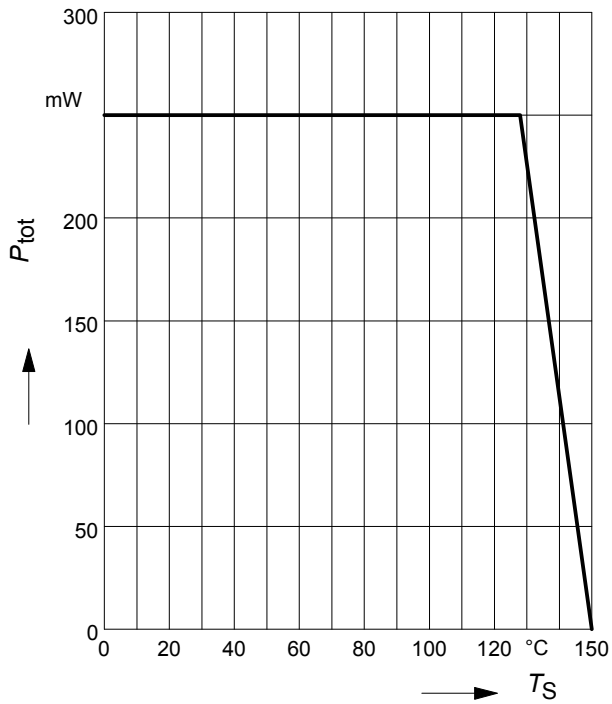
Input off voltage $V_{i(off)} = f(I_C)$

$V_{CE} = 5\text{ V}$ (common emitter configuration)



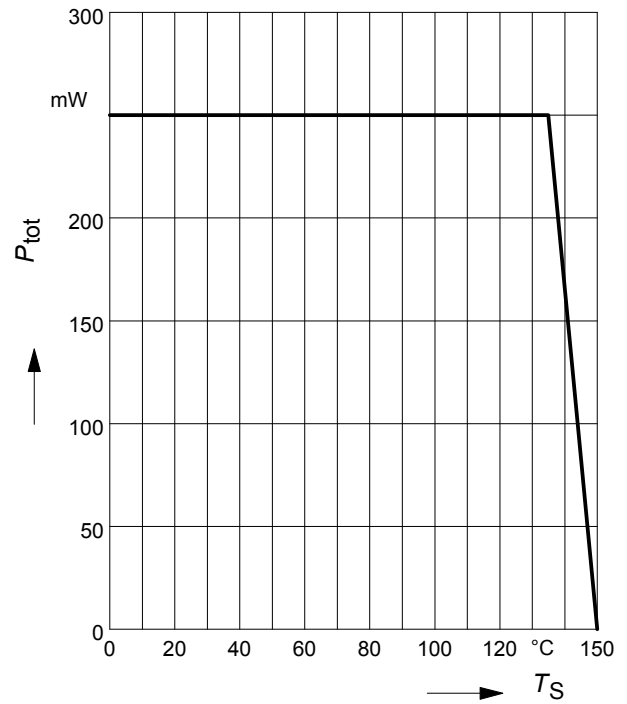
Total power dissipation $P_{\text{tot}} = f(T_S)$

BCR101F



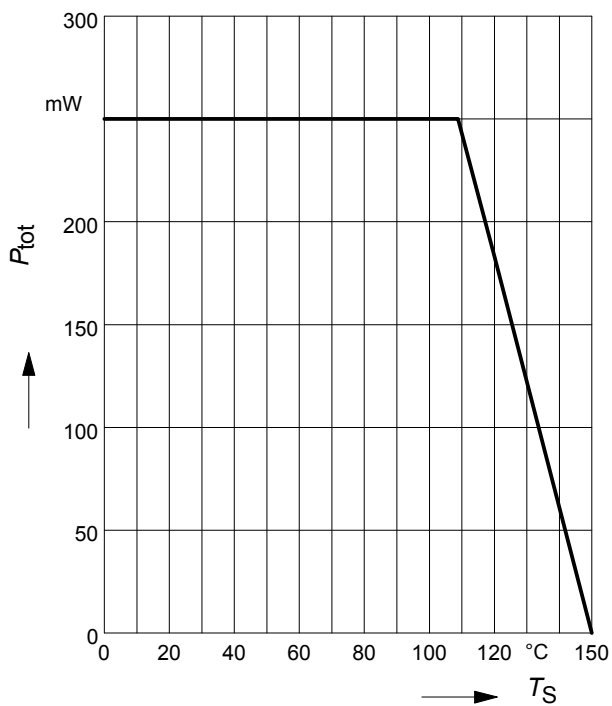
Total power dissipation $P_{\text{tot}} = f(T_S)$

BCR101L3



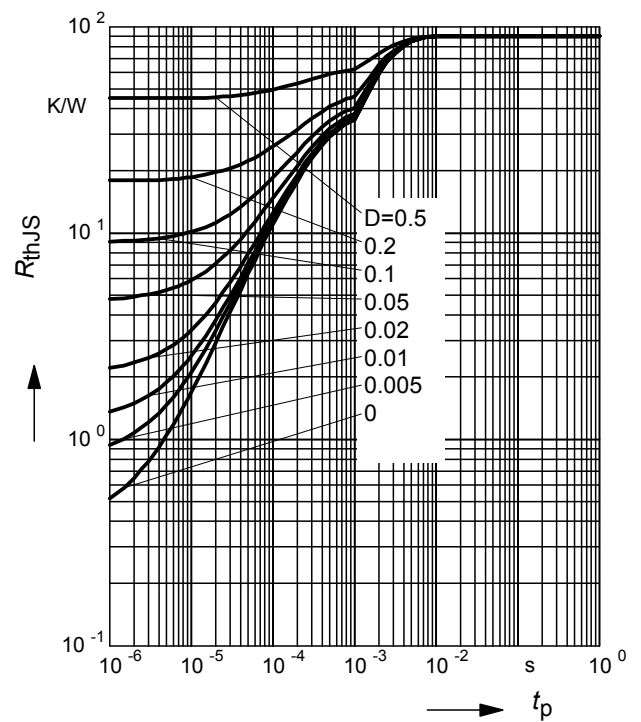
Total power dissipation $P_{\text{tot}} = f(T_S)$

BCR101T



Permissible Puls Load $R_{\text{thJS}} = f(t_p)$

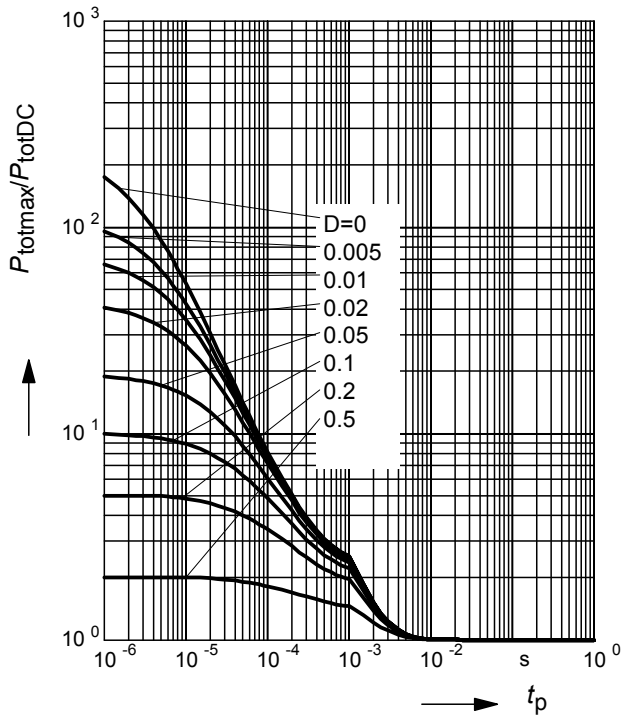
BCR101F



Permissible Pulse Load

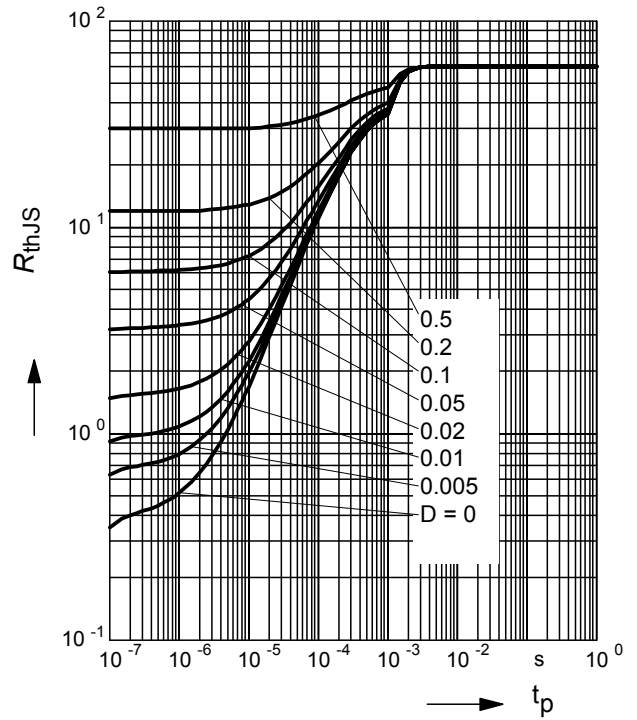
$$P_{\text{totmax}}/P_{\text{totDC}} = f(t_p)$$

BCR101F



Permissible Puls Load $R_{\text{thJS}} = f(t_p)$

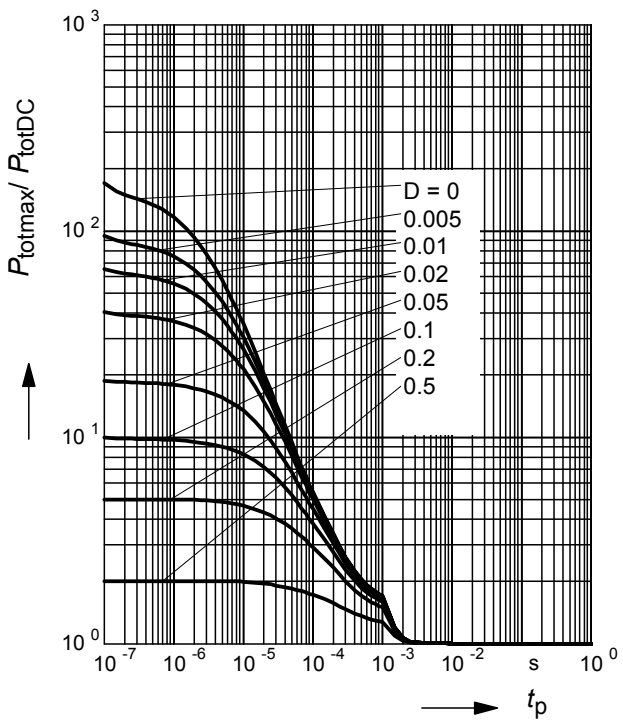
BCR101L3



Permissible Pulse Load

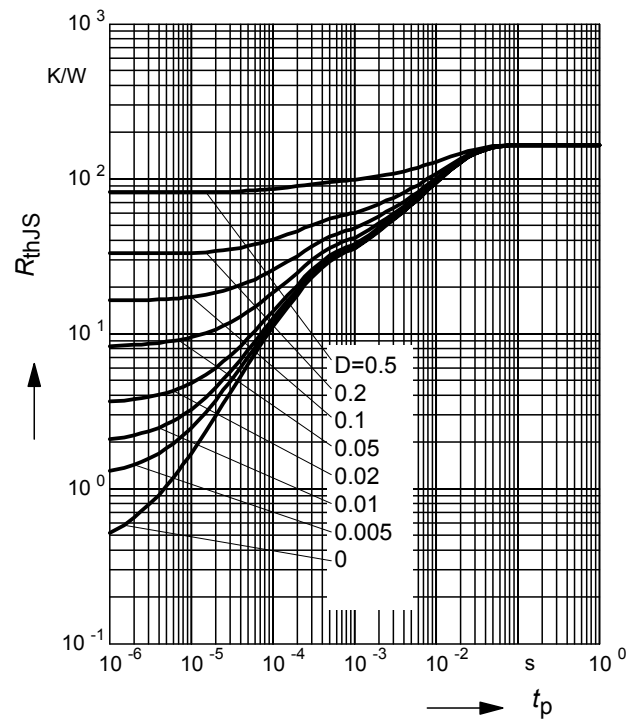
$$P_{\text{totmax}}/P_{\text{totDC}} = f(t_p)$$

BCR101L3



Permissible Puls Load $R_{\text{thJS}} = f(t_p)$

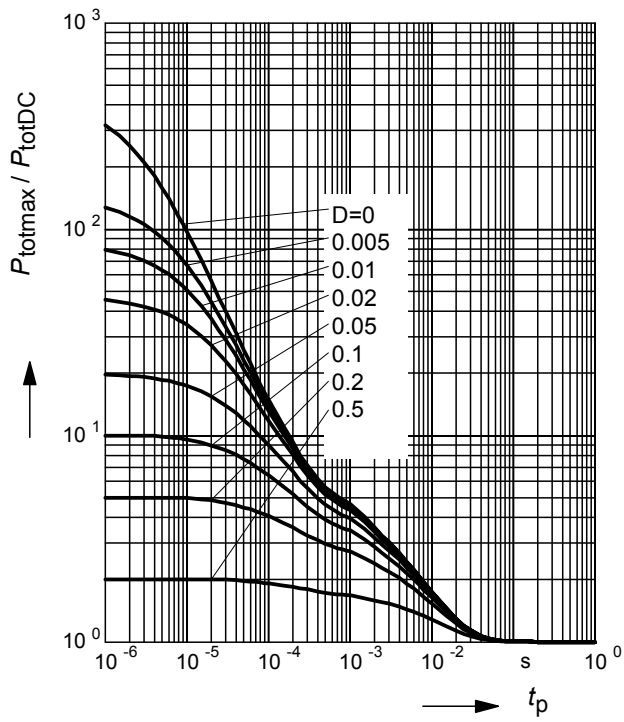
BCR101T



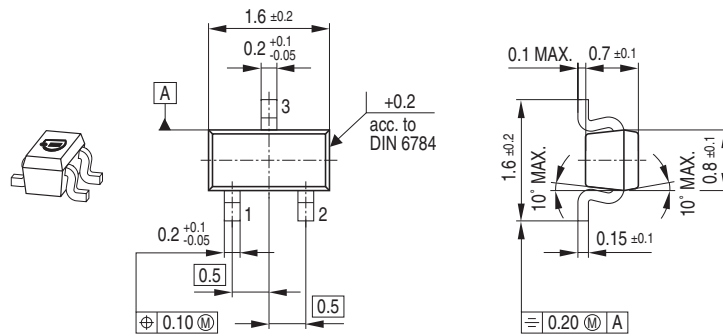
Permissible Pulse Load

$$P_{\text{totmax}}/P_{\text{totDC}} = f(t_p)$$

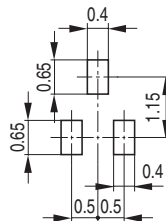
BCR101T



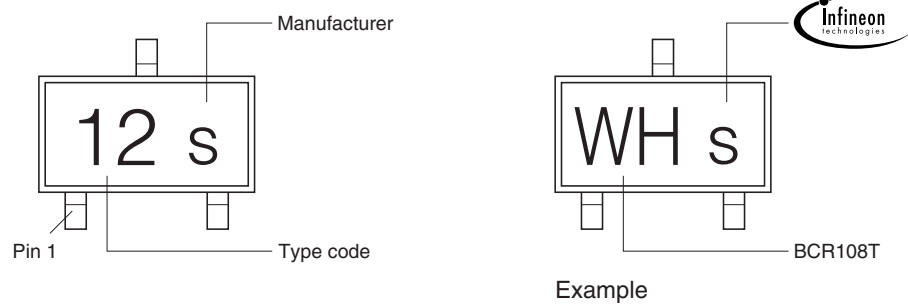
Package Outline



Foot Print

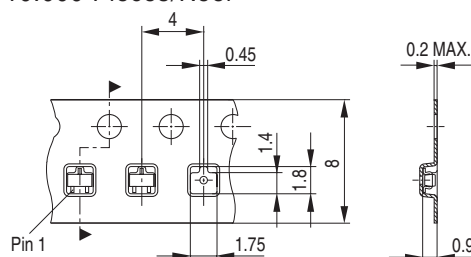


Marking Layout

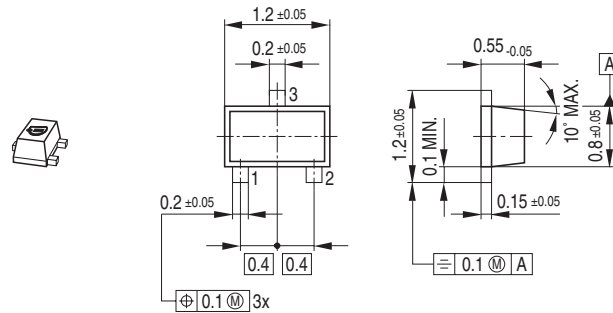


Packing

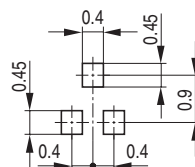
Code E6327: Reel ø180 mm = 3.000 Pieces/Reel
 Code E6433: Reel ø330 mm = 10.000 Pieces/Reel



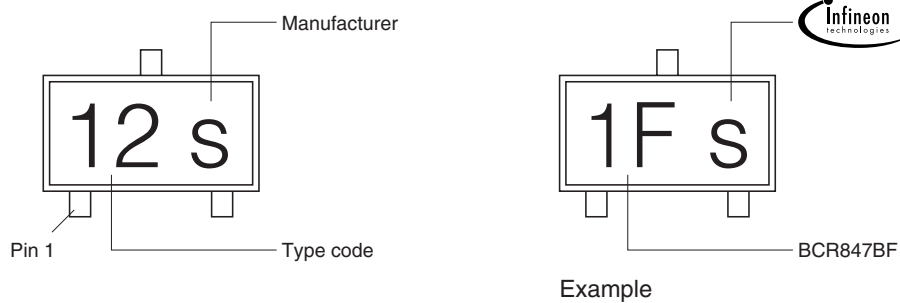
Package Outline



Foot Print

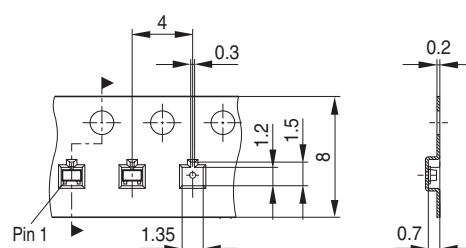


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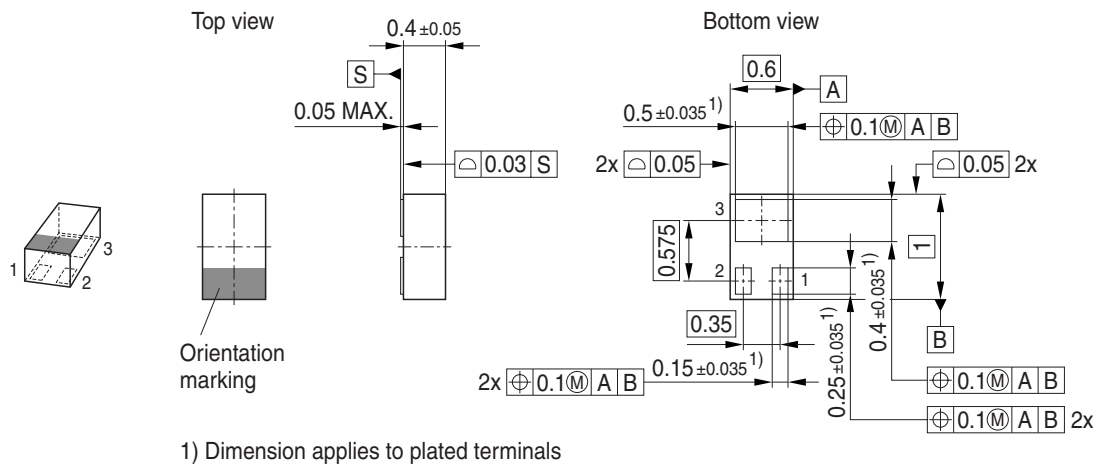


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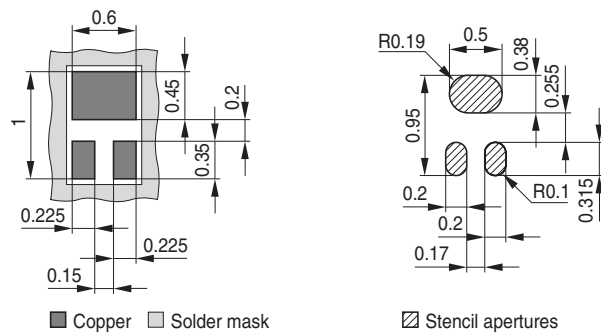
Code E6327: Reel ø180 mm = 3.000 Pieces/Reel
Code E6433: Reel ø330 mm = 10.000 Pieces/Reel



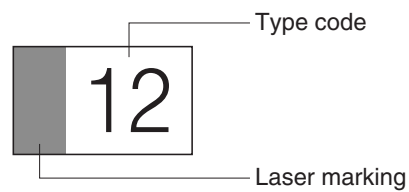
Package Outline



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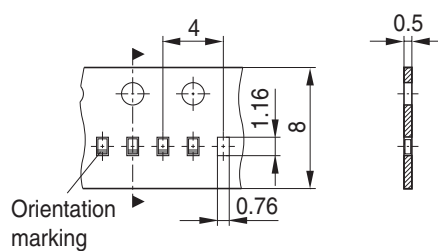


Marking Layout



Packing

Code E6327: Reel $\varnothing$ 180 mm = 15.000 Pieces/Reel



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