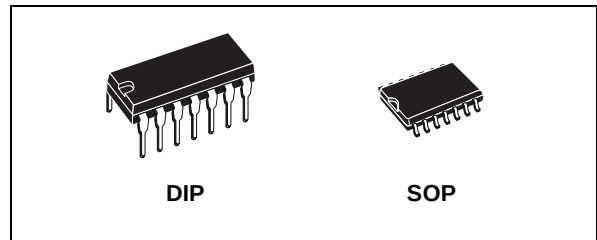


QUAD EXCLUSIVE-OR GATE

- MEDIUM SPEED OPERATION - $t_{pHL} = t_{pLH} = 65\text{ns}$ (TYP.) at $C_L = 50\text{pF}$ and $V_{DD} - V_{SS} = 10\text{V}$
- LOW OUTPUT IMPEDANCE : $500\ \Omega$ (TYP.) at $V_{DD} - V_{SS} = 10\text{V}$
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_I = 100\text{nA}$ (MAX) AT $V_{DD} = 18\text{V}$ $T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



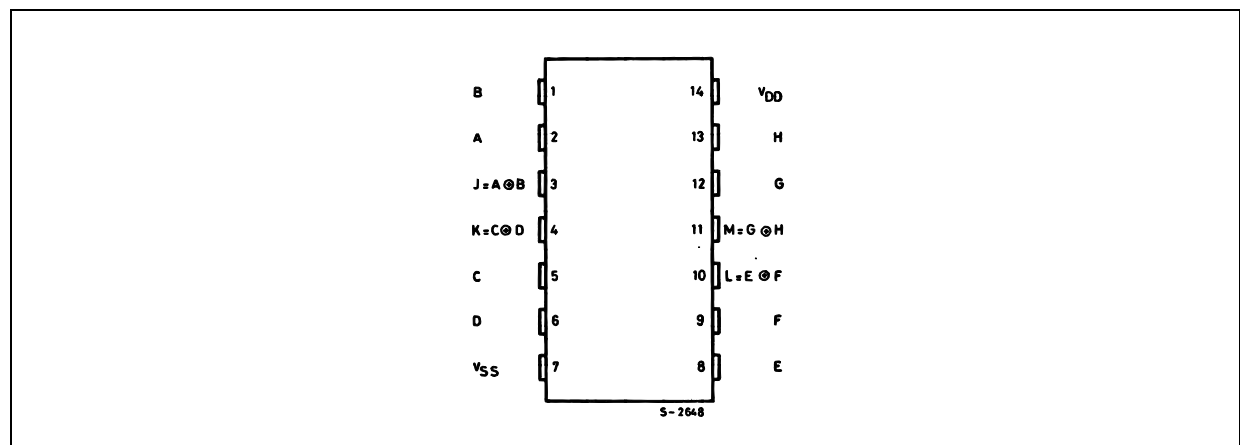
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4030BEY	
SOP	HCF4030BM1	HCF4030M013TR

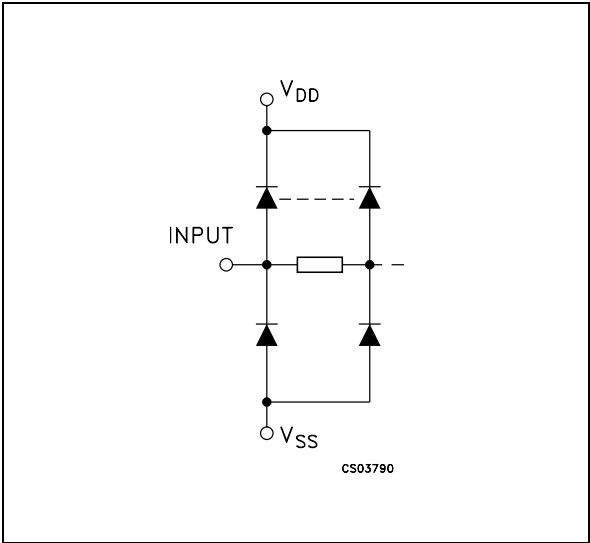
DESCRIPTION

HCF4030B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4030B types consist of four independent exclusive-OR gates integrated on a single monolithic silicon chip. Each exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



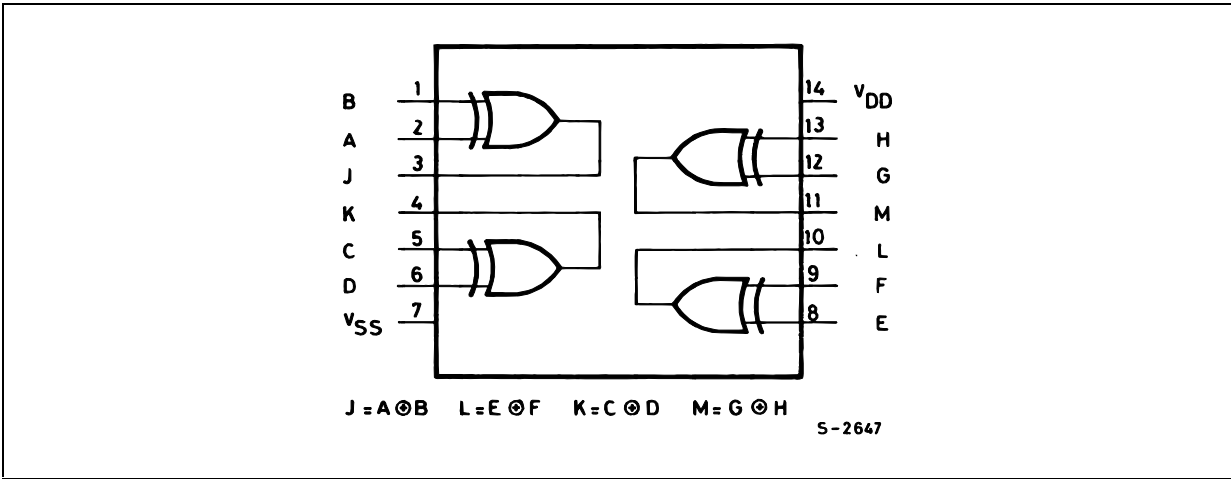
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 1, 5, 6, 8, 9, 12, 13	A, B, C, D, E, F, G, H	Data Inputs
3, 4, 10, 11	J, K, L, M	Data Outputs
7	V _{SS}	Negative Supply Voltage
14	V _{DD}	Positive Supply Voltage

TRUTH TABLE

IN1	IN2	OUT
L	L	L
L	H	H
H	L	H
H	H	L

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DD}	Supply Voltage	-0.5 to +22	V
V _I	DC Input Voltage	-0.5 to V _{DD} + 0.5	V
I _I	DC Input Current	± 10	mA
P _D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T _{op}	Operating Temperature	-55 to +125	°C
T _{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

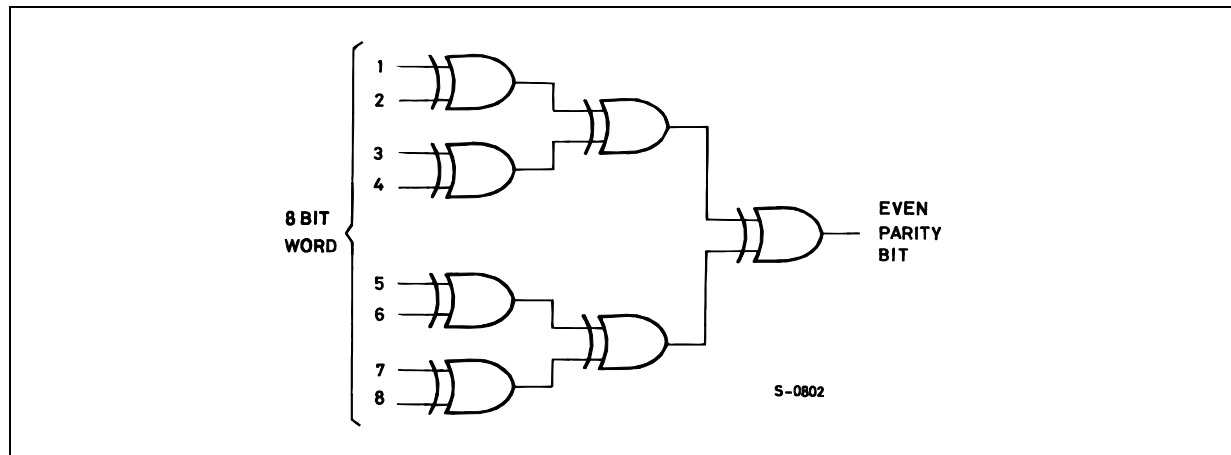
Symbol	Parameter	Test Condition				Value							Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent Current	0/5			5		0.02	4		4		30	μA
		0/10			10		0.02	8		8		60	
		0/15			15		0.02	16		16		120	
		0/20			20		0.04	20		20		600	
V _{OH}	Output High Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Output Low Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	Input High Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Input Low Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA
C _I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with $V_{DD}=5V$, 2V min. with $V_{DD}=10V$, 2.5V min. with $V_{DD}=15V$

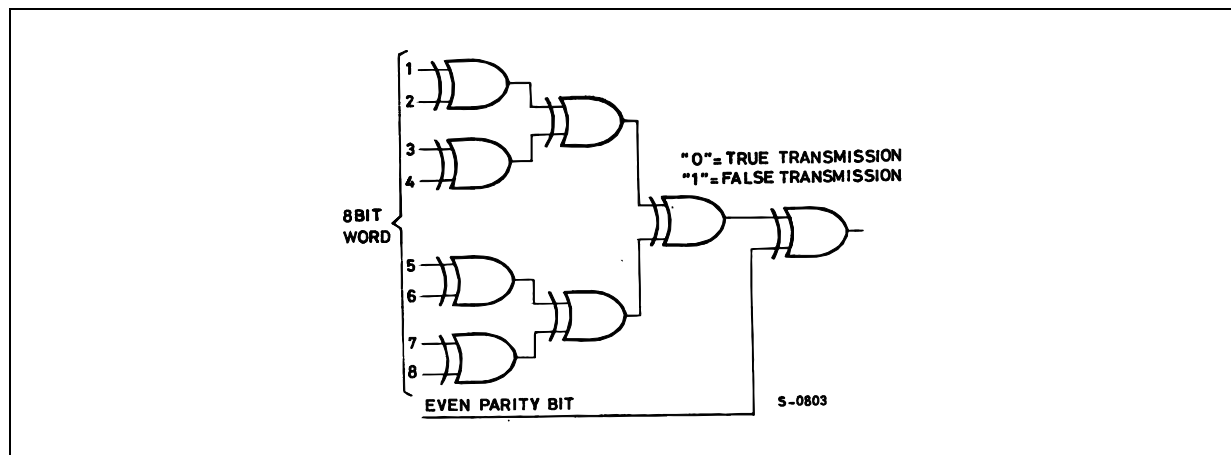
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$, $C_L = 50pF$, $R_L = 200K\Omega$, $t_r = t_f = 20 ns$)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time	5			140	280	ns
		10			65	130	
		15			50	100	
t_{TLH} t_{THL}	Output Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	

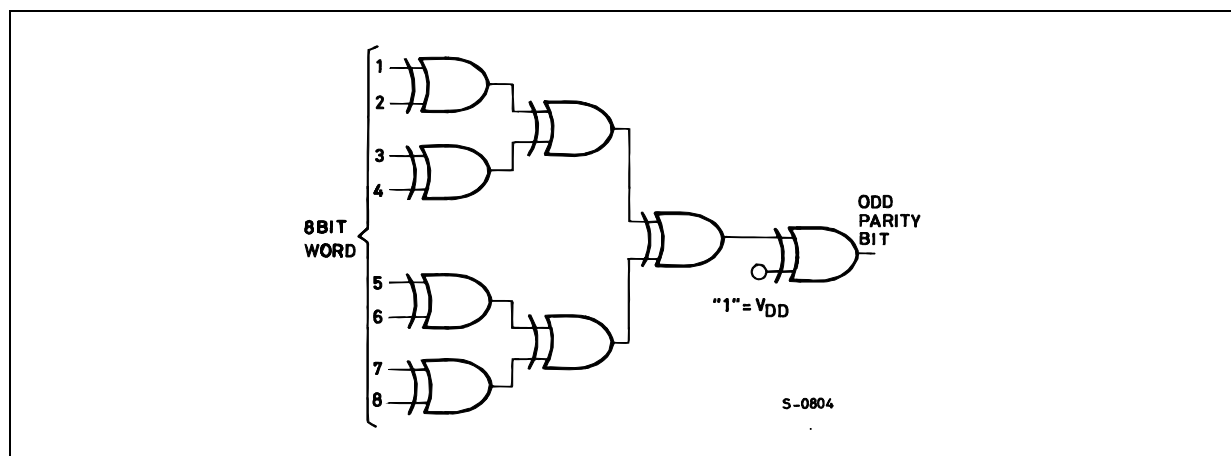
TYPICAL APPLICATION : EVEN PARITY-BIT GENERATOR



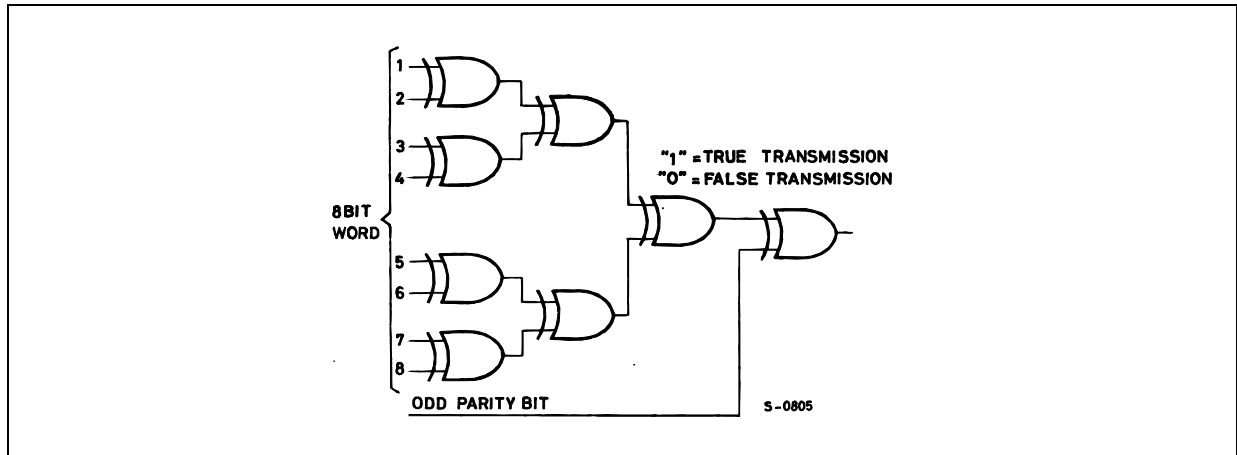
TYPICAL APPLICATION : EVEN PARITY-CHECKER



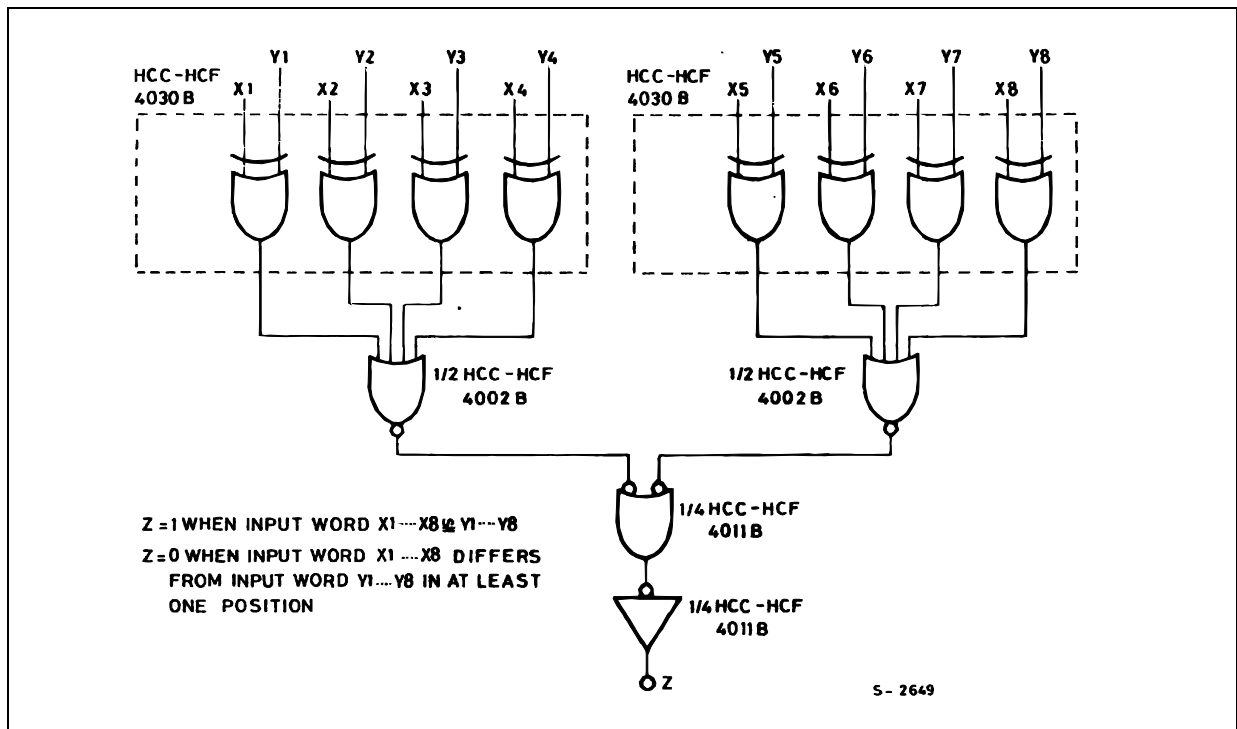
TYPICAL APPLICATION : ODD-PARITY-BIT GENERATOR

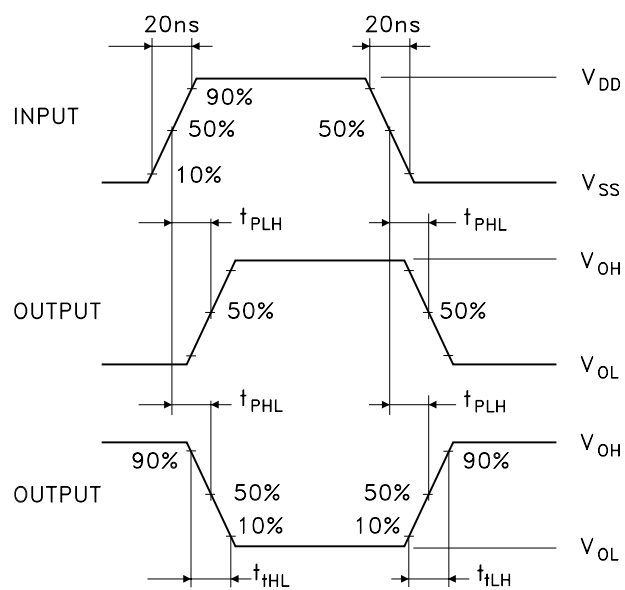


TYPICAL APPLICATION : ODD-PARITY-CHECKER



TYPICAL APPLICATION : 8-BIT COMPARATOR

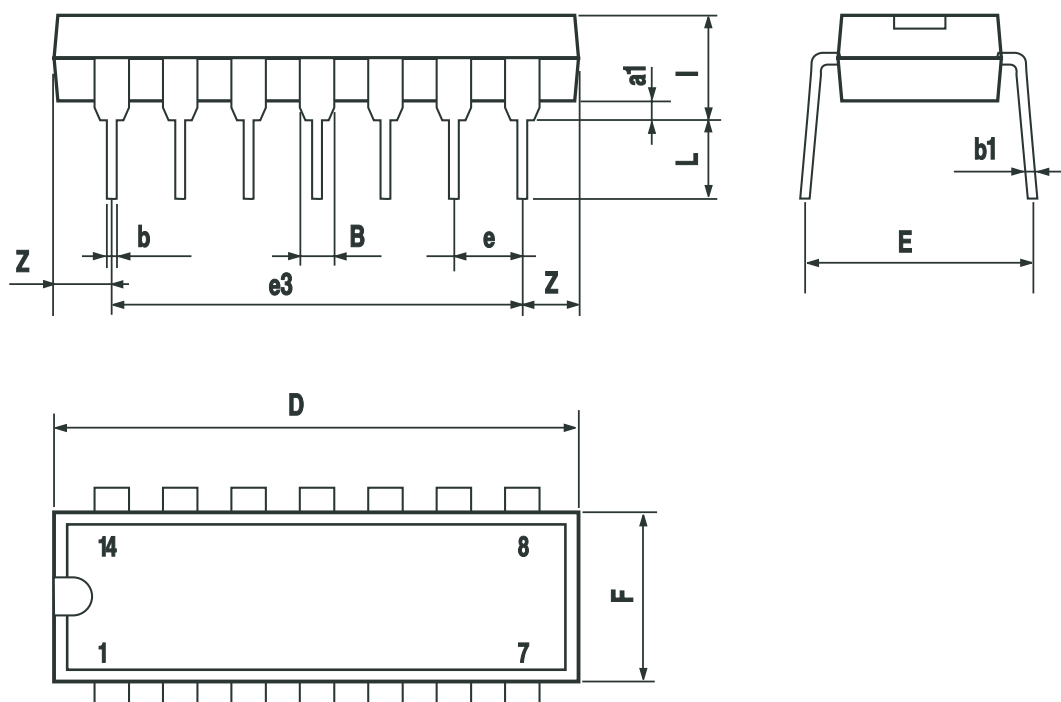


WAVEFORM : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)

CS08770

Plastic DIP-14 MECHANICAL DATA

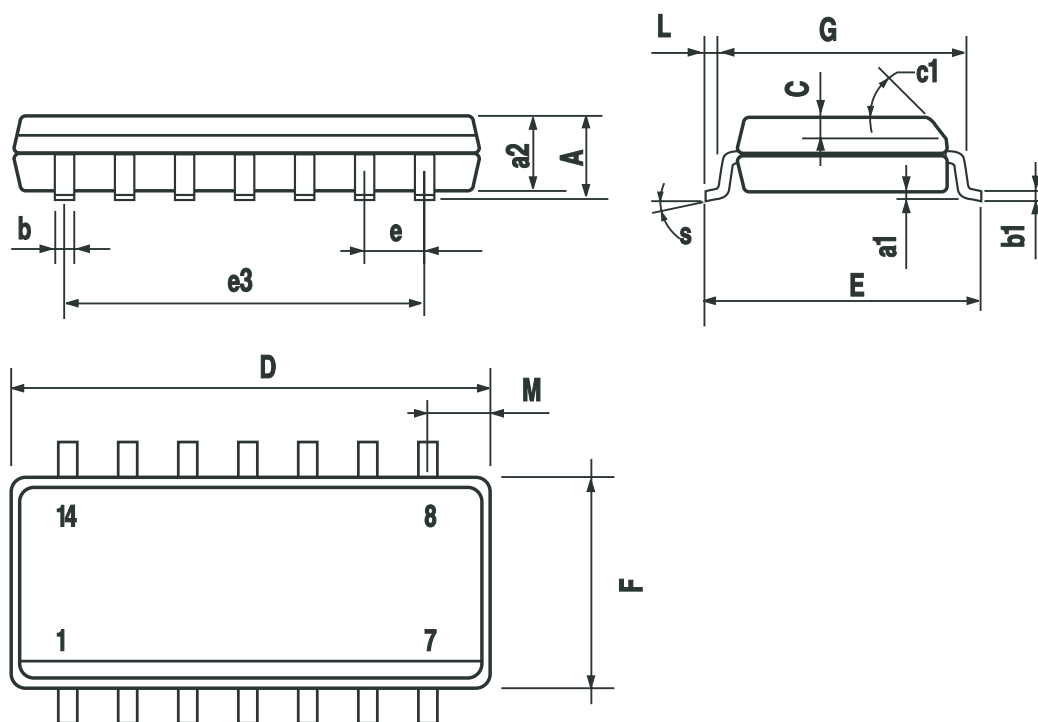
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>