16-Bit, Serial Input Multiplying Digital-to-Analog Converter

FEATURES

- **±0.5 LSB DNL**
- **16-Bit Monotonic**
- **±1 LSB INL**
- **Low Noise: 12 nV/√Hz**
- **Low Power: I_{DD} = 2 μA**
- **+2.7 V to +5.5 V Analog Power Supply**
- **2 mA Full-Scale Current ±20%, with V_{REF} = 10 V**
- **50-MHz Serial Interface**
- **0.5 μs Settling Time**
- **4-Quadrant Multiplying Reference**
- **Reference Bandwidth: 10 MHz**
- **±10 V Reference Input**
- **Reference Dynamics: -105 THD**
- **Tiny 8-Lead 3 x 3 mm SON and 3 x 5 mm MSOP Packages**
- **Industry-Standard Pin Configuration**

APPLICATIONS

- **Automatic Test Equipment**
- **Instrumentation**
- **Digitally Controlled Calibration**
- **Industrial Control PLCs**

DESCRIPTION

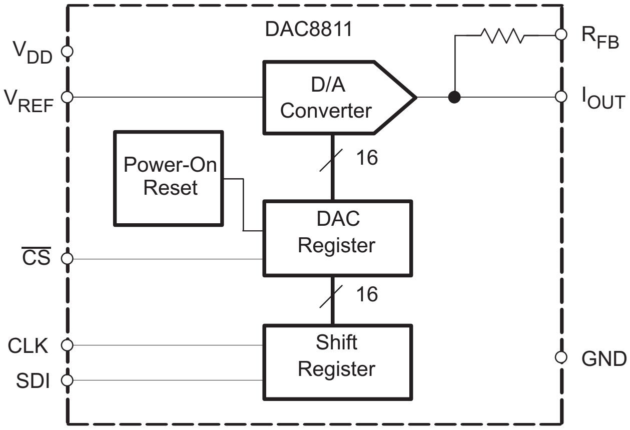
The DAC8811 multiplying digital-to-analog converter (DAC) is designed to operate from a single 2.7-V to 5.5-V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A serial data interface offers high-speed, three-wire microcontroller-compatible inputs using data-in (SDI), clock (CLK), and chip-select ($\overline{CS}$).

On power-up, the DAC register is filled with zeroes, and the DAC output is at zero scale.

The DAC8811 is packaged in space-saving 8-lead SON and MSOP packages.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8811C	±1	±1	MSOP-8 (DGK)	-40°C to 85°C	D11	DAC8811ICDGKT	Tape and Reel, 250
DAC8811C	±1	±1	MSOP-8 (DGK)	-40°C to 85°C	D11	DAC8811ICDGKR	Tape and Reel, 2500
DAC8811C	±1	±1	SON-8 (DRB)	-40°C to 85°C	D11	DAC8811ICDRBT	Tape and Reel, 250
DAC8811C	±1	±1	SON-8 (DRB)	-40°C to 85°C	D11	DAC8811ICDRBR	Tape and Reel, 2500
DAC8811B	±2	±1	MSOP-8 (DGK)	-40°C to 85°C	D11	DAC8811IBDGKT	Tape and Reel, 250
DAC8811B	±2	±1	MSOP-8 (DGK)	-40°C to 85°C	D11	DAC8811IBDGKR	Tape and Reel, 2500
DAC8811B	±2	±1	SON-8 (DRB)	-40°C to 85°C	D11	DAC8811IBDRBT	Tape and Reel, 250
DAC8811B	±2	±1	SON-8 (DRB)	-40°C to 85°C	D11	DAC8811IBDRBR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		DAC8811	UNIT
V_{DD} to GND		–0.3 to 7	V
Digital input voltage to GND		–0.3 to $+V_{DD}$ + 0.3	V
V (I_{OUT}) to GND		–0.3 to $+V_{DD}$ + 0.3	V
Operating temperature range		–40 to 105	°C
V_{REF}, R_{FB} to GND		–25 to 25	V
Storage temperature range		–65 to 150	°C
Junction temperature range (T_J max)		125	°C
Power dissipation		(T_J max – T_A) / $R_{\Theta JA}$	W
Thermal impedance, $R_{\Theta JA}$		55	°C/W
Lead temperature, soldering	Vapor phase (60s)	215	°C
Lead temperature, soldering	Infrared (15s)	220	°C
ESD rating, HBM		4000	V
ESD rating, CDM		1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; I_{OUT} = Virtual GND, GND = 0 V; V_{REF} = 10 V; T_A = full operating temperature. All specifications -40°C to 85°C, unless otherwise noted.

PARAMETER		CONDITIONS	DAC8811			UNITS
			MIN	TYP	MAX	
STATIC PERFORMANCE						
	Resolution		16			Bits
	Relative accuracy	DAC8811C			±1	LSB
	Relative accuracy	DAC8811B			±2	LSB
	Differential nonlinearity			±0.5	±1	LSB
	Output leakage current	Data = 0000h, T_A = 25°C			10	nA
	Output leakage current	Data = 0000h, $T_A = T_{MAX}$			10	nA
	Full-scale gain error	All ones loaded to DAC register		±1	±4	mV
	Full-scale tempco			±3		ppm/°C
OUTPUT CHARACTERISTICS(1)						
	Output current			2		mA
	Output capacitance	Code dependent		50		pF
REFERENCE INPUT(1)						
	V_{REF} Range		–15		15	V
	Input resistance			5		kΩ
	Input capacitance			5		pF
LOGIC INPUTS AND OUTPUT(1)						
V_{IL}	Input low voltage	V_{DD} = 2.7V			0.6	V
		V_{DD} = 5V			0.8	V
V_{IH}	Input high voltage	V_{DD} = 2.7V	2.1			V
		V_{DD} = 5V	2.4			V
I_{IL}	Input leakage current				10	µA
C_{IL}	Input capacitance				10	pF
INTERFACE TIMING						
f_{CLK}	Clock input frequency				50	MHz
$t_{(CH)}$	Clock pulse width high		10			ns
$t_{(CL)}$	Clock pulse width low		10			ns
$t_{(CSS)}$	$\overline{CS}$ to Clock setup time		0			ns
$t_{(CSH)}$	Clock to $\overline{CS}$ hold time		10			ns
$t_{(DS)}$	Data setup time		5			ns
$t_{(DH)}$	Data hold time		10			ns
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
	I_{DD} (normal operation)	Logic inputs = 0 V			5	µA
	V_{DD} = 4.5 V to 5.5 V	$V_{IH} = V_{DD}$ and V_{IL} = GND		3	5	µA
	V_{DD} = 2.7 V to 3.6 V	$V_{IH} = V_{DD}$ and V_{IL} = GND		1	2.5	µA
AC CHARACTERISTICS(1)(2)						
t_s	Output voltage settling time	To ±0.1% of full-scale, Data = 0000h to FFFFh to 0000h		0.3		µs
		To ±0.0015% of full-scale, Data = 0000h to FFFFh to 0000h		0.5		
BW –3 dB	Reference mutiplying BW	V_{REF} = 5 V_{PP}, Data = FFFFh		10		MHz
	DAC glitch impulse	V_{REF} = 0 V to 10 V, Data = 7FFFh to 8000h to 7FFFh		2		nV/s
	Feedthrough error V_{OUT}/V_{REF}	Data = 0000h, V_{REF} = 100 mV_{RMS}, f = 100kHz		–70		dB

(1) Specified by design and characterization; not production tested.

(2) All ac characteristic tests are performed in a closed-loop system using the THS4011 I-to-V converter amplifier.

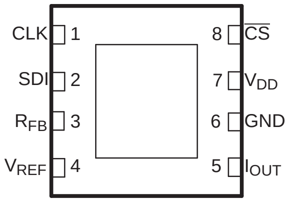
ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7 V to 5.5 V; I_{OUT} = Virtual GND, GND = 0 V; V_{REF} = 10 V; T_A = full operating temperature. All specifications -40°C to 85°C, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8811			UNITS
		MIN	TYP	MAX	
Digital feedthrough	$\overline{CS}$ = 1 and f_{CLK} = 1 MHz		2		nV/s
Total harmonic distortion	V_{REF} = 5 V_{PP}, Data = FFFFh, f = 1 kHz		–105		dB
Output spot noise voltage	f = 1 kHz, BW = 1 Hz		12		$nV/\sqrt{Hz}$

PIN ASSIGNMENTS

DRB PACKAGE
(TOP VIEW)



DGK PACKAGE
(TOP VIEW)

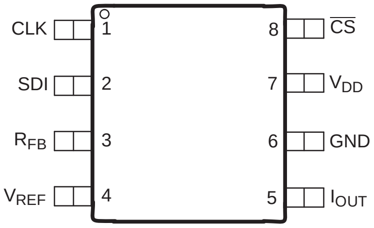


Table 1. TERMINAL FUNCTIONS

PIN	NAME	DESCRIPTION
1	CLK	Clock input; positive edge triggered clocks data into shift register
2	SDI	Serial register input; data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	R_{FB}	Internal matching feedback resistor. Connect to external op amp output.
4	V_{REF}	DAC reference input pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
5	I_{OUT}	DAC current output. Connects to inverting terminal of external precision I/V op amp.
6	GND	Analog and digital ground.
7	V_{DD}	Positive power supply input. Specified operating range of 2.7 V to 5.5 V.
8	$\overline{CS}$	Chip-select; active low digital input. Transfers shift register data to DAC register on rising edge. See Table 2 for operation.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

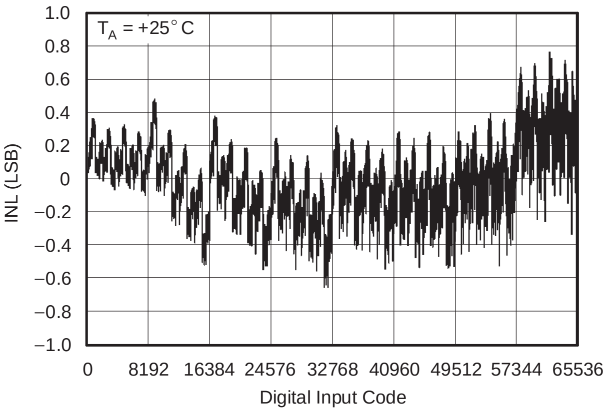


Figure 1.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

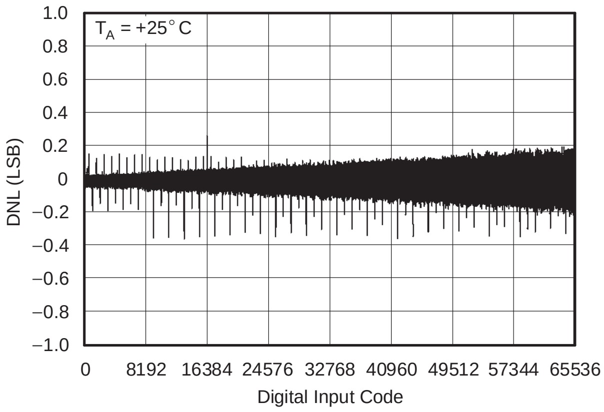


Figure 2.

LINEARITY ERROR vs DIGITAL INPUT CODE

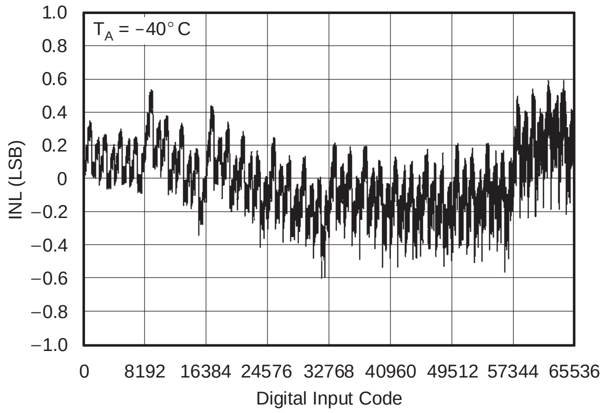


Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

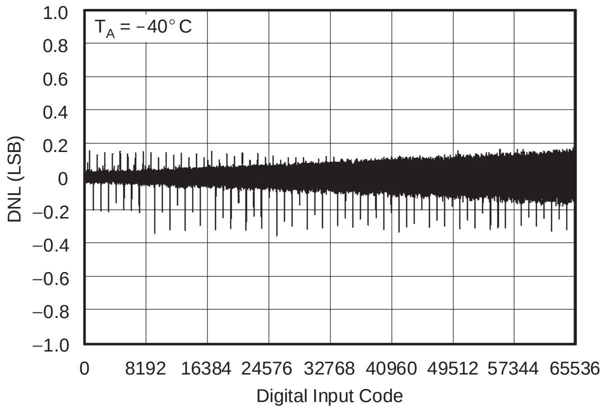


Figure 4.

LINEARITY ERROR vs DIGITAL INPUT CODE

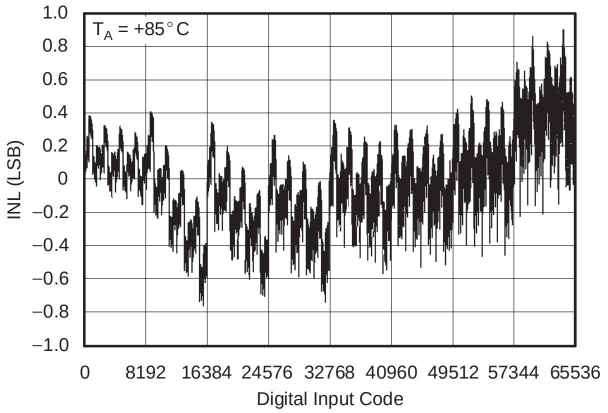


Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

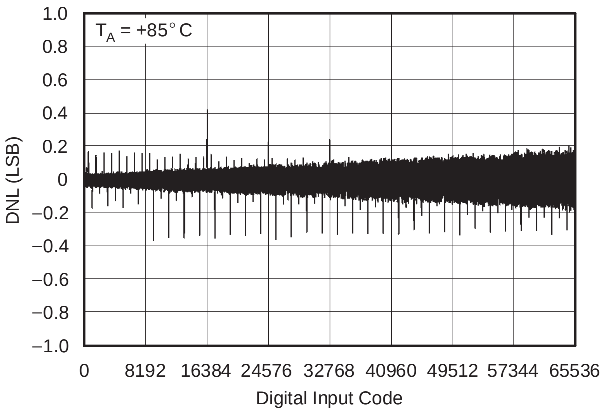


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

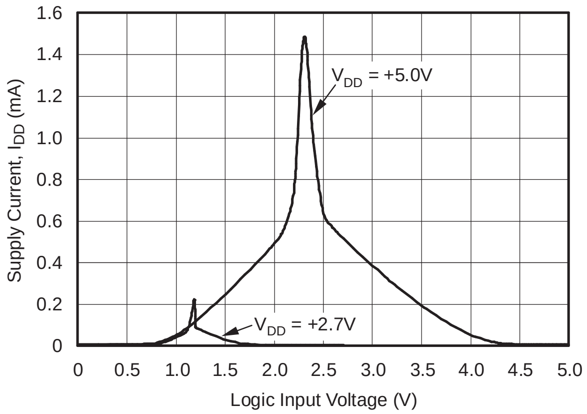


Figure 7.

REFERENCE MULTIPLYING BANDWIDTH

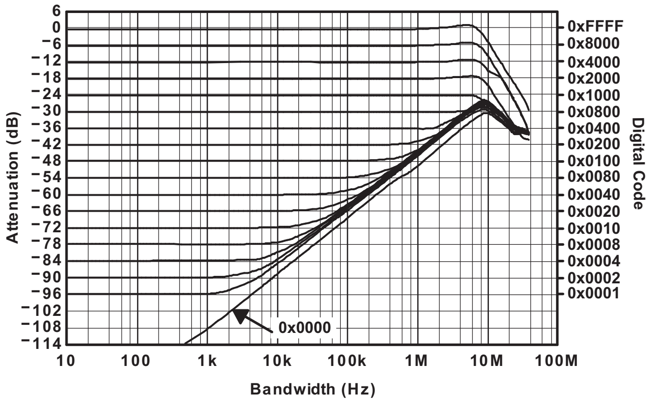


Figure 8.

DAC GLITCH

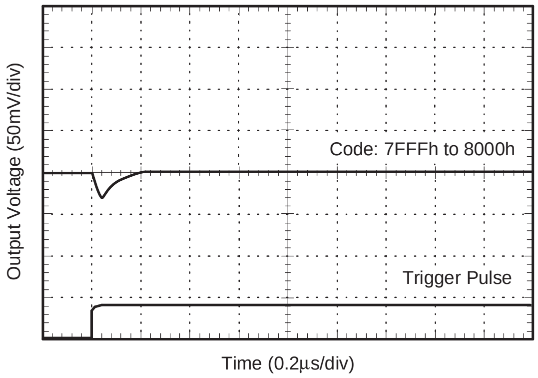


Figure 9.

DAC SETTLING TIME

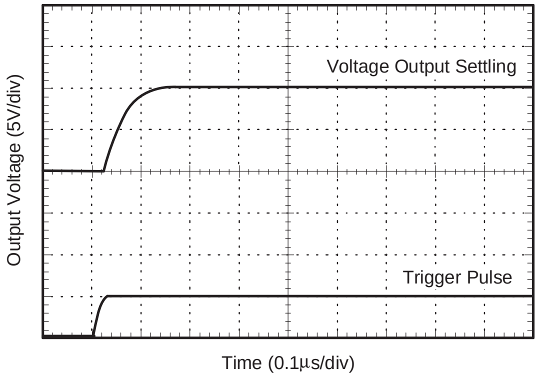


Figure 10.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V

At T_A = 25°C, $+V_{DD}$ = 2.7 V, unless otherwise noted.

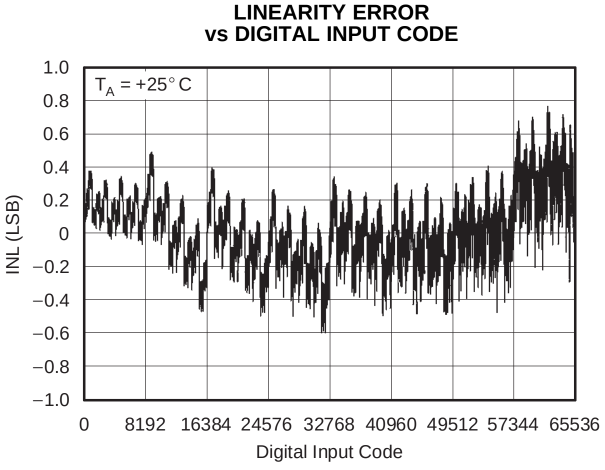


Figure 11.

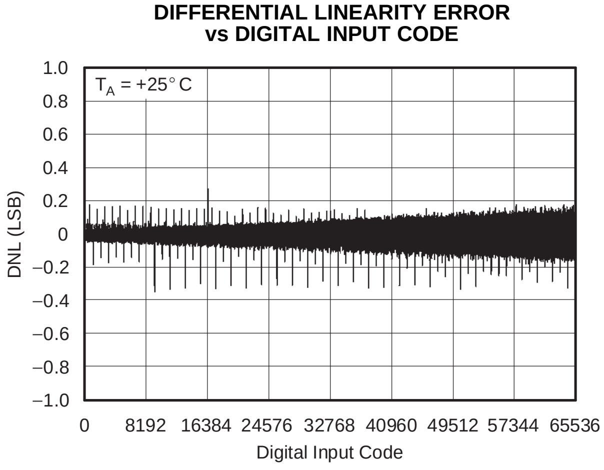


Figure 12.

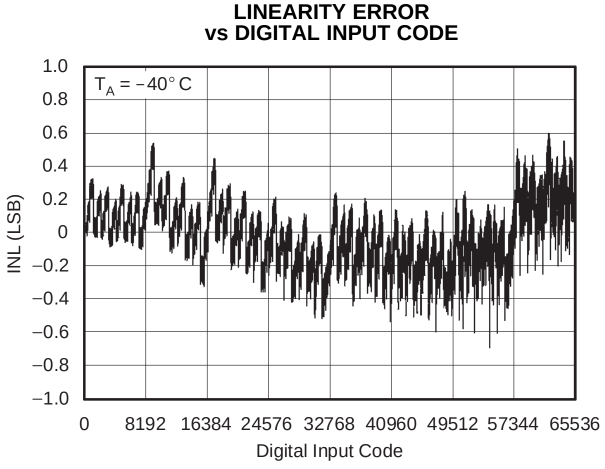


Figure 13.

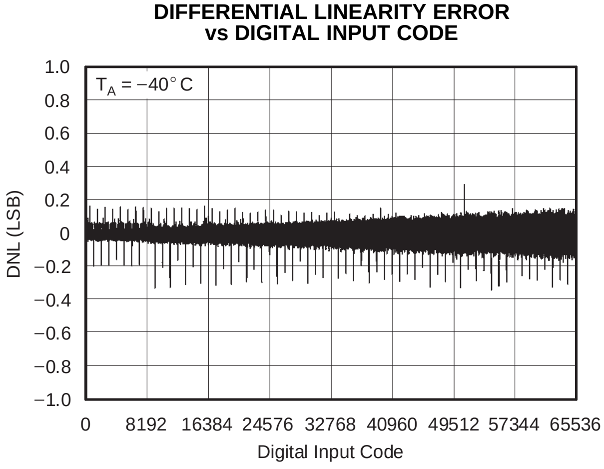


Figure 14.

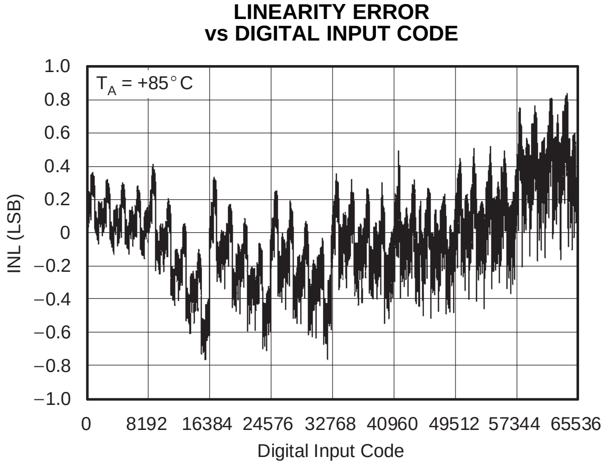


Figure 15.

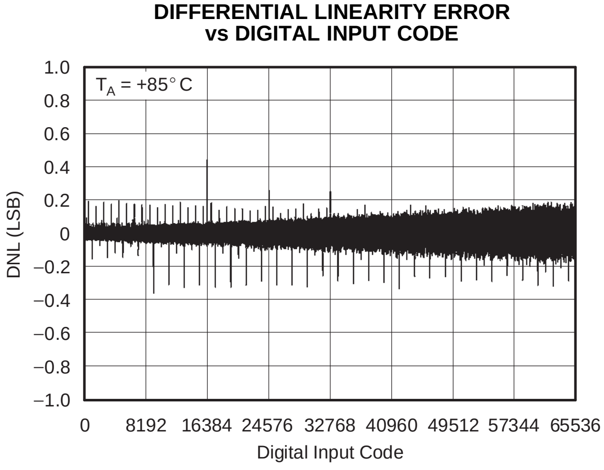


Figure 16.

THEORY OF OPERATION

The DAC8811 is a single channel current output, 16-bit digital-to-analog converter (DAC). The architecture, illustrated in Figure 17, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 5 kΩ ±25%. The external reference voltage can vary in a range of -15 V to 15 V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC8811 R_{FB} resistor, output voltage ranges of $-V_{REF}$ to V_{REF} can be generated.

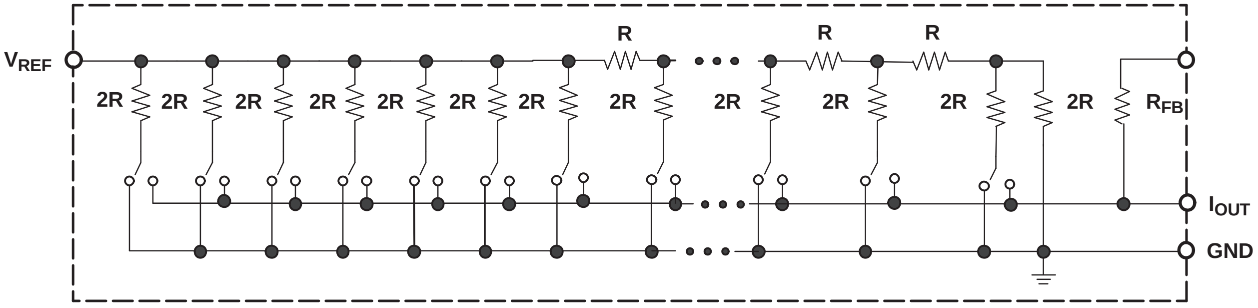


Figure 17. Equivalent R-2R DAC Circuit

When using an external I/V converter and the DAC8811 R_{FB} resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{CODE}{65536} \tag{1}$$

Each DAC code determines the 2R leg switch position to either GND or I_{OUT}. Because the DAC output impedance as seen looking into the I_{OUT} terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8811 due to offset modulation versus DAC code. For best linearity performance of the DAC8811, an op amp (OPA277) is recommended (Figure 18). This circuit allows V_{REF} swinging from -10 V to +10 V.

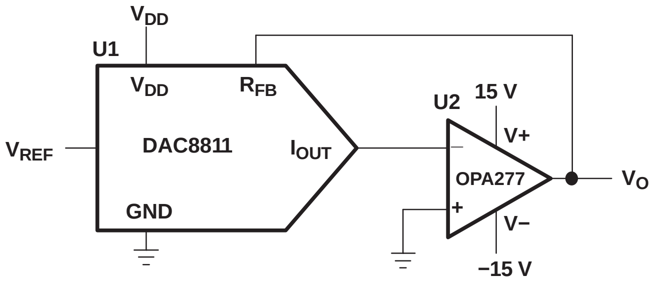


Figure 18. Voltage Output Configuration

THEORY OF OPERATION (continued)

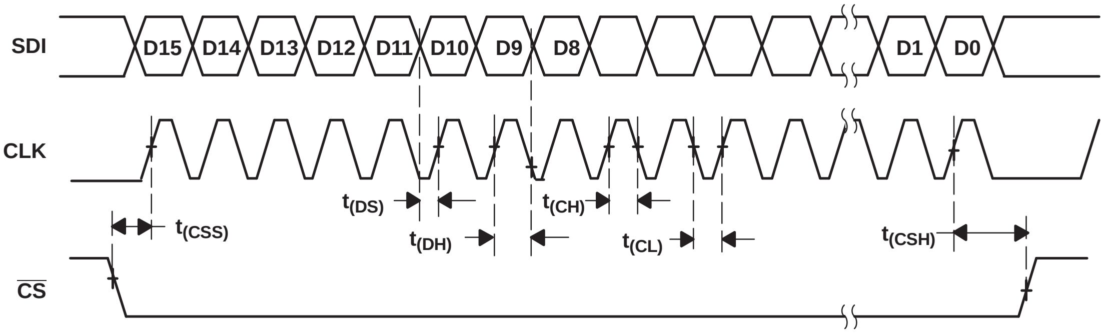


Figure 19. DAC8811 Timing Diagram

Table 2. Control Logic Truth Table(1)

CLK	$\overline{CS}$	Serial Shift Register	DAC Register
X	H	No effect	Latched
↑+	L	Shift register data advanced one bit	Latched
X	H	No effect	Latched
X	↑+	Shift register data transferred to DAC register	New data loaded from serial register

(1) ↑+ Positive logic transition; X = Don't care

Table 7.1. Serial Input Register Data Format, Data Loaded MSB First

Bit	B15 (MSB)	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage design (see Figure 20), the DAC8811 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct PCB layout design. For each code change there is a step function. If the GBP of the op amp is limited and parasitic capacitance is excessive at the inverting node then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C1 (4 pF to 20 pF typ) can be added to the design, as shown in Figure 20.

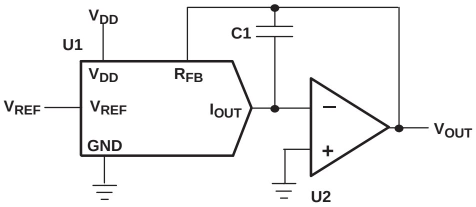


Figure 20. Gain Peaking Prevention Circuit With Compensation Capacitor

Positive Voltage Output Circuit

As Figure 21 illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC8811. This design is suggested instead of using an inverting amp to invert the output due to tolerance errors of the resistor. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a -2.5 V input to the DAC8811 with an op amp.

APPLICATION INFORMATION (continued)

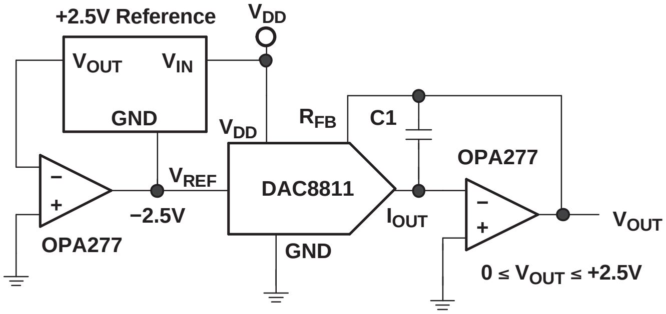


Figure 21. Positive Voltage Output Circuit

Bipolar Output Circuit

The DAC8811, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 22, external op amp U4 is added as a summing amp and has a gain of 2X that widens the output span to 5 V. A 4-quadrant multiplying circuit is implemented by using a 2.5-V offset of the reference voltage to bias U4. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full scale produces output voltages of V_{OUT} = -2.5 V to V_{OUT} = +2.5 V.

$$V_{OUT} = \left(\frac{D}{32,768} - 1\right) \times V_{REF} \tag{2}$$

External resistance mismatching is the significant error in Figure 22.

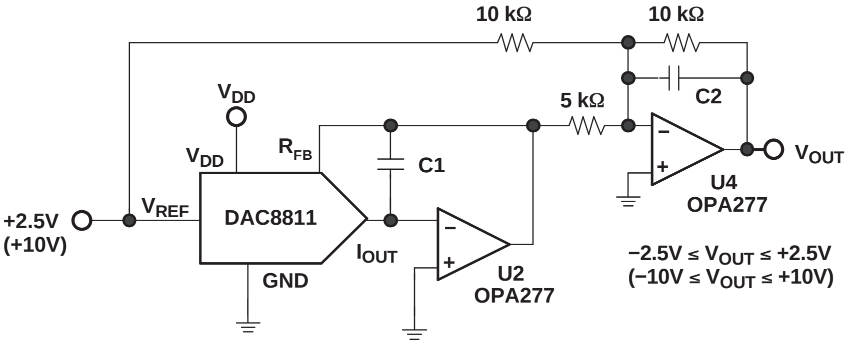


Figure 22. Bipolar Output Circuit

Programmable Current Source Circuit

A DAC8811 can be integrated into the circuit in Figure 23 to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_L = \frac{(R2 + R3) / R1}{R3} \times V_{REF} \times D \tag{3}$$

APPLICATION INFORMATION (continued)

The value of R3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive ±20 mA in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor C1 in the circuit is not suggested as a result of the change in the output impedance Z_O, according to Equation 4:

$$Z_O = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (4)$$

As shown in Equation 4, with matched resistors, Z_O is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

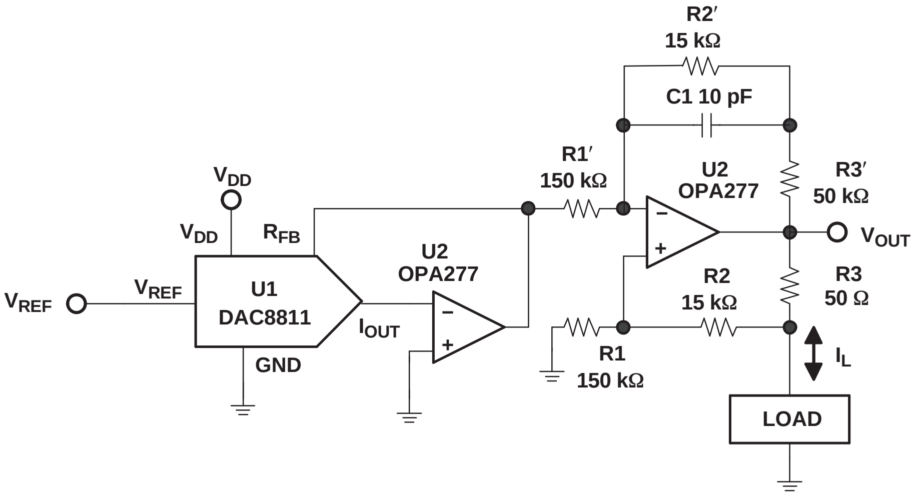


Figure 23. Programmable Bidirectional Current Source Circuit

Cross-Reference

The DAC8811 has an industry-standard pinout. Table 3 provides the cross-reference information.

Table 3. Cross-Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8811ICDGK	±1	±1	-40°C to +85°C	8-Lead MicroSOIC	MSOP-8	N/A
DAC8811IBDGK	±2	±1	-40°C to +85°C	8-Lead MicroSOIC	MSOP-8	AD5543BRM
DAC8811ICDRB	±1	±1	-40°C to +85°C	8-Lead Small Outline	SON-8	N/A
DAC8811IBDRB	±2	±1	-40°C to +85°C	8-Lead Small Outline	SON-8	N/A
N/A	±2	±1	-40°C to +85°C	8-Lead SOIC	SOIC-8	AD5543BR

Table 4. DAC8811 Revision History

Revision	Date	Description
A	12/04	Removed the *Product Preview* label.
		Added information to the Features.
		Added Output leakage current Data = 0000h, $T_A = T_{MAX}$ in the *Electrical Characteristics* table.
		Added Input high voltage for 2.7 V and 5 V in the Electrical Characteristics table.
		Changed the values of the *Power Requirements* and the *AC characteristics* in the Electrical Characteristics table.
B	10/06	Changed the ESD rating, HBM from 1500 to 4000 in the *Absolute Maximum Ratings*.
		Revised Figure 8.
		Added new paragraph to the *Description* text.
		Added test condition to the AC Characteristics in the *Electrical Characteristics* table.
		Added Table Note 3 to the *Electrical Characteristics*.
		Added row to ABS MAX table, Corrected AC Characteristics section in Electrical Characteristics table

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8811IBDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811IBDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811IBDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811IBDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811IBDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811ICDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811ICDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811ICDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811ICDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811ICDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D11	Samples
DAC8811ICDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D11	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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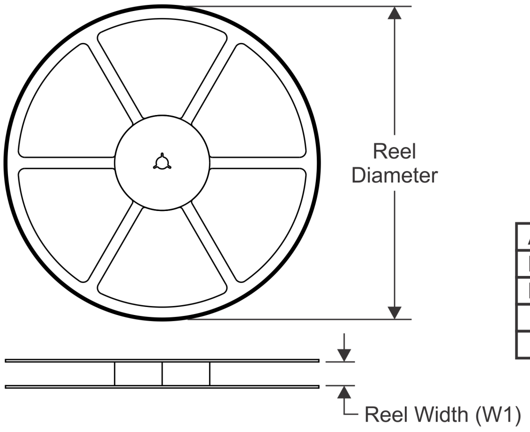
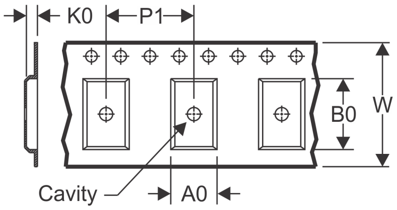
TAPE AND REEL INFORMATION

REEL DIMENSIONS

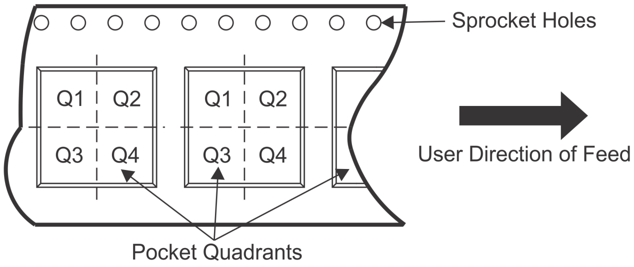


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

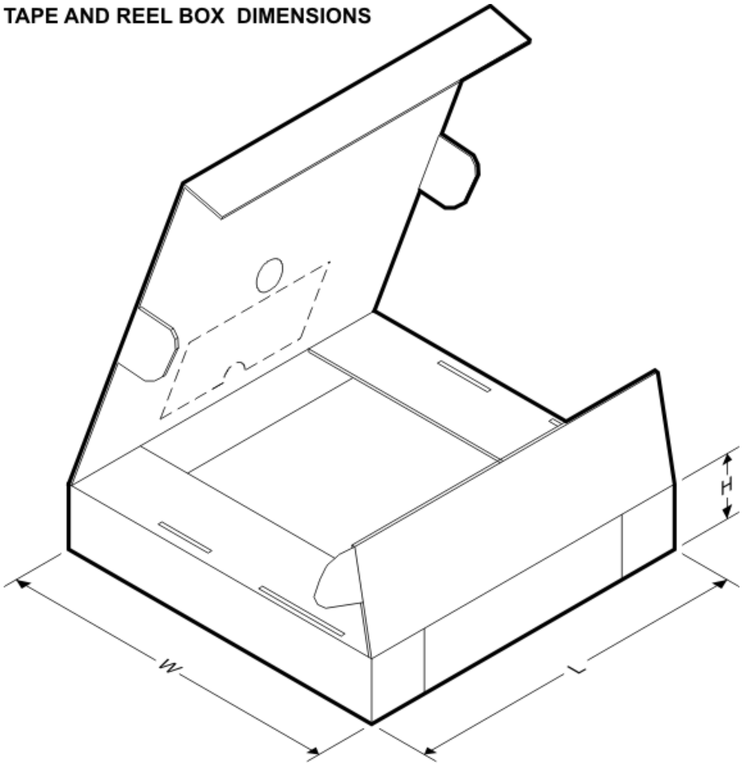
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8811IBDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8811IBDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8811IBDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DAC8811ICDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8811ICDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8811ICDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

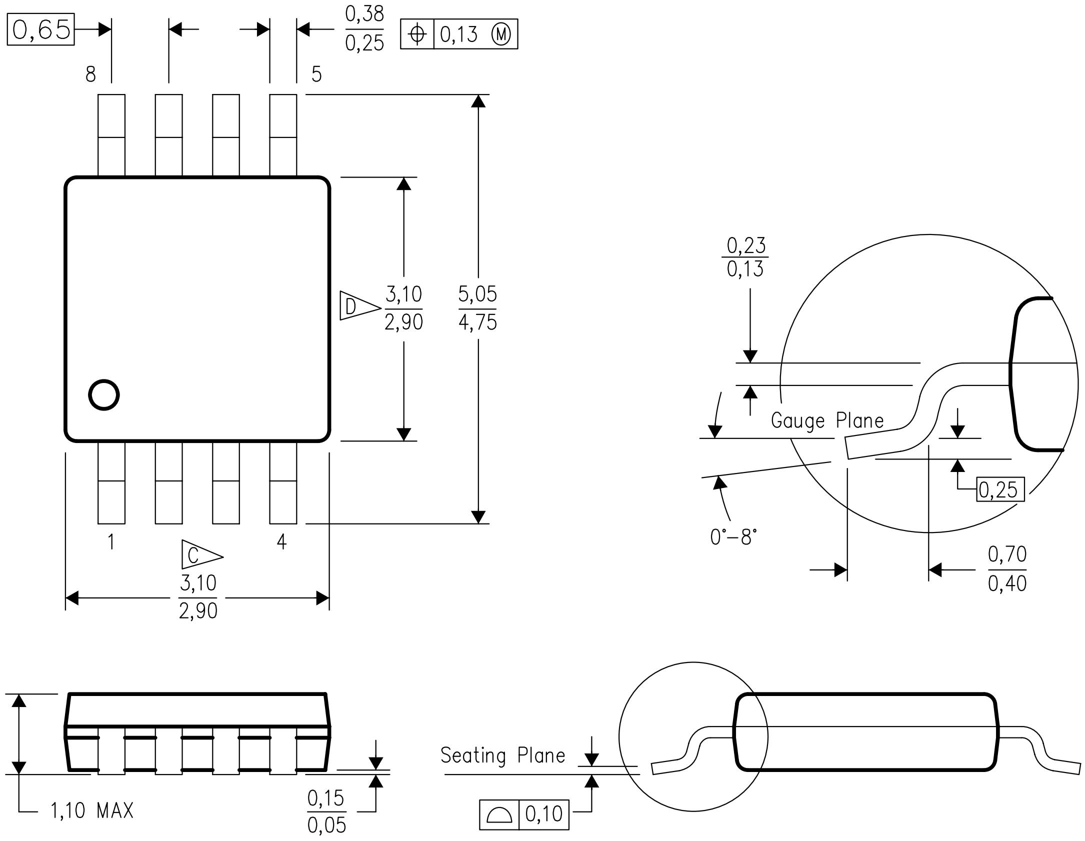
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8811IBDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
DAC8811IBDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
DAC8811IBDRBT	SON	DRB	8	250	210.0	185.0	35.0
DAC8811ICDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
DAC8811ICDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
DAC8811ICDRBT	SON	DRB	8	250	210.0	185.0	35.0

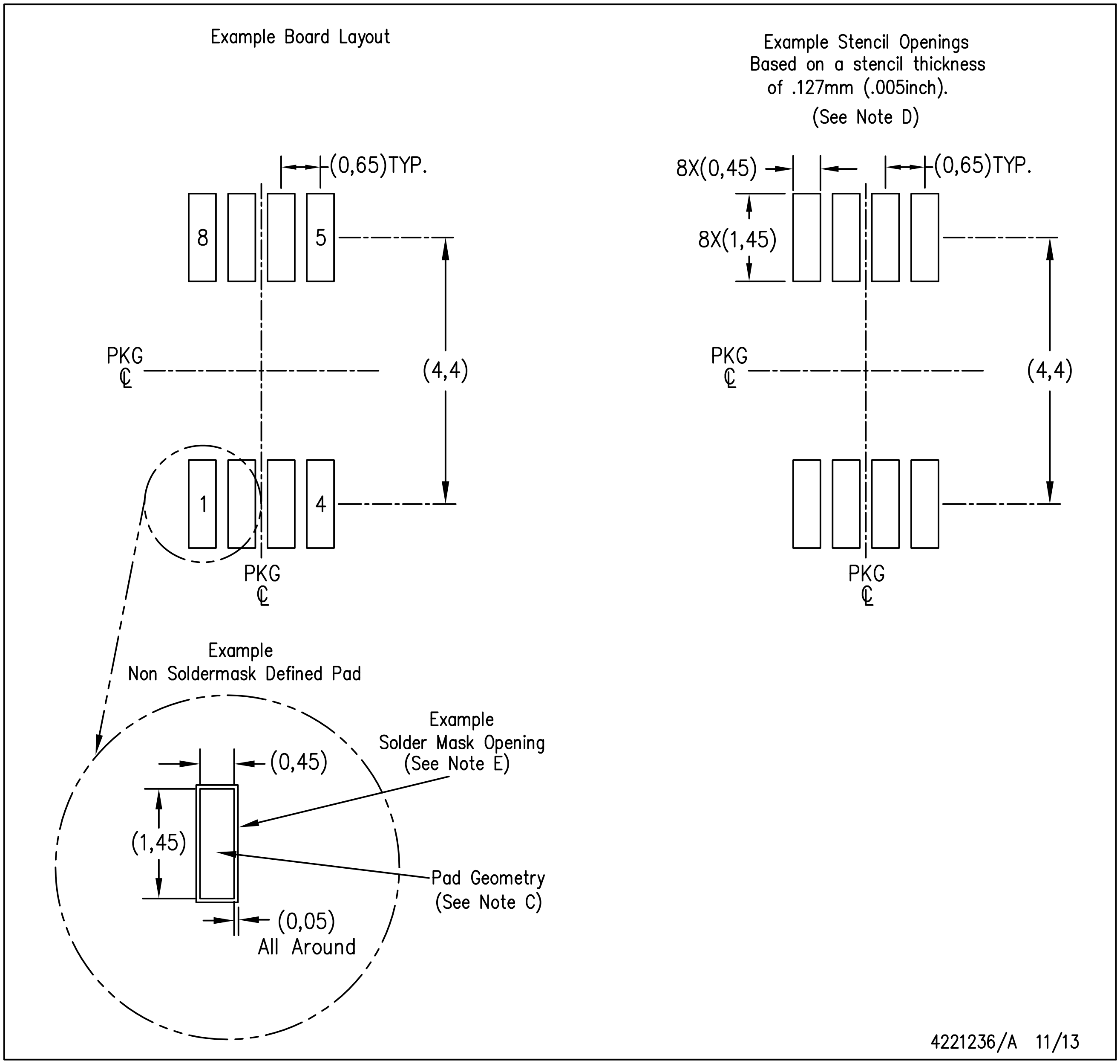
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

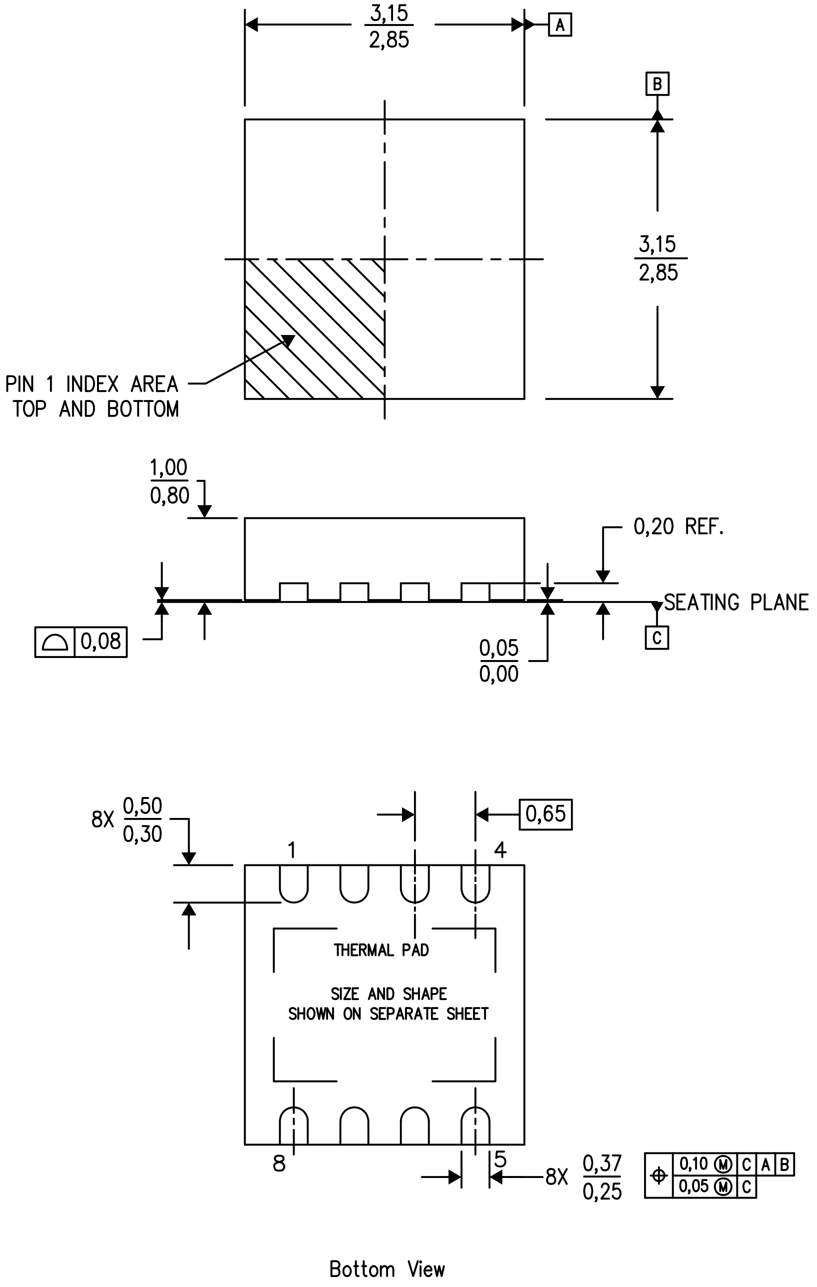
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

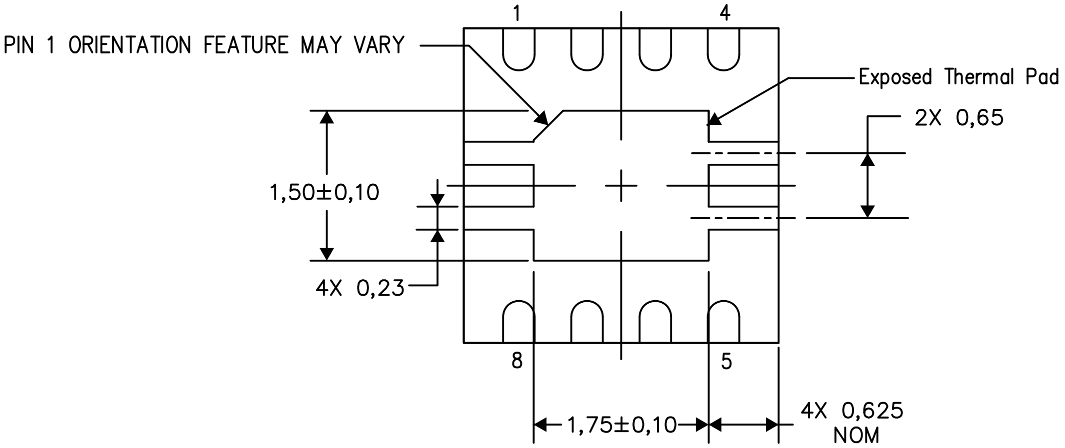
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



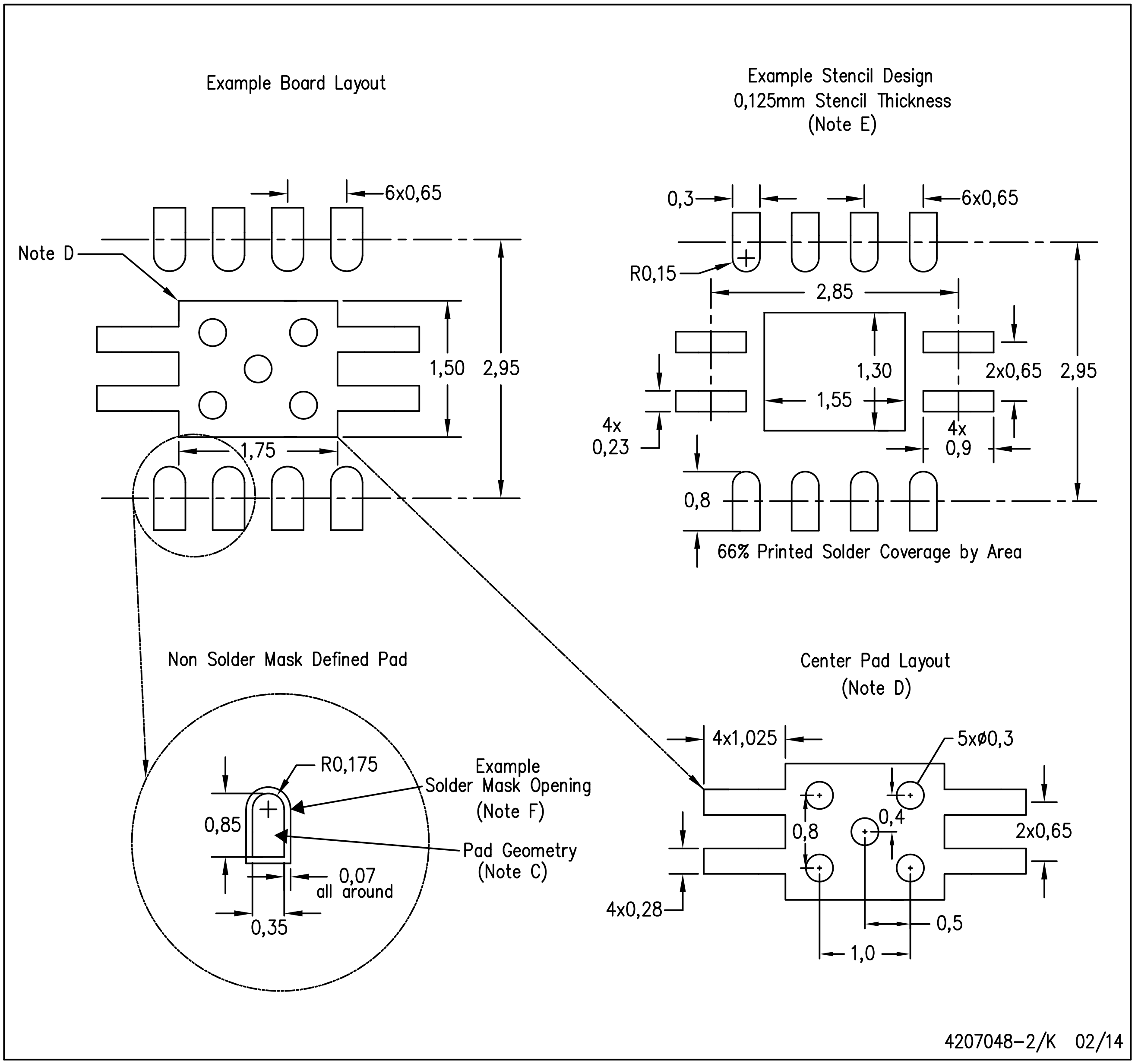
Bottom View

Exposed Thermal Pad Dimensions

4206340-2/O 02/14

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4207048–2/K 02/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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