DATA SHEET

3.3 V Differential ECL/PECL PLL Clock Generator

MPC9992

The MPC9992 is a 3.3 V compatible, PLL based PECL clock driver. Using SiGe technology and a fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC9992 makes the device ideal for workstation, mainframe computer and telecommunication applications. With output frequencies up to 400 MHz and output skews less than 100 ps the device meets the needs of the most demanding clock applications. The MPC9992 offers a differential PECL input and a crystal oscillator interface. All control signals are LVCMOS compatible.

3.3 V DIFFERENTIAL ECL/PECL CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-04

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-04

Features

- 7 differential outputs, PLL based clock generator
- SiGe technology supports minimum output skew (max. 100 ps)
- Supports up to two generated output clock frequencies with a maximum clock frequency up to 400 MHz
- Selectable crystal oscillator interface and PECL compatible clock input
- SYNC pulse generation
- PECL compatible differential clock inputs and outputs
- Single 3.3 V (PECL) supply
- Ambient temperature range 0°C to +70°C
- Standard 32 lead LQFP package
- Pin and function compatible to the MPC992
- 32-lead Pb-free Package Available

Functional Description

The MPC9992 utilizes PLL technology to frequency lock its outputs onto an input reference clock. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9992 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 2:1, 3:1, 3:2 and 5:2 can be realized. The two banks of outputs and the feedback frequency divider can be programmed by the FSEL[2:0] pins of the device. The VCO_SEL pin provides an extended PLL input reference frequency range.

The SYNC pulse generator monitors the phase relationship between the QA[3:0] and QB[2:0] output banks. The SYNC generator output signals the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies.

The REF_SEL pin selects the differential PECL compatible input pair or crystal oscillator interface as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9992 requires an external reset signal for start-up and for PLL recovery in case the reference input is interrupted. Assertion of the reset signal forces all outputs to the logic low state.

The MPC9992 is fully 3.3 V compatible and requires no external loop filter components. The differential clock input (PCLK) is PECL compatible and all control inputs accept LVCMOS compatible signals while the outputs provide PECL compatible levels with the capability to drive terminated 50 Ω transmission lines.

The device is pin and function compatible to the MPC992 and is packaged in a 32-lead LQFP package.

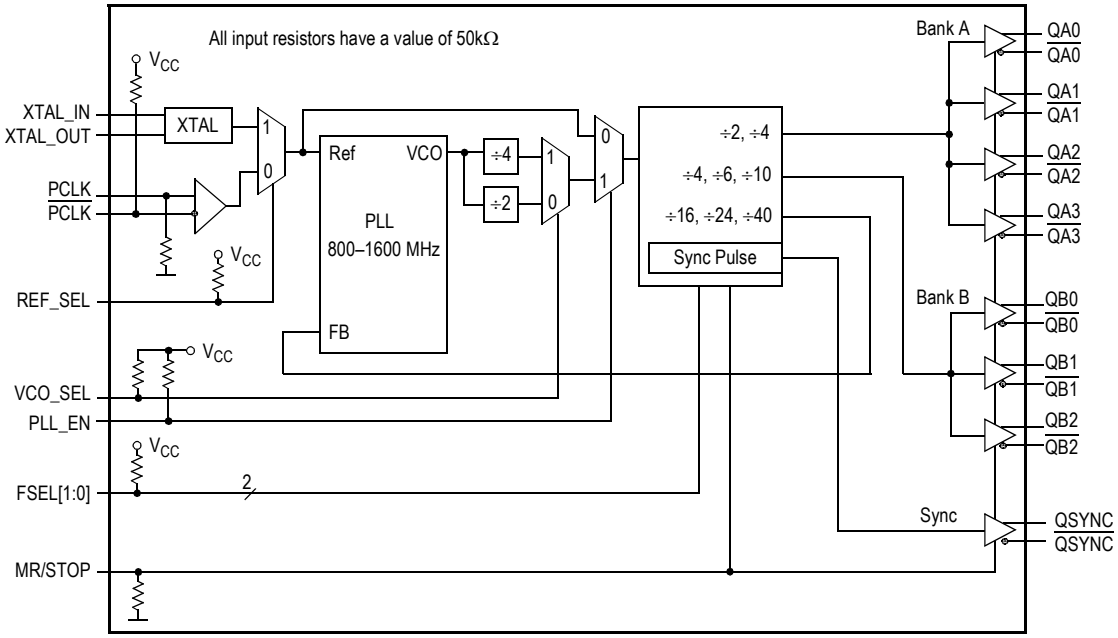


Figure 1. MPC9992 Logic Diagram

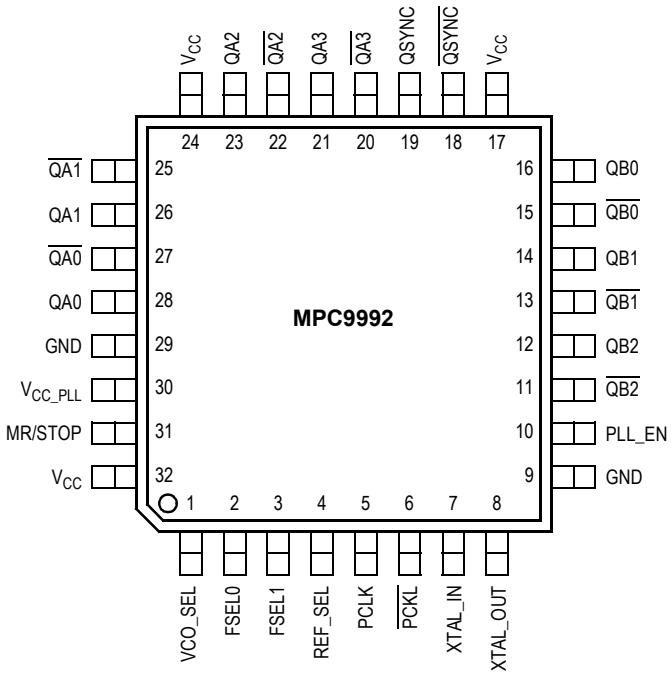


Figure 2. MPC9992 32-Lead Package Pinout (Top View)

Table 1. MPC9992 PLL Configurations

VCO_SEL	FSEL_0	FSEL_1	f_{REF} (MHz)	QA[3:0] (N_A)	QB[2:0] (N_B)	Frequency Ratio QA to QB	Internal Feedback (M · VCO_SEL)
0	0	0	16.6–33.3	VCO÷8 (6 · f_{REF})	VCO÷12 (4 · f_{REF})	3÷2	VCO÷48
0	0	1	25–50	VCO÷4 (8 · f_{REF})	VCO÷8 (4 · f_{REF})	2÷1	VCO÷32
0	1	0	10–20	VCO÷8 (10 · f_{REF})	VCO÷20 (4 · f_{REF})	5÷2	VCO÷80
0	1	1	16.6–33.3	VCO÷4 (12 · f_{REF})	VCO÷12 (4 · f_{REF})	3÷1	VCO÷48
1	0	0	8.3–16.6	VCO÷16 (6 · f_{REF})	VCO÷24 (4 · f_{REF})	3÷2	VCO÷96
1	0	1	12.5–25	VCO÷8 (8 · f_{REF})	VCO÷16 (4 · f_{REF})	2÷1	VCO÷64
1	1	0	5–10	VCO÷16 (10 · f_{REF})	VCO÷40 (4 · f_{REF})	5÷2	VCO÷160
1	1	1	8.3–16.6	VCO÷8 (12 · f_{REF})	VCO÷24 (4 · f_{REF})	3÷1	VCO÷96

Table 2. Function Table (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects PCLK, $\overline{\text{PCLK}}$ as PLL references signal input	Selects the crystal oscillator as PLL reference signal input
VCO_SEL	1	Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (high input frequency range)	Selects VCO÷4. The VCO frequency is scaled by a factor of 4 (low input frequency range).
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9992 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
MR/STOP	0	Normal operation	Reset of the device and output disable (output clock stop). The outputs are stopped in logic low state: Qx=L, $\overline{\text{Qx}}$=H. The minimum reset period should be greater than one reference clock cycle.

VCO_SEL and FSEL[1:0] control the operating PLL frequency range and input/output frequency ratios.
See Table 1 for the device frequency configuration.

Table 3. Pin Configuration

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	PECL	Differential reference clock signal input
XTAL_IN, XTAL_OUT		Analog	Crystal oscillator interface
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL Enable/Bypass mode select
REF_SEL	Input	LVCMOS	PLL reference signal input select
MR/STOP	Input	LVCMOS	Device reset and output clock disable (stop in logic low state)
FSEL[1:0]	Input	LVCMOS	Output and PLL feedback frequency divider select
QA[0-3], $\overline{\text{QA[0–3]}}$	Output	PECL	Differential clock outputs (bank A)
QB[0-2], $\overline{\text{QB[0–2]}}$	Output	PECL	Differential clock outputs (bank B)
QSYNC, $\overline{\text{QSYNC}}$	Output	PECL	Differential clock outputs (bank C)
GND	Supply	GND	Negative power supply
V_{CC}	Supply	V_{CC}	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details

Table 4. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	175			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	1000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature(1) (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9992 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9992 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, GND = 0V, T_A = 0°C to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential PECL Clock Inputs (PCLK, $\overline{PCLK}$)[1]						
V_{PP}	AC Differential Input Voltage[2]	0.2		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[3]	1.0		V_{CC}-0.3	V	Differential operation
I_{IN}	Input Current[4]			±120	µA	V_{IN} = V_{CC} or GND
LVCMOS Control Inputs (VCO_SEL, PLL_EN, MR/STOP, REF_SEL, FSEL[1:0])						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[4]			±120	µA	V_{IN} = V_{CC} or GND
PECL Clock Outputs (QA[3:0], $\overline{QA[3:0]}$, QB[2:0], $\overline{QB[2:0]}$, QSYNC, $\overline{QSYNC}$)						
V_{OH}	Output High Voltage	V_{CC}–1.025		V_{CC}–0.880	V	I_{OH} = –30 mA
V_{OL}	Output Low Voltage	V_{CC}–1.920		V_{CC}–1.620	V	I_{OL} = –5 mA
Supply Current and Voltage						
V_{CC_PLL}	PLL Supply Voltage	2.955		V_{CC}	V	V_{CC_PLL} pin
I_{CC_PLL}	Maximum PLL Supply Current		9.0	12	mA	V_{CC_PLL} pin
I_{GND}[5]	Maximum Supply Current		80	110	mA	GND pins

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Inputs have pull-down resistors affecting the input current.
4. Equivalent to a termination of 50 Ω to V_{TT}.
5. Does not include output drive current which is dependant on output termination methods.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, GND = 0 V, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	÷32 feedback	25.0		50.0	MHz	PLL locked
		÷48 feedback	16.67		33.3	MHz	
		÷64 feedback	12.5		25.0	MHz	
		÷80 feedback	10.0		20.0	MHz	
		÷96 feedback	8.33		16.67	MHz	
		÷160 feedback	5.0		10.0	MHz	
	Input Reference Frequency in PLL Bypass Mode[2]				400	MHz	PLL bypass
f_{XTAL}	Crystal Interface Frequency Range[3]		10		20	MHz	
f_{VCO}	VCO Frequency Range[4]		800		1600	MHz	
f_{MAX}	Output Frequency	÷4 output	200.0		400.0	MHz	PLL locked
		÷8 output	100.0		200.0	MHz	
		÷12 output	66.6		133.3	MHz	
		÷16 output	50.0		100.0	MHz	
		÷20 output	40.0		80.0	MHz	
		÷24 output	33.3		66.6	MHz	
		÷48 output	16.6		33.3	MHz	
V_{PP}	Differential Input Voltage[5] (peak-to-peak)		0.3		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[6]	(PCLK)	1.2		V_{CC}–0.3	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	(PCLK)	0.6	0.8		V	
$t_{PW,MIN}$	Input Reference Pulse Width[7]		2.0			ns	
$t_{sk(O)}$	Output-to-Output Skew				100	ps	
DC	Output Duty Cycle[8]		48	50	52	%	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter[9]			30	79	ps	
$t_{JIT(PER)}$	Period Jitter[9]			43	106	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[9]	RMS (1 σ)[10]		86	212	ps	
BW	PLL Closed Loop Bandwidth[11]	÷32 feedback		0.60-1.5		MHz	
		÷48 feedback		0.40-1.2		MHz	
		÷64 feedback		0.30-1.0		MHz	
		÷80 feedback		0.30-0.8		MHz	
		÷96 feedback		0.20-0.7		MHz	
		÷160 feedback		0.15-0.4		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	
t_r, t_f	Output Rise/Fall Time		0.05		1.0	ns	20% to 80%

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. In bypass mode, the MPC9992 divides the input reference clock.
3. The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio: $f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot VCO\_SEL)$ and 10 MHz ≤ f_{XTAL} ≤ 20 MHz.
4. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$
5. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics.
6. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification.
7. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF, MIN.}$ E.g. at f_{REF} = 50 MHz the input duty cycle range is 10% < DC < 90%.
8. Output duty cycle for QAx and QBx outputs. The pulse width for the QSYNC output is equal to one QAx output period t_{QA} ± 5%.
9. Jitter data is valid f_{ref} = 25 MHz.
10. See application section for a jitter calculation for other confidence factors than 1 σ.
11. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

SYNC Output Description

The MPC9992 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9992 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic high) one QA period in duration. The placement of the pulse is dependent on the QA and QB output frequencies ratio. Figure 3 shows the waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank B outputs.

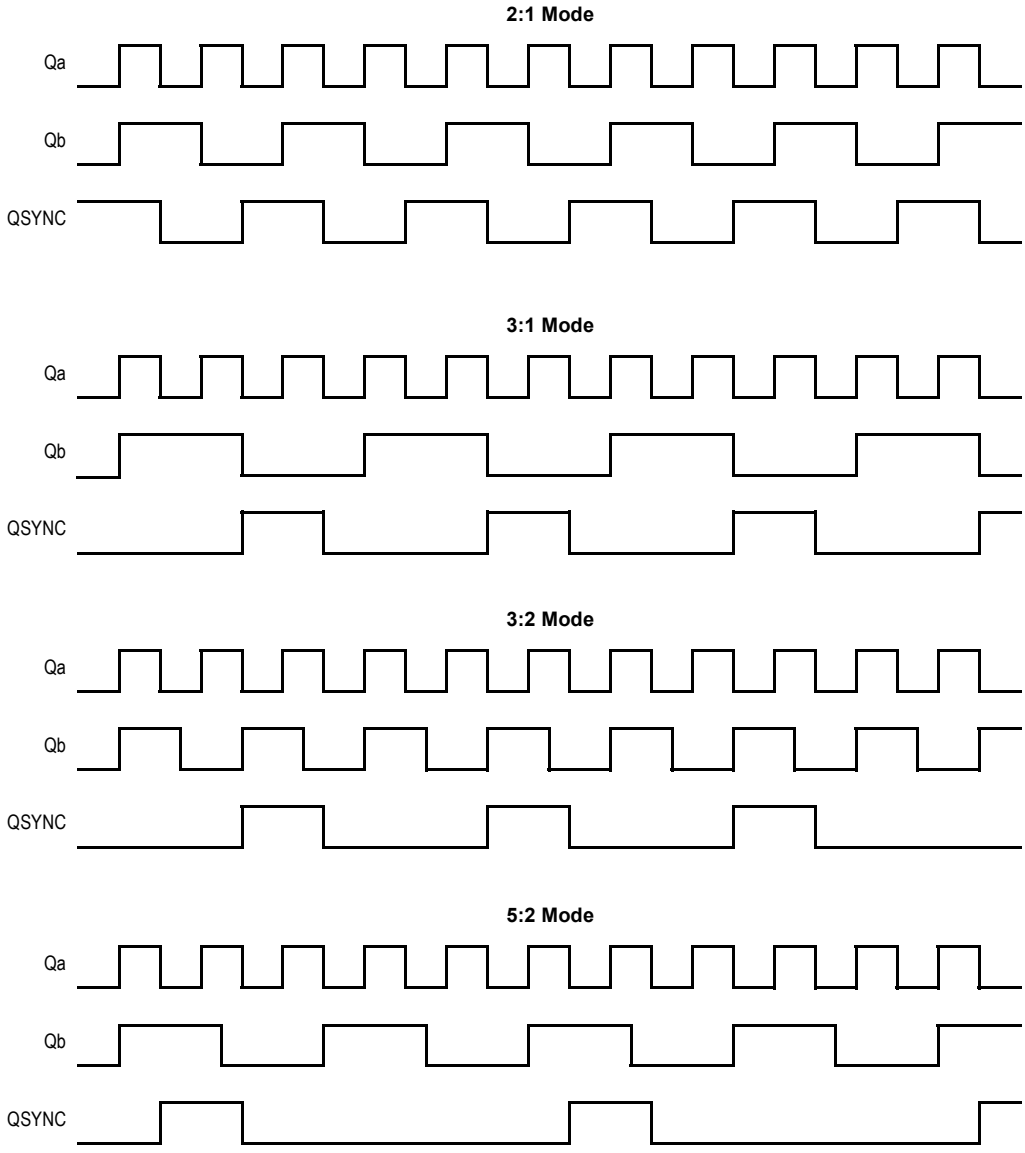


Figure 3. QSYNC Timing Diagram

Power Supply Filtering

The MPC9992 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9992 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9992. Figure 4 illustrates a typical power supply filter scheme. The MPC9992 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 9 mA (12 mA maximum), assuming that a minimum of 2.955 V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 4 must have a resistance of 10-15 Ω to meet the voltage drop criteria.

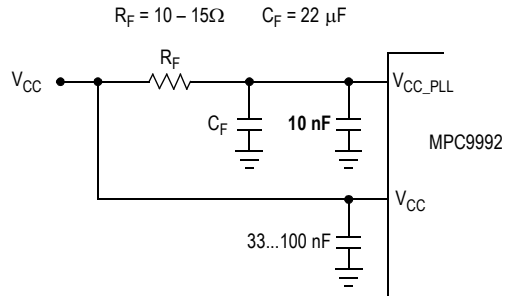


Figure 4. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 4, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

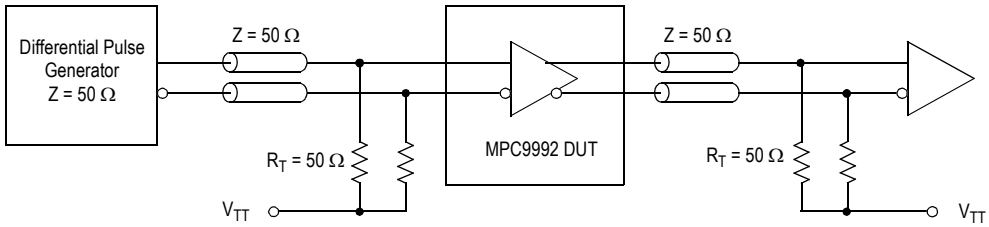
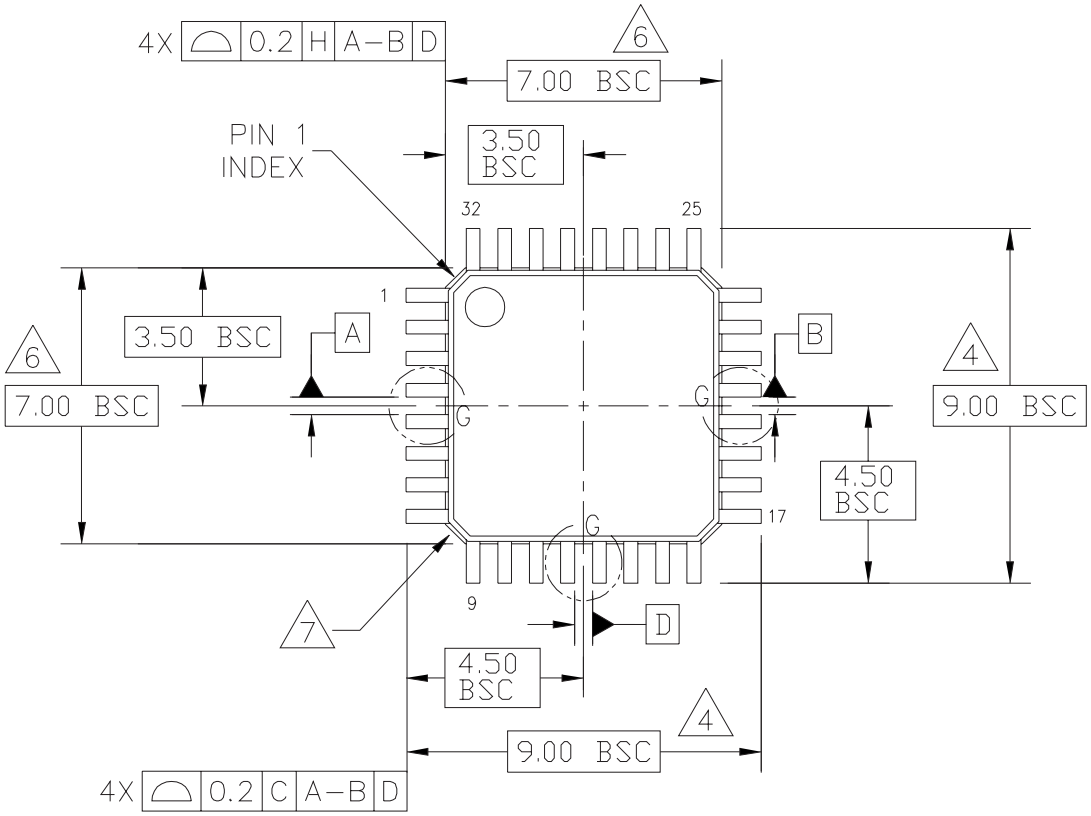
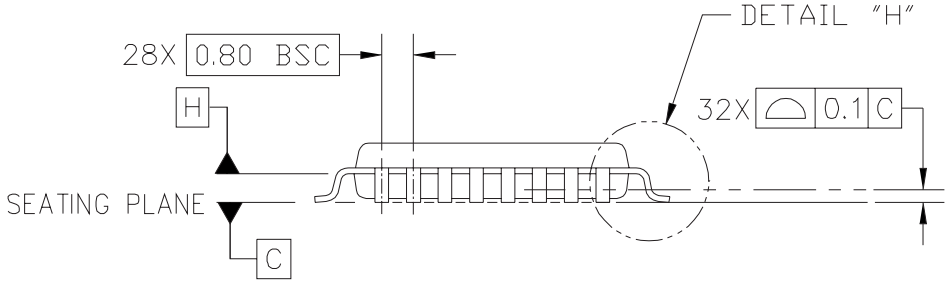


Figure 5. MPC9992 AC Test Reference

PACKAGE DIMENSIONS



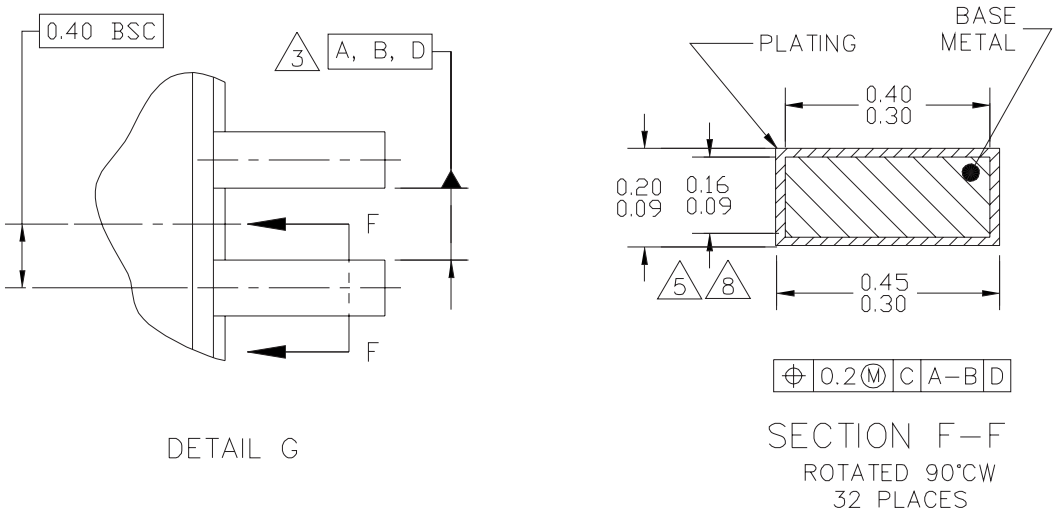


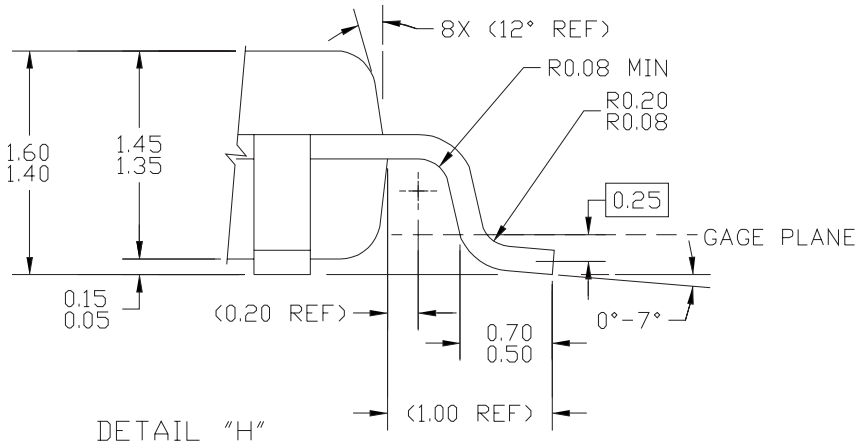
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

PAGE 1 OF 3

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

PACKAGE DIMENSIONS





© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: C
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	

PAGE 3 OF 3

CASE 873A-04
ISSUE C
32-LEAD LQFP PACKAGE

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

www.IDT.com

XX-XXXX-XXXXX