- **IEEE 802.5 and IBM Token-Ring Network™ Compatible**
- **IEEE 802.3 and Blue Book Ethernet™ Network Compatible**
- **Compatible With TI380FPA FNL PacketBlaster™**
- **Token-Ring Features**
  - **16- or 4-Megabit-per-Second Data Rates**
  - **Supports Up to 18K-Byte Frame Size (16-Mbps Operation Only)**
  - **Supports Universal and Local Network Addressing**
  - **Early Token-Release Option (16-Mbps Operation Only)**
  - **Compatible With the TMS38054**
- **Ethernet Features**
  - **10 Megabit-per-Second Data Rate in Half-Duplex Mode**
  - **20 Megabit-per-Second Data Rate in Full-Duplex Mode**
  - **Compatible With Most Ethernet Serial-Network-Interface Devices**
  - **Network-Speed Self-Test Feature**
- **Glueless Interface to DRAMs**
- **High-Performance 16-Bit CPU for Communications-Protocol Processing**
- **1- to 16.5-Megabyte-per-Second High-Speed Bus Master DMA Interface**
- **Low-Cost Host-Slave I/O Interface Option**
- **Up to 32-Bit Host Address Bus**
- **Selectable Host System-Bus Options**
- **Adapter Local-Bus Speed Is Switchable Between 4 MHz and 6 MHz**
- **80x8x or 68xxx-Type Bus and Memory Organization**
  - **8- or 16-Bit Data Bus on 80x8x Buses**
  - **Optional Parity Checking**
- **Dual-Port DMA and Direct I/O Transfers to Host Bus**
- **Supports 8- or 16-Bit Pseudo-DMA Operation**
- **Enhanced-Address-Copy-Option (EACO) Interface Supports External Address-Checking Logic for Bridging or External Custom Applications**
- **Support for Module High-Impedance In-Circuit Testing**
- **Built-In Real-Time Error Detection**
- **Bring-Up and Self-Test Diagnostics With Loopback**
- **Automatic Frame-Buffer Management**
- **2- to 33-MHz System-Bus Clock**
- **Slow-Clock Low-Power Mode**
- **Single 5-V Supply**
- **0.8-μm CMOS Technology**
- **250-mA Typical Latch-Up Immunity at 25°C**
- **ESD Protection Exceeds 2000 V**
- **144-Pin Plastic Thin Quad Flat Package (PGE Suffix)**
- **Operating Temperature Range 0°C to 70°C**

ADVANCE INFORMATION

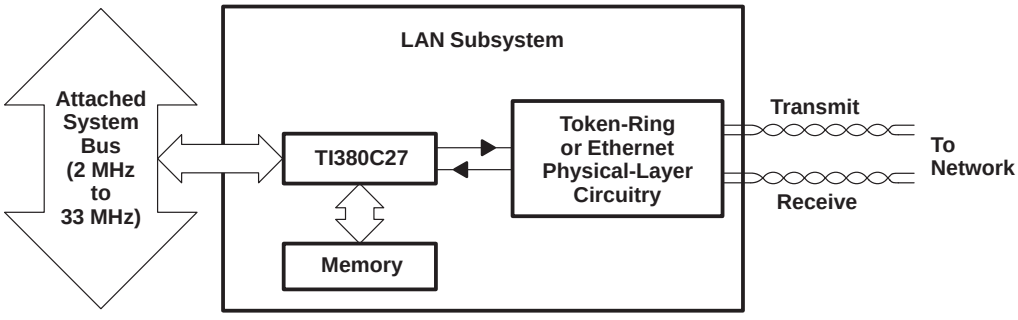

Figure 1. Network-Commprocessor Applications Diagram

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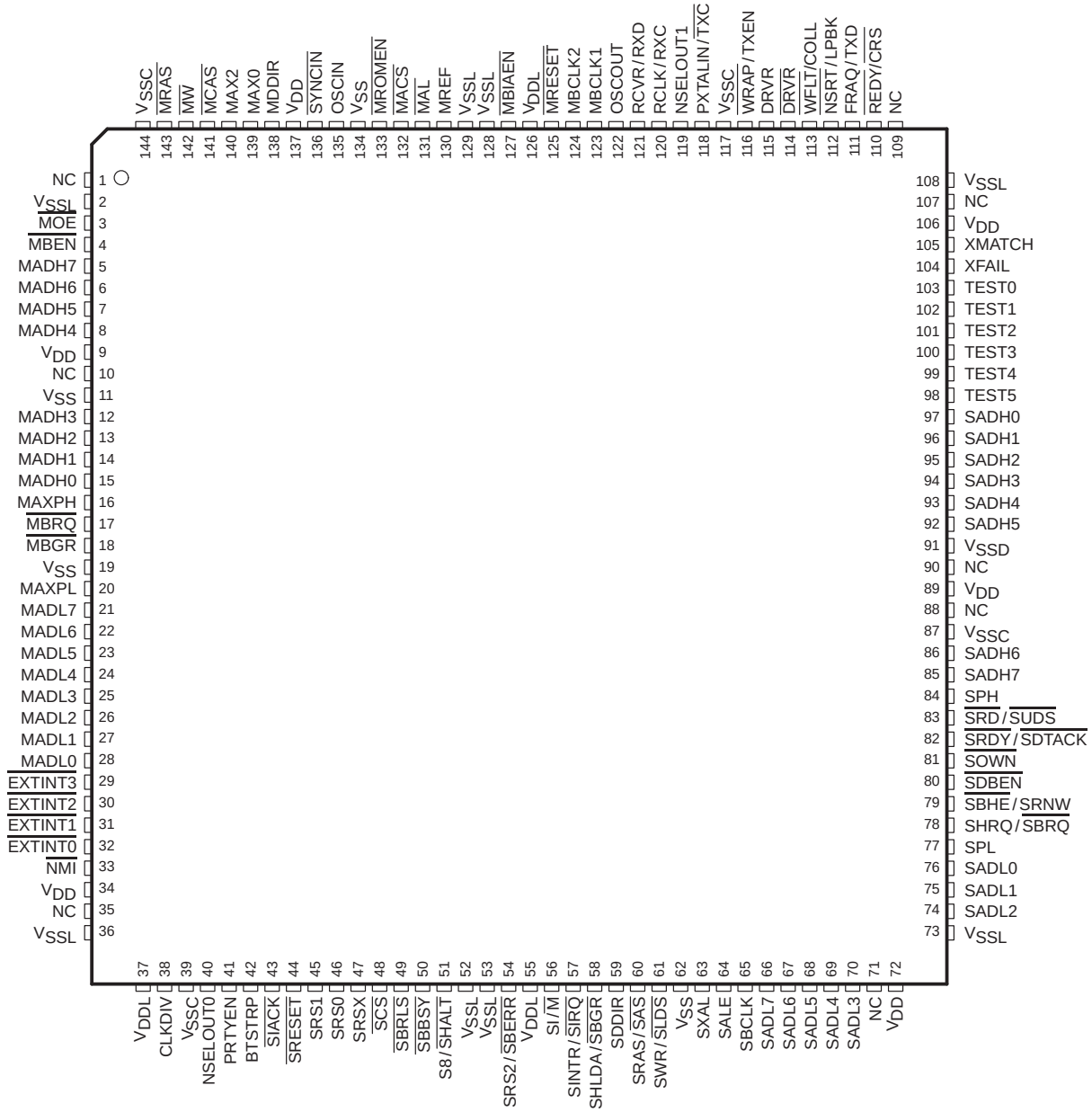
PacketBlaster is a trademark of Texas Instruments Incorporated.
Ethernet is a trademark of Xerox Corporation.

pin assignments

PGE PACKAGE
(TOP VIEW)



ADVANCE INFORMATION

description

The TI380C27 is a single-chip network-communications processor (commprocessor) that supports token-ring or Ethernet local area networks (LANs). Token ring at a data rate of either 16 Mbps or 4 Mbps or Ethernet at a data rate of either 10 Mbps (half duplex) or 20 Mbps (full duplex) can be selected. A flexible configuration scheme allows network type and speed to be configured by hardware or software. This allows the design of LAN subsystems that support both token-ring and Ethernet networks by electrically or physically switched network front-end circuits. In addition, the TI380C27 can be used with the TI380FPA PacketBlaster for maximum performance.

The TI380C27 token-ring capability conforms to ISO 8802–5/IEEE 802.5–1992 standards and has been verified to be completely IBM Token-Ring Network compatible. By integrating the essential control building blocks needed on a LAN-subsystem card into one device, the TI380C27 can ensure that this IBM compatibility is maintained in silicon.

The TI380C27 Ethernet capability conforms to ISO/IEC 8802–3 (ANSI/IEEE Std. 802.3) CSMA/CD standards and the Ethernet Blue Book standard.

The high degree of integration of the TI380C27 makes it a virtual LAN subsystem on a single chip. Protocol handling, host-system interfacing, memory interfacing, and communications processing are all provided through the TI380C27. To complete LAN-subsystem design, only the network-interface hardware, local memory, and minimal additional components such as PAL® devices and crystal oscillators need to be added.

The TI380C27 provides a 32-bit system-memory address reach with a high-speed bus-master DMA interface that supports rapid communications with the host system. In addition, the TI380C27 supports direct I/O and a low-cost 8- or 16-bit pseudo-DMA interface that requires only a chip select to work directly on an 80x8x 8-bit slave I/O interface. Finally, selectable 80x8x or 68xxx-type host-system bus and memory organization add to design flexibility.

The TI380C27 supports addressing for up to 2M bytes of local memory. This expanded memory capacity can improve LAN-subsystem performance by minimizing the frequency of host LAN-subsystem communications by allowing larger blocks of information to be transferred at one time. The support of large local memory is important in applications that require large data transfers (such as graphics or data-base transfers) and in heavily loaded networks where the extra memory can provide data buffers to store data until it can be processed by the host.

The proprietary CPU used in the TI380C27 allows protocol software to be downloaded into RAM or stored in ROM in the local-memory space. By moving protocols to the LAN subsystem, overall system performance is increased. This is accomplished by the offloading of processing from the host system to the TI380C27, which can also reduce LAN-subsystem-to-host communications. As other protocol software is developed, greater differentiation of end products with enhanced system performance will be possible.

In addition, the TI380C27 includes hardware counters that provide real-time error detection and automatic frame-buffer management. These counters control system-bus retries, control burst size, and track host and LAN-subsystem buffer status. Previously, these counters needed to be maintained in software. By integrating them into hardware, software overhead is removed and LAN-subsystem performance is improved.

The TI380C27 implements a TI-patented enhanced-address-copy-option (EACO) interface. This interface supports external address-checking devices, such as the TMS380SRA source-routing accelerator. The TI380C27 has a 128-word external I/O space in its memory to support external address-checker devices and other hardware extensions to the TMS380 architecture.

The major blocks of the TI380C27 include the communications processor (CP), the system interface (SIF), the memory interface (MIF), the protocol handler (PH), the clock generator (CG), and the adapter-support function (ASF), as shown in the functional block diagram.

The TI380C27 is available in a 144-pin plastic thin quad flat package (PGE suffix) and is characterized for operation from 0°C to 70°C.

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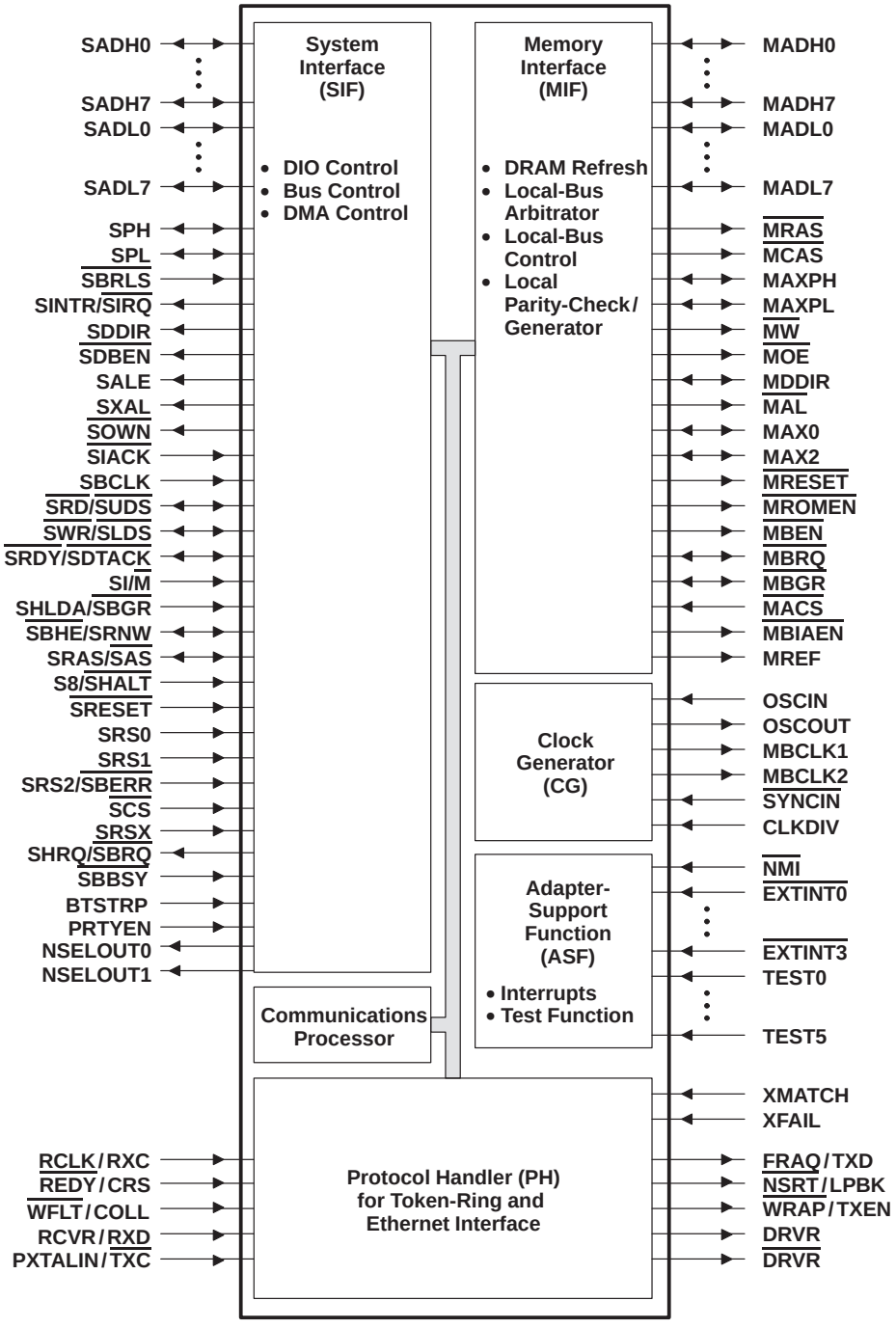
ADVANCE INFORMATION

description (continued)

The TI380C27 has a bus interface to the host system, a bus interface to local memory, and an interface to the physical-layer circuitry. Pin names starting with the letter S attach to the host-system bus and pin names starting with the letter M attach to the local-memory bus. Active-low signals have names with overbars; e.g., $\overline{\text{SCS}}$.

functional block diagram



ADVANCE INFORMATION

Pin Functions

PIN NAME	PIN NO.	I/O†	DESCRIPTION
BTSTRP	42	I	Bootstrap. The value on BTSTRP is loaded into the BOOT bit of the SIFACL register at reset (i.e., when SRESET is asserted or the ARESET bit in the SIFACL register is set) to form a default value. BTSTRP indicates whether chapters 0 and 31 of the memory map are RAM or ROM. If these chapters are RAM, the TI380C27 is denied access to the local-memory bus until the CPHALT bit in the SIFACL register is cleared. H = Chapters 0 and 31 of local memory are RAM based (see Note 1). L = Chapters 0 and 31 of local memory are ROM based.
CLKDIV	38	I	Clock divider select (see Note 2) H = 64-MHz OSCIN for 4-MHz local bus L = 32-MHz OSCIN for 4-MHz local bus or 48-MHz OSCIN for 6-MHz local bus
$\overline{\text{EXTINT0}}$ $\overline{\text{EXTINT1}}$ $\overline{\text{EXTINT2}}$ $\overline{\text{EXTINT3}}$	32 31 30 29	I/O	Reserved; must be pulled high (see Note 3)
$\overline{\text{MACS}}$	132	I	Reserved; must be tied low (see Note 4)
MADH0 MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	15 14 13 12 8 7 6 5	I/O	Local-memory address, data, and status bus — high byte. For the first quarter of the local-memory cycle, these bus lines carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0 and the least significant bit is MADH7. Memory Cycle 1Q: Signal = AX4, A0–A6 2Q: Status 3Q: D0–D7 4Q: D0–D7
MADL0 MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	28 27 26 25 24 23 22 21	I/O	Local-memory address, data, and status bus — low byte. For the first quarter of the local-memory cycle, these bus lines carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0 and the least significant bit is MADL7. Memory Cycle 1Q: Signal = A7–A14 2Q: AX4, A0–A6 3Q: D8–D15 4Q: D8–D15
$\overline{\text{MAL}}$	131	O	Memory-address latch. $\overline{\text{MAL}}$ is a strobe signal for sampling the address at the start of the memory cycle; it is used by SRAMs and EPROMs. The full 20-bit word address is valid on MAX0, MAXPH, MAX2, MAXPL, MADH0–MADH7, and MADL0–MADL7. Three 8-bit transparent latches can be used to retain a 20-bit static address throughout the cycle. Rising edge = No signal latching Falling edge = Allows the above address signals to be latched
MAX0	139	I/O	Local-memory-extended address bit. MAX0 drives AX0 at row-address time and drives A12 at column-address and data-valid times for all cycles. This signal can be latched by $\overline{\text{MRAS}}$. Driving A12 eases interfacing to a BIA ROM. Memory Cycle 1Q: Signal = AX0 2Q: A12 3Q: A12 4Q: A12

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
2. The TI380FPA and TMS380SRA are currently supported only with the 4-MHz local bus in either CLKDIV state. Expansion to support the 6-MHz local bus is under development.
3. Each pin must be individually tied to V_{CC} with a 1-kΩ pullup resistor.
4. Pin should be connected to ground.

ADVANCE INFORMATION

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
MAX2	140	I/O	Local-memory-extended address bit. MAX2 drives AX2 at row-address time, which can be latched by MRAS, and drives A14 at column-address and data-valid times for all cycles. Driving A14 eases interfacing to a BIA ROM. Memory Cycle 1Q 2Q 3Q 4Q Signal AX2 A14 A14 A14
MAXPH	16	I/O	Local-memory-extended address and parity — high byte. For the first quarter of a memory cycle, MAXPH carries the extended-address bit AX1; for the second quarter of a memory cycle, it carries the extended-address bit AX0; and for the last half of the memory cycle, it carries the parity bit for the high-data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX1 AX0 Parity Parity
MAXPL	20	I/O	Local-memory-extended address and parity — low byte. For the first quarter of a memory cycle, MAXPL carries the extended-address bit AX3; for the second quarter of a memory cycle, it carries extended-address bit AX2; and for the last half of the memory cycle, it carries the parity bit for the low-data byte. Memory Cycle 1Q 2Q 3Q 4Q Signal AX3 AX2 Parity Parity
MBCLK1 MBCLK2	123 124	O	Local-bus clock 1 and local-bus clock 2. These signals are referenced for all local-bus transfers. MBCLK2 lags MBCLK1 by a quarter of a cycle. These clocks operate according to: MBCLK[1:2] OSCIN CLKDIV 8 MHz 64 MHz H 8 MHz 32 MHz L 12 MHz 48 MHz L
$\overline{\text{MBEN}}$	4	O	Buffer enable. $\overline{\text{MBEN}}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. This signal is used in conjunction with MDDIR, which selects the buffer output direction. H = Buffer output disabled L = Buffer output enabled
$\overline{\text{MBGR}}$	18	I/O	Reserved; must be left unconnected.
$\overline{\text{MBIAEN}}$	127	O	Burned-in address enable. $\overline{\text{MBIAEN}}$ is an output signal used to provide an output enable for the ROM containing the adapter's burned-in address (BIA). H = This signal is driven high for any write accesses to the addresses between >00.0000 and >00.000F, or any accesses (read/write) to any other address. L = This signal is driven low for any read from addresses between >00.0000 and >00.000F.
$\overline{\text{MBRQ}}$	17	I/O	Reserved; must be pulled high (see Note 3).

† I = input, O = output

NOTE 3: Each pin must be individually tied to V_{CC} with a 1-kΩ pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
$\overline{\text{MCAS}}$	141	O	Column-address strobe for DRAMs. $\overline{\text{MCAS}}$ is valid for the 3/16 of the memory cycle following the row-address portion of the cycle. $\overline{\text{MCAS}}$ is driven low every memory cycle while the column address is valid on MADL0–MADL7, MAXPH, and MAXPL, except when one of the following conditions occurs: 1) When the address accessed is in the BIA ROM (>00.0000 – >00.000F) 2) When the address accessed is in the EPROM memory map (i.e., when the BOOT bit in the SIFACL register is zero and an access is made between >00.0010 – >00.FFFF or >1F.0000 – >1F.FFFF) 3) When the cycle is a refresh cycle, in which case $\overline{\text{MCAS}}$ is driven at the start of the cycle before $\overline{\text{MRAS}}$ (for DRAMs that have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh). For DRAMs that do not support $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, it may be necessary to disable $\overline{\text{MCAS}}$ with MREF during the refresh cycle.
MDDIR	138	I/O	Data direction. MDDIR is used as a direction control for bidirectional bus drivers. This signal becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TI380C27 memory-bus write L = TI380C27 memory-bus read
$\overline{\text{MOE}}$	3	O	Memory output enable. $\overline{\text{MOE}}$ is used to enable the outputs of the DRAM memory during a read cycle. This signal is high for EPROM or BIA ROM read cycles. H = Disable DRAM outputs L = Enable DRAM outputs
$\overline{\text{MRAS}}$	143	O	Row-address strobe for DRAMs. The row address lasts for the first 5/16 of the memory cycle. $\overline{\text{MRAS}}$ is driven low every memory cycle while the row address is valid on MADL0–MADL7, MAXPH, and MAXPL for both RAM and ROM cycles. It is also driven low during refresh cycles when the refresh address is valid on MADL0–MADL7.
MREF	130	O	DRAM refresh cycle in progress. MREF is used to indicate that a DRAM refresh cycle is occurring. It is also used for disabling $\overline{\text{MCAS}}$ to all DRAMs that do not use a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. H = DRAM refresh cycle in process L = Not a DRAM refresh cycle
$\overline{\text{MRESET}}$	125	O	Memory-bus reset. $\overline{\text{MRESET}}$ is a reset signal generated when either the ARESET bit in the SIFACL register is set or $\overline{\text{SRESET}}$ is asserted. This signal is used for resetting external local-bus glue logic. H = External logic not reset L = External logic reset
$\overline{\text{MROMEN}}$	133	O	ROM enable. During the first 5/16 of the memory cycle, $\overline{\text{MROMEN}}$ is used to provide a chip select for ROMs when the BOOT bit of the SIFACL register is zero (i.e., when code is resident in ROM, not RAM). It can be latched by $\overline{\text{MAL}}$. It goes low for any read from addresses >00.0010 – >00.FFFF or >1F.0000 – >1F.FFFF when the BOOT bit in the SIFACL register is zero. $\overline{\text{MROMEN}}$ stays high for writes to these addresses, accesses of other addresses, or accesses of any address when the BOOT bit is 1. During the final three quarters of the memory cycle, $\overline{\text{MROMEN}}$ outputs the A13 address signal for interfacing to a BIA ROM. This means $\overline{\text{MBIAEN}}$, MAX0, $\overline{\text{ROMEN}}$, and MAX2 together form a glueless interface for the BIA ROM. H = ROM disabled L = ROM enabled

† I = input, O = output

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
$\overline{MW}$	142	O	Local-memory write. $\overline{MW}$ is used to specify a write cycle on the local-memory bus. The data on the MADH0 – MADH7 and MADL0 – MADL7 buses is valid while $\overline{MW}$ is low. DRAMs latch data on the falling edge of $\overline{MW}$, while SRAMs latch data on the rising edge of $\overline{MW}$. H = Not a local-memory write cycle L = Local-memory write cycle
$\overline{NMI}$	33	I	Nonmaskable interrupt request. $\overline{NMI}$ must be left unconnected.
OSCIN	135	I	External oscillator input. OSCIN provides the clock frequency to the TI380C27 for a 4-MHz or 6-MHz internal bus (see Note 5 and Note 6). CLKDIV OSCIN H 64 MHz for a 4-MHz local bus L 32 MHz for a 4-MHz local bus or 48 MHz for a 6-MHz local bus
OSCOUT	122	O	Oscillator output CLKDIV OSCOUT L OSCIN/4 (if OSCIN = 32 MHz, OSCOUT = 8 MHz; if OSCIN = 48 MHz, OSCOUT = 12 MHz H OSCIN/8 (if OSCIN = 64 MHz, then OSCOUT = 8 MHz)
PRTYEN	41	I	Parity enable. The value on PRTYEN is loaded into the PEN bit of the SIFACL register at reset (i.e., when $\overline{SRESET}$ is asserted or the ARESET bit in the SIFACL register is set) to form a default value. PRTYEN enables parity checking for the local memory. H = Local-memory data bus checked for parity (see Note 1) L = Local-memory data bus not checked for parity
NSELOUT0 NSELOUT1	40 119	O	Network selection outputs. NSELOUT0 and NSELOUT1 are controlled by the host through the corresponding bits of the SIFACL register. The value of these bits/signals can be changed only while the TI380C27 is reset. NSELOUT0 NSELOUT1 DESCRIPTION L L Full-duplex Ethernet L H 16-Mbps token ring H L Half-duplex Ethernet H H 4-Mbps token ring
SADH0 SADH1 SADH2 SADH3 SADH4 SADH5 SADH6 SADH7	97 96 95 94 93 92 86 85	I/O	System address/data bus — high byte (see Note 1).These lines make up the most significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADH0, and the least significant bit is SADH7. Address multiplexing: Bits 31 – 24 and bits 15 – 8 Data multiplexing: Bits 15 – 8
SADL0 SADL1 SADL2 SADL3 SADL4 SADL5 SADL6 SADL7	76 75 74 70 69 68 67 66	I/O	System address/data bus — low byte (see Note 1). These lines make up the least significant byte of each address word (32-bit address bus) and data word (16-bit data bus). The most significant bit is SADL0, and the least significant bit is SADL7. Address multiplexing: Bits 23 – 16 and bits 7 – 0 Data multiplexing: Bits 7 – 0

† I = input, O = output

NOTES: 1 Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads).
5. Pin has an expanded input voltage specification.
6. A maximum of two TI380C27 devices may be connected to any one oscillator.

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION	
SALE	64	O	System address-latch enable. SALE is the enable pulse used to externally latch the 16 LSBs of the address from the SADH0 – SADH7 and SADL0 – SADL7 buses at the start of the DMA cycle. Systems that implement address parity can also externally latch the parity bits (SPH and SPL) for the latched address.	
$\overline{\text{SBBSY}}$	50	I	System bus busy. The TI380C27 samples the value on $\overline{\text{SBBSY}}$ during arbitration (see Note 1). The sample has one of two values: H = Not busy. The TI380C27 can become bus master if the grant condition is met. L = Busy. The TI380C27 cannot become bus master.	
SBCLK	65	I	System bus clock. The TI380C27 requires SBCLK to synchronize its bus timings for all DMA transfers. Valid frequencies are 2 MHz – 33 MHz.	
$\overline{\text{SBHE}}$/SRNW	79	I/O	Intel Mode	$\overline{\text{SBHE}}$ is used for system byte high enable. $\overline{\text{SBHE}}$ is a 3-state output driven during DMA; it is an input at all other times. H = System byte high not enabled (see Note 1) L = System byte high enabled
			Motorola Mode	SRNW is used for system read not write. SRNW serves as a control signal to indicate a read or write cycle. H = Read cycle (see Note 1) L = Write cycle
$\overline{\text{SBRLS}}$	49	I	System bus release. $\overline{\text{SBRLS}}$ indicates to the TI380C27 that a higher-priority device requires the system bus. The value on $\overline{\text{SBRLS}}$ is ignored when the TI380C27 is not perfoming DMA. $\overline{\text{SBRLS}}$ is internally synchronized to SBCLK. H = The TI380C27 can hold onto the system bus (see Note 1). L = The TI380C27 should release the system bus upon completion of current DMA cycle. If the DMA transfer is not yet complete, the SIF rearbitrates for the system bus.	
$\overline{\text{SCS}}$	48	I	System chip select. $\overline{\text{SCS}}$ activates the system interface of the TI380C27 for a DIO read or write. H = Not selected (see Note 1) L = Selected	
$\overline{\text{SDBEN}}$	80	O	System data-bus enable. $\overline{\text{SDBEN}}$ signals to the external data buffers to begin driving data. $\overline{\text{SDBEN}}$ is activated during both DIO and DMA. H = Keep external data buffers in the high-impedance state L = Cause external data buffers to begin driving data	
SDDIR	59	O	System data direction. SDDIR provides to the external data buffers a signal indicating the direction the data is moving. During DIO writes and DMA reads, SDDIR is low (data direction is into the TI380C27). During DIO reads and DMA writes, SDDIR is high (data direction is out from the TI380C27). When the system interface is not involved in a DIO or DMA operation, SDDIR is high by default. SDDIR: H / L DATA DIRECTION: output / input DIO: read / write DMA: write / read	

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

ADVANCE INFORMATION

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION	
SHLDA/$\overline{\text{SBGR}}$	58	I	Intel Mode	SHLDA is used for system hold acknowledge. SHLDA indicates that the system DMA hold request has been acknowledged. It is internally synchronized to SBCLK (see Note 1). H = Hold request acknowledged L = Hold request not acknowledged
			Motorola Mode	$\overline{\text{SBGR}}$ is used for system bus grant. $\overline{\text{SBGR}}$ is an active-low bus grant, as defined in the standard 68xxx interface, and is internally synchronized to SBCLK (see Note 1). H = System bus not granted L = System bus granted
SHRQ/$\overline{\text{SBRQ}}$	78	O	Intel Mode	SHRQ is used for system hold request. SHRQ is used to request control of the system bus in preparation for a DMA transfer. SHRQ is internally synchronized to SBCLK. H = System bus requested L = System bus not requested
			Motorola Mode	$\overline{\text{SBRQ}}$ is used for system bus request. SBRQ is used to request control of the system bus in preparation for a DMA transfer. SBRQ is internally synchronized to SBCLK. H = System bus not requested L = System bus requested
$\overline{\text{SIACK}}$	43	I	System interrupt acknowledge. $\overline{\text{SIACK}}$ is from the host processor to acknowledge the interrupt request from the TI380C27. H = System interrupt not acknowledged (see Note 1) L = System interrupt acknowledged: The TI380C27 places its interrupt vector onto the system bus.	
SI/$\overline{\text{M}}$	56	I	System Intel/Motorola mode select. The value on SI/$\overline{\text{M}}$ specifies the system-interface mode. H = Intel-compatible interface mode selected. Intel interface can be 8-bit or 16-bit mode (see S8/$\overline{\text{SHALT}}$ description and Note 1). L = Motorola-compatible interface mode selected. Motorola interface mode is always 16 bits.	
SINTR/$\overline{\text{SIRQ}}$	57	O	Intel Mode	SINTR is used for system-interrupt request. TI380C27 activates SINTR to signal an interrupt request to the host processor. H = Interrupt request by TI380C27 L = No interrupt request
			Motorola Mode	$\overline{\text{SIRQ}}$ is used for system-interrupt request. TI380C27 activates $\overline{\text{SIRQ}}$ to signal an interrupt request to the host processor. H = No interrupt request L = Interrupt request by TI380C27
$\overline{\text{SOWN}}$	81	O	System bus owned. $\overline{\text{SOWN}}$ indicates to external devices that TI380C27 has control of the system bus. $\overline{\text{SOWN}}$ drives the enable signal of the bus transceiver chips that drive the address and bus-control signals. H = TI380C27 does not have control of the system bus. L = TI380C27 has control of the system bus.	
SPH	84	I/O	System parity high. The optional odd-parity bit for each address or data byte transmitted over SADH0–SADH7 (see Note 1).	
SPL	77	I/O	System parity low. The optional odd-parity bit for each address or data byte transmitted over SADL0–SADL7 (see Note 1).	

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†		DESCRIPTION
SRAS/$\overline{\text{SAS}}$	60	I/O	Intel Mode	SRAS is used for system memory-address strobe (see Note 7). SRAS is used to latch the $\overline{\text{SCS}}$ and SRSX – SRS2 register input signals. In a minimum-chip system, SRAS is tied to the SALE output of the system bus. The latching capability can be defeated since the internal latch for these inputs remains transparent as long as SRAS remains high. This permits SRAS to be pulled high and the signals at $\overline{\text{SCS}}$, SRSX – SRS2, and $\overline{\text{SBHE}}$ to be applied independently of the SALE strobe from the system bus. During DMA, SRAS remains an input. H = Transparent mode L = Holds latched values of $\overline{\text{SCS}}$, SRSX – SRS2, and $\overline{\text{SBHE}}$ Falling edge = Latches $\overline{\text{SCS}}$, SRSX – SRS2, and $\overline{\text{SBHE}}$
			Motorola Mode	$\overline{\text{SAS}}$ is used for sytem-memory address strobe (see Note 7). $\overline{\text{SAS}}$ is an active-low address strobe that is an input during DIO (although ignored as an address strobe) and an output during DMA. H = Address is not valid. L = Address is valid and a transfer operation is in progress.
$\overline{\text{SRD}}$/$\overline{\text{SUDS}}$	83	I/O	Intel Mode	$\overline{\text{SRD}}$ is used for system read strobe (see Note 7). $\overline{\text{SRD}}$ is the active-low strobe indicating that a read cycle is performed on the system bus. $\overline{\text{SRD}}$ is an input during DIO and an output during DMA. H = Read cycle is not occurring. L = If DMA, host provides data to system bus. If DIO, SIF provides data to system bus.
			Motorola Mode	$\overline{\text{SUDS}}$ is used for upper-data strobe (see Note 7). $\overline{\text{SUDS}}$ is the active-low upper-data strobe. $\overline{\text{SUDS}}$ is an input during DIO and an output during DMA. H = Not valid data on SADH0 – SADH7 lines L = Valid data on SADH0 – SADH7 lines
$\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$	82	I/O	Intel Mode	$\overline{\text{SRDY}}$ is used for system bus ready (see Note 7). $\overline{\text{SRDY}}$ indicates to the bus master that a data transfer is complete. $\overline{\text{SRDY}}$ is asynchronous but during DMA and pseudo-DMA cycles, it is internally synchronized to SBCLK. During DMA cycles, $\overline{\text{SRDY}}$ must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. $\overline{\text{SRDY}}$ is an output when the TI380C27 is selected for DIO; otherwise, it is an input. H = System bus is not ready. L = Data transfer is complete; system bus is ready.
			Motorola Mode	$\overline{\text{SDTACK}}$ is used for system data-transfer acknowledge (see Note 7). The purpose of $\overline{\text{SDTACK}}$ is to indicate to the bus master that a data transfer is complete. $\overline{\text{SDTACK}}$ is internally synchronized to SBCLK. During DMA cycles, $\overline{\text{SDTACK}}$ must be asserted before the falling edge of SBCLK in state T2 in order to prevent a wait state. $\overline{\text{SDTACK}}$ is an output when the TI380C27 is selected for DIO; otherwise, it is an input. H = System bus is not ready. L = Data transfer is complete; system bus is ready.
$\overline{\text{SRESET}}$	44	I	System reset. $\overline{\text{SRESET}}$ is activated to place the TI380C27 into a known initial state. Hardware reset puts most of the TI380C27 outputs into the high-impedance state and place all blocks into the reset state. The Intel mode DMA bus-width selection (S8) is latched on the rising edge of $\overline{\text{SRESET}}$. H = No system reset L = System reset Rising edge = Latch bus width for DMA operations (for Intel-mode applications)	

† I = input, O = output

NOTE 7: Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.

ADVANCE INFORMATION

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†		DESCRIPTION
SRSX SRS0 SRS1 SRS2/$\overline{\text{SBERR}}$	47 46 45 54	I	Intel Mode	SRSX and SRS0–SRS2 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS2 (see Note 1). MSb LSb Register selected = SRSX SRS0 SRS1 SRS2/$\overline{\text{SBERR}}$
			Motorola Mode	SRSX, SRS0 and SRS1 are used for system-register select. These inputs select the word or byte to be transferred during a system DIO access. The most significant bit is SRSX and the least significant bit is SRS1 (see Note 1). MSb LSb Register selected = SRSX SRS0 SRS1 $\overline{\text{SBERR}}$ is used for bus error. $\overline{\text{SBERR}}$ corresponds to the bus-error signal of the 68xxx microprocessor. $\overline{\text{SBERR}}$ is internally synchronized to SBCLK. This input is driven low during a DMA cycle to indicate to the TI380C27 that the cycle must be terminated, (see Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information).
$\overline{\text{SWR}}$/$\overline{\text{SLDS}}$	61	I/O	Intel Mode	$\overline{\text{SWR}}$ is used for system-write strobe (see Note 7). $\overline{\text{SWR}}$ is an active-low write strobe that is an input during DIO and an output during DMA. H = Write cycle is not occurring. L = If DMA, data to be driven from SIF to host bus. If DIO, on the rising edge, the data is latched and written to the selected register.
			Motorola Mode	$\overline{\text{SLDS}}$ is used for lower-data strobe (see Note 7). $\overline{\text{SLDS}}$ is an input during DIO and an output during DMA. H = Not valid data on SADL0–SADL7 lines L = Valid data on SADL0–SADL7 lines
SXAL	63	O		System-extended-address latch. SXAL provides the enable pulse used to externally latch the most significant 16 bits of the 32-bit system address during DMA. SXAL is activated prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carry out of the lower 16 bits). Systems that implement parity on addresses can use SXAL to externally latch the parity bits (available on SPL and SPH) for the DMA address extension.
$\overline{\text{SYNCIN}}$	136	I		Reserved. $\overline{\text{SYNCIN}}$ must be left unconnected (see Note 1).
S8/$\overline{\text{SHALT}}$	51	I	Intel Mode	S8 is used for system 8/16-bit bus select. S8 selects the bus width used for communications through the system interface. On the rising edge of $\overline{\text{SRESET}}$, the TI380C27 latches the DMA bus width; otherwise, the value on S8 dynamically selects the DIO bus width. H = Selects 8-bit mode (see Note 1) L = Selects 16-bit mode
			Motorola Mode	$\overline{\text{SHALT}}$ is used for system halt/bus error retry. If $\overline{\text{SHALT}}$ is asserted along with $\overline{\text{SBERR}}$, the adapter retries the last DMA cycle. This is the rerun operation as defined in the 68xxx specification. The BERETRY counter is not decremented by $\overline{\text{SBERR}}$ when $\overline{\text{SHALT}}$ is asserted (see Section 3.4.5.3 of the *TMS380 Second-Generation Token Ring User's Guide* (SPWU005) for more information).

† I = input, O = output

NOTES: 1. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).
7. Pin should be tied to V_{CC} with a 4.7-kΩ pullup resistor.

Pin Functions (Continued)

Network Media Interface — Token-Ring Mode (TEST1 = H, TEST2 = H)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
DRVR DRVR	115 114	O	Differential-driver data output. DRVR and DRVR are the differential outputs that send the TI380C27 transmit data to the TMS38054 for driving onto the ring-transmit-signal pair.
FRAQ	111	O	Frequency-acquisition control. FRAQ determines the use of frequency- or phase-acquisition mode in the TMS38054. H = Wide range. Frequency centering to PXTALIN by TMS38054. L = Narrow range. Phase lock onto the incoming data (RCVINA and RCVINB) by the TMS38054.
NSRT	112	O	Insert-control signal to the TMS38054. NSRT enables the phantom-driver outputs (PHOUTA and PHOUTB) of the TMS38054, through the watchdog timer, for insertion onto the token ring. Static high = Inactive, phantom current removed (due to watchdog timer) Static low = Inactive, phantom current removed (due to watchdog timer) NSRT low and pulsed high = Active, current output on PHOUTA and PHOUTB
PXTALIN	118	I	Ring-interface clock-frequency control (see Note 5). At 16-Mbps ring speed, PXTALIN must be supplied a 32-MHz signal. At 4-Mbps ring speed, PXTALIN must be 8 MHz and can be the output from OSCOUT.
RCLK	120	I	Ring-interface recovered clock (see Note 5). RCLK is the clock recovered by the TMS38054 from the token-ring received data. For 16-Mbps operation, RCLK is a 32-MHz clock; for 4-Mbps operation, RCLK is an 8-MHz clock.
RCVR	121	I	Ring-interface received data (see Note 5). RCVR contains the data received by the TMS38054 from the token ring.
REDY	110	I	Ring-interface ready. REDY indicates the presence of received data as monitored by the TMS38054 energy-detect capacitor. H = Not ready. Ignore received data. L = Ready. Received data.
WFLT	113	I	Wire-fault detect. WFLT is an input to the TI380C27 driven by the TMS38054. WFLT indicates a current imbalance of the TMS38054 PHOUTA and PHOUTB pins. H = No wire fault detected L = Wire fault detected
WRAP	116	O	Internal wrap select. WRAP is an output from the TI380C27 to the ring interface to activate an internal attenuated feedback path from the transmitted data (DRVR) to receive data (RCVR) signals for bring-up diagnostic testing. When active, the TMS38054 also cuts off the current drive to the transmission pair. H = Normal ring operation L = Transmit data drives receive data (loopback)

† I = input, O = output

NOTE 5: Pin has an expanded input voltage specification.

ADVANCE INFORMATION

Pin Functions (Continued)

Network-Media Interface — Ethernet Mode (TEST1 = L, TEST2 = H)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
DRVR DRVR	115 114	O	DRVR and DRVR have no Ethernet function and should be left unconnected.
TXD	111	O	Ethernet transmit data. TXD provides the Ethernet PHY-layer circuitry with a bit-rate from the TI380C27. Data is output synchronously TXC. TXD is normally connected to TXD of an Ethernet serial network interface (SNI) chip.
LPBK	112	O	Loopback. LPBK enables loopback of Ethernet transmit data through the Ethernet (SNI) device to receive data. H = Wrap through the front-end device L = Normal operation
TXC	118	I	Ethernet transmit clock. TXC is a 10-MHz clock input used to synchronize transmit data from the TI380C27 to the Ethernet PHY layer circuitry. TXC is a continuously running clock and is normally connected to the TXC output of an Ethernet SNI chip (see Note 5).
RXC	120	I	Ethernet receive clock. RXC is a 10-MHz clock input used to synchronize received data from the Ethernet PHY-layer circuitry to the TI380C27. RXC must be present whenever CRS is active (although it can be held low for a maximum of 16 clock cycles after the rising edge of CRS). When CRS is inactive, it is permissible to hold RXC low and is normally connected to the RXC output of an Ethernet SNI chip. The TI380C27 requires RXC to be maintained in the low state when CRS is not asserted (see Note 5).
RXD	121	I	Ethernet received data. RXD signal provides the TI380C27 with bit-rate network data from the Ethernet front-end device. Data must be synchronous with RXC and is normally connected to RXD of an Ethernet SNI chip (see Note 5).
CRS	110	I	Ethernet carrier sense. CRS indicates to the TI380C27 that the Ethernet PHY-layer circuitry has network data present on RXD. CRS is asserted (high) when the first bit of the frame is received and is deasserted after the last bit of the frame is received. H = Receiving data L = No data on network
COLL	113	I	Ethernet collision detect. COLL indicates to the TI380C27 that the Ethernet PHY-layer circuitry has detected a network collision. COLL must be present for at least two TXC clock cycles to ensure it is accepted by the TI380C27 and is normally connected to COLL of an Ethernet SNI chip. COLL can also be an indication of the SQE test signal. H = COLL detected by the SNI device L = Normal operation
TXEN	116	O	Ethernet transmit enable. TXEN indicates to the Ethernet PHY-layer circuitry that bit-rate data is present on TXD. TXEN is output synchronously to TXC and is normally connected to TXE of an Ethernet SNI chip. H = Data line currently contains data to be transmitted L = No valid data on TXEN

† I = input, O = output

NOTE 5: Pin has an expanded input voltage specification.

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
TEST0 TEST1 TEST2	103 102 101	I	Network select inputs. TEST0–TEST2 are used to select the network speed and type to be used by the TI380C27. These inputs should be changed only during adapter reset. Connect TEST2 to V_{DDL}. TEST0 TEST1 TEST2 DESCRIPTION L L H Full-duplex Ethernet L H H 16-Mbps token ring H L H Half-duplex Ethernet H H H 4-Mbps token ring X X L Reserved
TEST3 TEST4 TEST5	100 99 98	I	Test inputs. TEST3–TEST5 should be left unconnected (see Note 1). Module-in-place test mode is achieved by tying TEST3 and TEST4 to ground. In this mode, all TI380C27 outputs are in the high-impedance state. Internal pullups on all TI380C27 inputs are disabled (except TEST3–TEST5).
XFAIL	104	I	External fail-to-match signal. An enhanced-address-copy-option (EACO) device uses XFAIL to indicate to the TI380C27 that it should not copy the frame nor set the ARI/FCI bits in a token-ring frame due to an external address match.The ARI/FCI bits in a token-ring frame can be set due to an internal address-matched frame. If an EACO device is not used, XFAIL must be left unconnected. XFAIL is ignored when CAF mode is enabled [see table in XMATCH description (see Note 1)]. H = No address match by external address checker L = External address-checker-armed state
XMATCH	105	I	External match signal. An enhanced-address-copy-option (EACO) device uses XMATCH to indicate to the TI380C27 to copy the frame and set the ARI/FCI bits in a token-ring frame. If an EACO device is not used, XMATCH must be left unconnected. XMATCH is ignored when CAF mode is enabled (see Note 1). H = Address match recognized by external address checker L = External address-checker-armed state XMATCH XFAIL FUNCTION 0 0 Armed (processing frame data) 0 1 Do not externally match the frame (XFAIL takes precedence). 1 0 Copy the frame 1 1 Do not externally match the frame (XFAIL takes precedence). Hi-Z Hi-Z Reset state (adapter not initialized)
V_{DDL}	37 55 126	I	Positive-supply voltage for digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.
V_{DD}	106 137 9 34 72 89	I	Positive-supply voltage for output buffers. All V_{DD} pins must be attached to the common-system power-supply plane.
V_{SSC}	39 87 117 144	I	Ground reference for output buffers (clean ground). All V_{SSC} pins must be attached to the common-system ground plane.

† I = input, O = output

NOTE 1: Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch).

ADVANCE INFORMATION

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
V_{SSL}	2 36 52 53 73 108 128 129	I	Ground reference for input buffers. All V_{SSL} pins must be attached to the common-system ground plane.
V_{SS}	11 19 62 91 134	I	Ground connections for output buffers. All V_{SS} pins must be attached to system ground plane.
NC	1 10 35 71 88 90 107 109		These pins should be left unconnected.

† I = input, O = output

ADVANCE INFORMATION

architecture

The major blocks of the TI380C27 include the communications processor (CP), system interface (SIF), memory interface (MIF), protocol handler (PH), clock generator (CG), and adapter support function (ASF). The functionality of each block is described in the following sections.

communications processor (CP)

The CP performs the control and monitoring of the other functional blocks in the TI380C27. The control and monitoring protocols are specified by the software (downloaded or ROM based) in local memory. Available protocols include:

- Media access control (MAC) software
- Logical link control (LLC) software (token-ring mode only)
- Copy all frames (CAF) software

The CP is a proprietary 16-bit central processing unit (CPU) with data cache and a single prefetch pipe for pipelining of instructions. These features enhance the TI380C27's maximum performance capability to about 8 million instructions per second (MIPS), with an average of about 5 MIPS.

system interface (SIF)

The SIF performs the interfacing of the LAN subsystem to the host system. This interface may require additional logic depending on the application. The system interface can transfer information/data using any of these three methods:

- Direct memory access (DMA)
- Direct input/output (DIO)
- Pseudo-direct memory access (PDMA)

DMA (or PDMA) is used to transfer all data to/from host memory from/to local memory. The main uses of DIO are for loading the software to local memory and for initializing the TI380C27. DIO also allows command/status interrupts to occur to and from the TI380C27.

The system interface can be hardware selected for either of two modes by use of SI/$\overline{M}$. The mode selected determines the memory organizations and control signals used. These modes are:

- The Intel 80x8x families: 8-, 16-, and 32-bit bus devices
- The Motorola 68xxx microprocessor family: 16- and 32-bit bus devices

The system interface supports host-system memory addressing up to 32 bits (32-bit reach into the host-system memory). This allows greater flexibility in using/accessing host-system memory. System designers are allowed to customize the system interface to their particular bus by:

- Programmable burst transfers or cycle-steal DMA operations
- Optional parity protection

These features are implemented in hardware to reduce system overhead, facilitate automatic rearbitration of the bus after a burst, or repeat a cycle when errors occur (parity or bus). Bus retries are also supported.

The system-interface hardware also includes features to enhance the integrity of the TI380C27 and the data. These features include the following:

- Always internally maintain odd-byte parity regardless of parity being disabled
- Monitor for the presence of a clock failure
- Switchable SIF speeds of 2 MHz to 33 MHz

On every cycle, the system interface compares all the system clocks to a reference clock. If any of the clocks become invalid, the TI380C27 enters the slow-clock mode, which prevents latch-up of the TI380C27. If the SBCLK is invalid, any DMA cycle is terminated immediately; otherwise, the DMA cycle is completed and the TI380C27 is placed in the slow-clock mode.

system interface (SIF) (continued)

When the TI380C27 enters the slow-clock mode, the clock that failed is replaced by a slow free-running clock and the device is placed into a low-power reset state. When the failed clock(s) return to valid operation, the TI380C27 must be reinitialized.

For DMA with a 16-MHz clock, a continuous transfer rate of 64 megabits per second (8 Mbps) can be obtained. For DMA with a 25-MHz clock, a continuous transfer rate of 96 megabits per second (12 Mbps) can be obtained. For DMA with a 33 MHz clock, a continuous transfer rate of 128 megabits per second (16 Mbps) can be obtained.For 8-bit and 16-bit pseudo-DMA, the following data rates can be obtained:

LOCAL BUS SPEED	8-BIT PDMA	16-BIT PDMA
4 MHz	48 Mbps	64 Mbps
6 MHz	72 Mbps	96 Mbps

Since the main purpose of DIO is for downloading and initialization, the DIO transfer rate is not a significant issue.

memory interface (MIF)

The MIF performs the memory management to allow the TI380C27 to address 2M bytes in local memory. Hardware in the MIF allows the TI380C27 to be directly connected to DRAMs without additional circuitry. This glueless DRAM connection includes the DRAM refresh controller. The MIF also handles all internal bus arbitration between these blocks. When required, the MIF then arbitrates for the external bus.

The MIF is responsible for the memory mapping of the CPU of a task. The memory map of DRAMs, EPROMs, burned-in addresses (BIA), and external devices are appropriately addressed when required by the system interface, protocol handler, or for a DMA transfer.

The memory interface is capable of a 64-Mbps continuous transfer rate when using a 4-MHz local bus (64-MHz device crystal) and a 96-Mbps continuous transfer rate when using a 6-MHz local bus.

protocol handler (PH)

The PH performs the hardware-based real-time protocol functions for a token-ring or an Ethernet LAN. Network type is determined by TEST0–TEST2. Token-ring network is determined by software and can be either 16 Mbps or 4 Mbps. The Ethernet network can be either full duplex or half duplex. These speeds are not fixed by the hardware but by the software.

The PH converts the parallel-transmit data to serial-network data of the appropriate coding and converts the received serial data to parallel data. The PH data-management state machines direct the transmission/reception of data to/from local memory through the MIF. The PH's buffer-management state machines automatically oversee this process, directly sending/receiving linked lists of frames without CPU intervention.

The protocol handler contains many state machines that provide the following features:

- Transmit and receive frames
- Capture tokens (token ring)
- Provide token-priority controls (token ring)
- Automatic retry of frame transmissions after collisions (Ethernet)
- Implement the random exponential backoff algorithm (Ethernet)
- Manage the TI380C27 buffer memory
- Provide frame-address recognition (group, specific, functional, and multicast)
- Provide internal parity protection
- Control and verify the PHY-layer circuitry-interface signals

protocol handler (PH) (continued)

Integrity of the transmitted and received data is assured by cyclic redundancy checks (CRC), detection of network data violations, and parity on internal data paths. All data paths and registers are optionally parity protected to assure functional integrity.

adapter support function (ASF)

The ASF performs support functions not contained in the other blocks. The features are:

- The TI380C27 base timer
- Identification, management, and service of internal and external interrupts
- Test-pin mode control, including the unit-in-place mode for board testing
- Checks for illegal states, such as illegal opcodes and parity

clock generator (CG)

The CG performs the generation of all the clocks required by the other functional blocks, including the local memory-bus clocks (MBCLK1, MBCLK2). The CG also generates the reference timer used to sample all input clocks (SBCLK, OSCIN, RCLK, and PXTALIN). If no transition is detected within the period of the reference timer on any input clock signal, the CG places the TI380C27 into slow-clock mode. The frequency of the reference timer is in the range of 10 kHz – 100 kHz.

user-accessible hardware registers and TI380C27-internal pointers

The following tables show how to access internal data via pointers and how to address the registers in the host interface. The SIFACL register, which directly controls device operation, is described in detail. The adapter-internal pointers table on the following page is defined only after TI380C27 initialization and until the OPEN command is issued. These pointers are defined by the TI380C27 software (microcode), and this table describes the release 1.xx and 2.x software.

Adapter-Internal Pointers for Token Ring†

ADDRESS	DESCRIPTION
>00.FFF8‡	Pointer to software raw microcode level in chapter 0
>00.FFFA‡	Pointer to starting location of copyright notices. Copyright notices are separated by a >0A character and terminated by a >00 character in chapter 0.
>01.0A00	Pointer to burned-in address in chapter 1
>01.0A02	Pointer to software level in chapter 1
>01.0A04	Pointer to TI380C27 addresses in chapter 1: Pointer + 0 node address Pointer + 6 group address Pointer + 10 functional address
>01.0A06	Pointer to TI380C27 parameters in chapter 1: Pointer + 0 physical-drop number Pointer + 4 upstream neighbor address Pointer + 10 upstream physical-drop number Pointer + 14 last ring-poll address Pointer + 20 reserved Pointer + 22 transmit access priority Pointer + 24 source class authorization Pointer + 26 last attention code Pointer + 28 source address of the last received frame Pointer + 34 last beacon type Pointer + 36 last major vector Pointer + 38 ring status Pointer + 40 soft-error timer value Pointer + 42 ring-interface error counter Pointer + 44 local ring number Pointer + 46 monitor error code Pointer + 48 last beacon-transmit type Pointer + 50 last beacon-receive type Pointer + 52 last MAC frame correlator Pointer + 54 last beaconing-station UNA Pointer + 60 reserved Pointer + 64 last beaconing-station physical-drop number
>01.0A08	Pointer to MAC buffer (a special buffer used by the software to transmit adapter generated MAC frames) in chapter 1
>01.0A0A	Pointer to LLC counters in chapter 1: Pointer + 0 MAX_SAPs Pointer + 1 open SAPs Pointer + 2 MAX_STATIONs Pointer + 3 open stations Pointer + 4 available stations Pointer + 5 reserved
>01.0A0C	Pointer to 4-/16-Mbps word flag. If zero, the adapter is set to run at 4 Mbps. If nonzero, the adapter is set to run at 16 Mbps.
>01.0A0E	Pointer to total TI380C27 RAM found in 1K bytes in RAM allocation test in chapter 1

† This table describes the pointers for release 2.x of the TI380C27 software.
‡ This address valid only for microcode release 2.x

Adapter-Internal Pointers for Ethernet†

ADDRESS	DESCRIPTION
>00.FFF8‡	Software raw-microcode level in chapter 0
>00.FFFA‡	Pointer to starting location of copyright notices. Copyright notices are separated by a >0A character and terminated by a >00 character in chapter 0.
>01.0A00	Pointer to burned-in address in chapter 1
>01.0A02	Pointer to software level in chapter 1
>01.0A04	Pointer to TI380C27 addresses in chapter 1: Pointer + 0 node address Pointer + 6 group address Pointer + 10 functional address
>01.0A08	Pointer to MAC buffer (a special buffer used by the software to transmit adapter generated MAC frames) in chapter 1
>01.0A0A	Pointer to LLC counters in chapter 1: Pointer + 0 MAX_SAPs Pointer + 1 open SAPs Pointer + 2 MAX_STATIONs Pointer + 3 open stations Pointer + 4 available stations Pointer + 5 reserved
>01.0A0C	Pointer to 4-/16-Mbps word flag. If zero, the adapter is set to run at 4 Mbps. If nonzero, the adapter is set to run at 16 Mbps.
>01.0A0E	Pointer to total TI380C27 RAM found in 1K bytes in RAM allocation test in chapter 1

† This table describes the pointers for release 2.x of the TI380C27 software.
‡ This address valid only for microcode release 2.x

User-Access Hardware Registers

80x8x 16-BIT MODE: (SI/$\overline{M}$ = 1, S8/$\overline{SHALT}$ = 0)†						
WORD TRANSFERS			NORMAL MODE $\overline{SBHE}$ = 0 SRS2 = 0		PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = 0 SRS2 = 0	
BYTE TRANSFERS			$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0	$\overline{SBHE}$ = 0 SRS2 = 1	$\overline{SBHE}$ = 1 SRS2 = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

† $\overline{SBHE}$ = 1 and SRS2 = 1 are not defined.

80x8x 8-BIT MODE: (SI/$\overline{M}$ = 1, S8/$\overline{SHALT}$ = 1)					
SRSX	SRS0	SRS1	SRS2	NORMAL MODE $\overline{SBHE}$ = X	PSEUDO-DMA MODE ACTIVE $\overline{SBHE}$ = X
0	0	0	0	SIFDAT LSB	SDMADAT LSB
0	0	0	1	SIFDAT MSB	SDMADAT MSB
0	0	1	0	SIFDAT/INC LSB	DMALEN LSB
0	0	1	1	SIFDAT/INC MSB	DMALEN MSB
0	1	0	0	SIFADR LSB	SDMAADR LSB
0	1	0	1	SIFADR MSB	SDMAADR MSB
0	1	1	0	SIFSTS	SDMAADX LSB
0	1	1	1	SIFCMD	SDMAADX MSB
1	0	0	0	SIFACL LSB	SIFACL LSB
1	0	0	1	SIFACL MSB	SIFACL MSB
1	0	1	0	SIFADR LSB	SIFADR LSB
1	0	1	1	SIFADR MSB	SIFADR MSB
1	1	0	0	SIFADX LSB	SIFADX LSB
1	1	0	1	SIFADX MSB	SIFADX MSB
1	1	1	0	DMALEN LSB	DMALEN LSB
1	1	1	1	DMALEN MSB	DMALEN MSB

68xxx MODE: (SI/$\overline{M}$ = 0)‡						
WORD TRANSFERS			NORMAL MODE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0		PSEUDO-DMA MODE ACTIVE $\overline{SUDS}$ = 0 $\overline{SLDS}$ = 0	
BYTE TRANSFERS			$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0	$\overline{SUDS}$ = 0 $\overline{SLDS}$ = 1	$\overline{SUDS}$ = 1 $\overline{SLDS}$ = 0
SRSX	SRS0	SRS1				
0	0	0	SIFDAT MSB	SIFDAT LSB	SDMADAT MSB	SDMADAT LSB
0	0	1	SIFDAT/INC MSB	SIFDAT/INC LSB	DMALEN MSB	DMALEN LSB
0	1	0	SIFADR MSB	SIFADR LSB	SDMAADR MSB	SDMAADR LSB
0	1	1	SIFCMD	SIFSTS	SDMAADX MSB	SDMAADX LSB
1	0	0	SIFACL MSB	SIFACL LSB	SIFACL MSB	SIFACL LSB
1	0	1	SIFADR MSB	SIFADR LSB	SIFADR MSB	SIFADR LSB
1	1	0	SIFADX MSB	SIFADX LSB	SIFADX MSB	SIFADX LSB
1	1	1	DMALEN MSB	DMALEN LSB	DMALEN MSB	DMALEN LSB

‡ 68xxx mode is always 16 bit.

ADVANCE INFORMATION

SIF adapter-control register (SIFACL)

The SIFACL register allows the host processor to control and to some extent reconfigure the TI380C27 under software control.

SIFACL Register

Bit #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	TEST0	TEST1	TEST2	—	SWHLDA	SWDDIR	SWHRQ	PSDMAEN	ARESET	CPHALT	BOOT	LBP	SINTEN	PEN	NSEL OUT0	NSEL OUT1
	R	R	R		RP – 0	R – u	R – 0	RS – 0	RW – 0	RP – b	RP – b	RW – 0	RW – 1	RP – p	RP – 0	RP – 1

Legend:

R	=	Read
W	=	Write
P	=	Write during ARESET = 1 only
S	=	Set only
– n	=	Value after reset
b	=	Value on BTSTRP
p	=	Value on PRTYEN
u	=	Indeterminate

Bits 0 – 2: Value on TEST0 – TEST2 pins

These bits are read only and always reflect the value on the corresponding device pins. This allows the host S/W to determine the network type and speed configuration. If the network speed and type are software configurable, these bits can be used to determine which configurations are supported by the network hardware.

TEST0	TEST1	TEST2	Description
L	L	H	Full-duplex Ethernet
L	H	H	16-Mbps token ring
H	L	H	Half-duplex Ethernet
H	H	H	4-Mbps token ring
X	X	L	Reserved

Bit 3: **Reserved.** Read data is indeterminate.

Bit 4: SWHLDA — Software Hold Acknowledge

This bit allows the function of SHLDA/$\overline{\text{SBGR}}$ to be emulated from software control for pseudo-DMA mode.

PSDMAEN	SWHLDA	SWHRQ	RESULT
0†	X	X	SWHLDA value in the SIFACL register cannot be set to a one.
1†	0	0	No pseudo-DMA request pending
1†	0	1	Indicates a pseudo-DMA request interrupt
1†	1	X	Pseudo-DMA process in progress

† The value on SHLDA/$\overline{\text{SBGR}}$ is ignored.

ADVANCE INFORMATION

SIF adapter-control register (SIFACL) (continued)

Bit 5: SWDDIR — Current SDDIR Signal Value

This bit contains the current value of the pseudo-DMA direction. This enables the host to easily determine the direction of DMA transfers, which allows system DMA to be controlled by system software.

0 = Pseudo DMA from host system to TI380C27
1 = Pseudo DMA from TI380C27 to host system

Bit 6: SWHRQ — Current SHRQ Signal Value

This bit contains the current value on SHRQ/$\overline{\text{SBRQ}}$ when in Intel mode, and the inverse of the value on SHRQ/$\overline{\text{SBRQ}}$ in Motorola mode. This enables the host to easily determine if a pseudo-DMA transfer is requested.

	INTEL MODE (SI/$\overline{\text{M}}$ = H)	MOTOROLA MODE (SI/$\overline{\text{M}}$ = L)
0 =	System bus not requested	System bus not requested
1 =	System bus requested	System bus requested

Bit 7: PSDMAEN — Pseudo-System-DMA Enable

This bit enables pseudo-DMA operation.

0 = Normal bus-master DMA operation is possible.
1 = Pseudo-DMA operation selected. Operation dependent on the values of SWHLDA and SWHRQ bits in the SIFACL register.

Bit 8: ARESET — Adapter Reset

This bit is a hardware reset of the TI380C27. This bit has the same effect as $\overline{\text{SRESET}}$ except that the DIO interface to the SIFACL register is maintained. This bit is set to 1 if a clock failure is detected (OSCIN, PXTALIN, RCLK, or SBCLK not valid).

0 = The TI380C27 operates normally.
1 = The TI380C27 is held in the reset condition.

Bit 9: CPHALT — Communications-Processor Halt

This bit controls TI380C27's processor access to the internal TI380C27 buses. This prevents the TI380C27 from executing instructions before the microcode has been downloaded.

0 = The TI380C27 processor can access the internal TI380C27 buses.
1 = The TI380C27 processor is prevented from accessing the internal adapter buses.

Bit 10: BOOT — Bootstrap CP Code

This bit indicates whether the memory in chapters 0 and 31 of the local-memory space is RAM or ROM/PROM/EPROM. This bit controls the operation of $\overline{\text{MCAS}}$ and $\overline{\text{MROMEN}}$.

0 = ROM/PROM/EPROM memory in chapters 0 and 31
1 = RAM memory in chapters 0 and 31

SIF adapter-control register (SIFACL) (continued)

Bit 11: LBP – Local-Bus Priority

This bit controls the priority levels of devices on the local bus.

0 = No external devices (such as the TI380FPA) are used with the TI380C27.
1 = An external device (such as the TI380FPA) is used with the TI380C27. This allows the external bus master to operate at the necessary priorities on the local bus.

If the system uses the TMS380SRA only, the bit must be set to 0. If the system uses both the TMS380SRA and the TI380FPA, this bit must be set to 1.

Bit 12: SINTEN — System-Interrupt Enable

This bit allows the host processor to enable or disable system-interrupt requests from the TI380C27. The system-interrupt request from the TI380C27 is on SINTR/$\overline{\text{SIRQ}}$. The following equation shows how SINTR/$\overline{\text{SIRQ}}$ is driven. The table also explains the results of the states.

SINTR/$\overline{\text{SIRQ}}$ = (PSDMAEN * SWHRQ * !SWHLDA) + (SINTEN * SYSTEM_INTERRUPT)

PSDMAEN	SWHRQ	SWHLDA	SINTEN	SYSTEM INTERRUPT (SIFSTS REGISTER)	RESULT
1†	1	1	X	X	Pseudo DMA is active.
1†	1	0	X	X	The TI380C27 generated a system interrupt for a pseudo DMA.
1†	0	0	X	X	Not a pseudo-DMA interrupt.
X	X	X	1	1	The TI380C27 generates a system interrupt.
0	X	X	1	0	The TI380C27 does not generate a system interrupt.
0	X	X	0	X	The TI380C27 cannot generate a system interrupt.

† The value on SHLDA/$\overline{\text{SBGR}}$ is ignored.

Bit 13: PEN — Parity Enable

This bit determines whether data transfers within the TI380C27 are checked for parity.

0 = Data transfers are not checked for parity.
1 = Data transfers are checked for correct odd parity.

Bit 14 – 15: NSELOUT0, NSELOUT0 1 — Network-Selection Outputs

The values in these bits control NSELOUT0 and NSELOUT1. These bits can be modified only while the ARESET bit is set.

These bits can be used to software configure a multiprotocol TI380C27 as follows: NSELOUT0 and NSELOUT1 should be connected to TEST0 and TEST1, respectively (TEST2 should be left unconnected or tied high). NSELOUT0 is used to select network speed and NSELOUT1 is used to select network type as shown in the table below:

NSELOUT0	NSELOUT1	SELECTION
0	0	Full-duplex Ethernet
0	1	16-Mbps token ring
1	0	Half-duplex Ethernet
1	1	4-Mbps token ring

At power up, these bits are set corresponding to 16-Mbps token ring (NSELOUT1 = 1, NSELOUT0 = 0).

ADVANCE INFORMATION

SIFACL control for pseudo-DMA operation

Pseudo DMA is software controlled by the use of five bits in the SIFACL register. The logic model for the SIFACL register control of pseudo-DMA operation is shown in Figure 2.

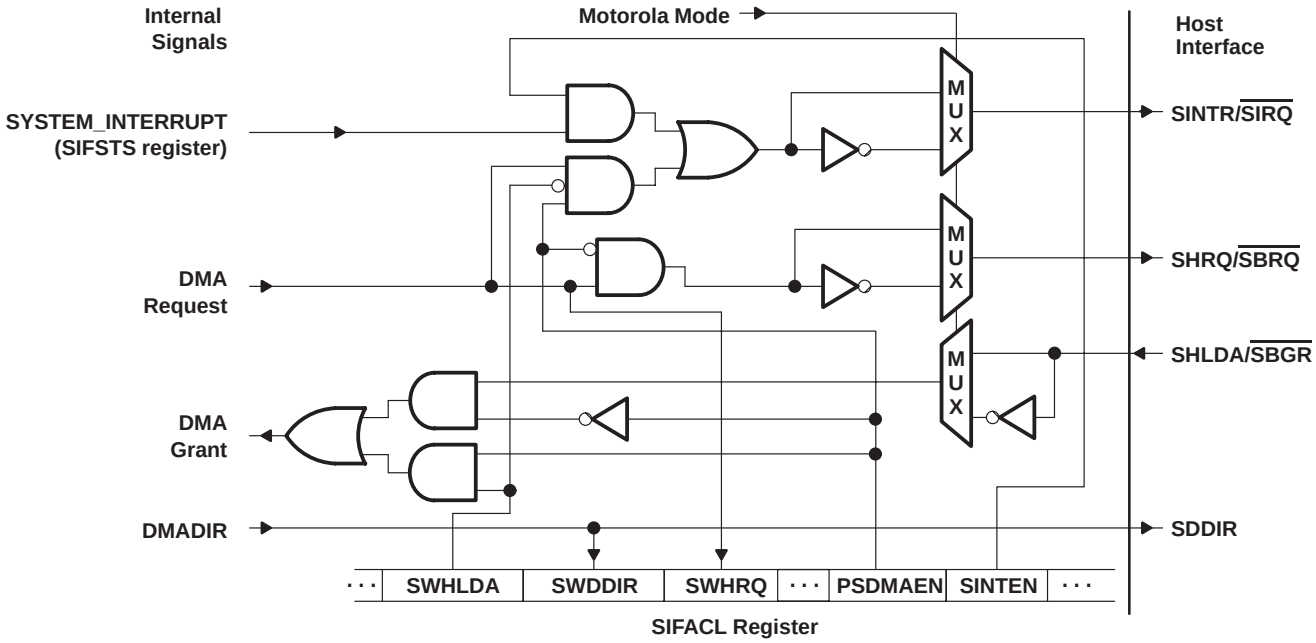


Figure 2. Pseudo-DMA Logic Related to SIFACL Bits

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 8) . . . . . 7 V
Input voltage range (see Note 8) . . . . . – 0.3 V to 20 V
Output voltage range . . . . . – 2 V to 7 V
Power dissipation . . . . . 0.9 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 8: Voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage (see Note 9)		0	0	0	V
V_{IH}	High-level input voltage	TTL-level signal	2		V_{DD}+0.3	V
		OSCIN	2.4		V_{DD}+0.3	
		RCLK, PXTALIN, RCVR	2.6		V_{DD}+0.3	
V_{IL}	Low-level input voltage, TTL-level signal (see Note 10)		–0.3		0.8	V
I_{OH}	High-level output current				–400	µA
I_{OL}	Low-level output current (see Note 11)				2	mA
T_A	Operating free-air temperature		0		70	°C
T_C	Operating case temperature				100	°C

NOTES: 9. All V_{SS} pins should be routed to minimize inductance to system ground.
10. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
11. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 12)	V_{DD} = MIN,	I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OL} = MAX			0.6	V
I_O	High-impedance output current	V_{DD} = MAX,	V_O = 2.4 V			20	µA
		V_{DD} = MAX,	V_O = 0.4 V			– 20	
I_I	Input current, any input or input/output	V_I = V_{SS} to V_{DD}				± 20	µA
I_{DD}	Supply current	V_{DD} = MAX				160	mA
I_{SCM}	Supply current, slow-clock mode	V_{DD} = 5 V			3		mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V			15	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V			15	pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.

NOTE 12: The following signals require an external pullup resistor: SRAS/$\overline{SAS}$, $\overline{SRDY}$/SDTACK, $\overline{SRD}$/SUDS, $\overline{SWR}$/SLDS, $\overline{EXTINT0}$–$\overline{EXTINT3}$, and $\overline{MBRQ}$.

ADVANCE INFORMATION

timing parameters

The timing parameters for all the signals of TI380C27 are shown in the following tables and are illustrated in the accompanying figures. The purpose of these figures and tables is to quantify the timing relationships among the various signals. The parameters are numbered for convenience.

static signals

The following table lists signals that are not allowed to change dynamically and therefore have no timing associated with them. They should be strapped high, low, or left unconnected as required.

SIGNAL	FUNCTION
SI/$\overline{M}$	Host-processor select (Intel/Motorola)
CLKDIV	Reserved
BTSTRP	Default bootstrap mode (RAM/ROM)
PRTYEN	Default parity select (enabled/disabled)
TEST0	Test terminal indicates network type
TEST1	Test terminal indicates network type
TEST2	Test terminal indicates network type
TEST3	Test terminal for TI manufacturing test †
TEST4	Test terminal for TI manufacturing test †
TEST5	Test terminal for TI manufacturing test †

† For unit-in-place test

timing parameter symbology

Some timing parameter symbols have been created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the signal names and other related terminology have been abbreviated as shown below:

DR	DRVR	RS	$\overline{\text{SRESET}}$
DRN	$\overline{\text{DRVR}}$	VDD	V_{DDL}, V_{DD}
OSC	OSCIN		
SCK	SBCLK		

Lower case subscripts are defined as follows:

c	cycle time	r	rise time
d	delay time	sk	skew
h	hold time	su	setup time
w	pulse duration (width)	t	transition time

The following additional letters and phrases are defined as follows:

H	High	Z	High impedance
L	Low	Falling edge	No longer high
V	Valid	Rising edge	No longer low

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

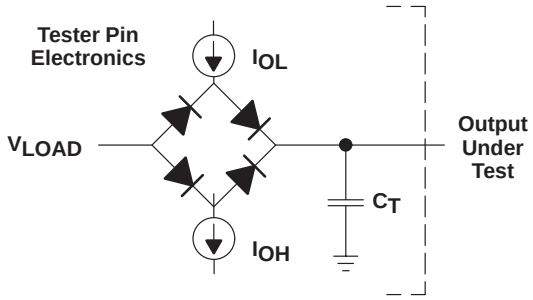
Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

Output transition times are specified as follows: For a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V, and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.

test measurement

The test-load circuit shown in Figure 3 represents the programmable load of the tester pin electronics that are used to verify timing parameters of TI380C27 output signals.



Where: I_{OL} = 2 mA, dc-level verification (all outputs)
I_{OH} = 400 μA (all outputs)
V_{LOAD} = 1.5 V, typical dc-level verification or 0.7 V, typical timing verification
C_T = 65 pF, typical load-circuit capacitance

Figure 3. Test-Load Circuit

ADVANCE INFORMATION

power up, SBCLK, OSCIN, MBCLK1, MBCLK2, $\overline{\text{SYNCIN}}$, and $\overline{\text{SRESET}}$ timing

NO.				MIN	NOM	MAX	UNIT
100†	$t_{r(VDD)}$	Rise time, 1.2 V to minimum V_{DD}-high level				1	ms
101†‡	$t_{d(VDDH-SCKV)}$	Delay time, minimum V_{DD}-high level to first valid SBCLK no longer high				1	ms
102†‡	$t_{d(VDDH-OSCV)}$	Delay time, minimum V_{DD}-high level to first valid OSCIN high				1	ms
103	$t_{c(SCK)}$	Cycle time, SBCLK (see Note 13)		30.3		500	ns
104	$t_{w(SCKH)}$	Pulse duration, SBCLK high		13		500	ns
105	$t_{w(SCKL)}$	Pulse duration, SBCLK low		13		500	ns
106†	$t_{t(SCK)}$	Transition time, SBCLK				2	ns
107	$t_{c(OSC)}$	Cycle time, OSCIN (see Note 14)			1/OSCIN		ns
108	$t_{w(OSCH)}$	Pulse duration, OSCIN high (see Note 15)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
109	$t_{w(OSCL)}$	Pulse duration, OSCIN low (see Note 15)	OSCIN = 64 MHz	5.5			ns
			OSCIN = 48 MHz	8			
			OSCIN = 32 MHz	8			
110†	$t_{t(OSC)}$	Transition time, OSCIN				3	ns
111†	$t_{d(OSCV-CKV)}$	Delay time, OSCIN valid to MBCLK1 and MBCLK2 valid				1	ms
117†	$t_{h(VDDH-RSL)}$	Hold time, $\overline{\text{SRESET}}$ low after V_{DD} reaches minimum high level		5			ms
118†	$t_{w(RSH)}$	Pulse duration, $\overline{\text{SRESET}}$ high		14			µs
119†	$t_{w(RSL)}$	Pulse duration, $\overline{\text{SRESET}}$ low		14			µs
288†	$t_{su(RST)}$	Setup time, DMA size to $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
289†	$t_{h(RST)}$	Hold time, DMA size from $\overline{\text{SRESET}}$ high (Intel mode only)		10			ns
	t_M	One-eighth of a local memory cycle	CLKDIV = H	$2t_{c(OSC)}$			ns
			CLKDIV = L	$t_{c(OSC)}$			

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.

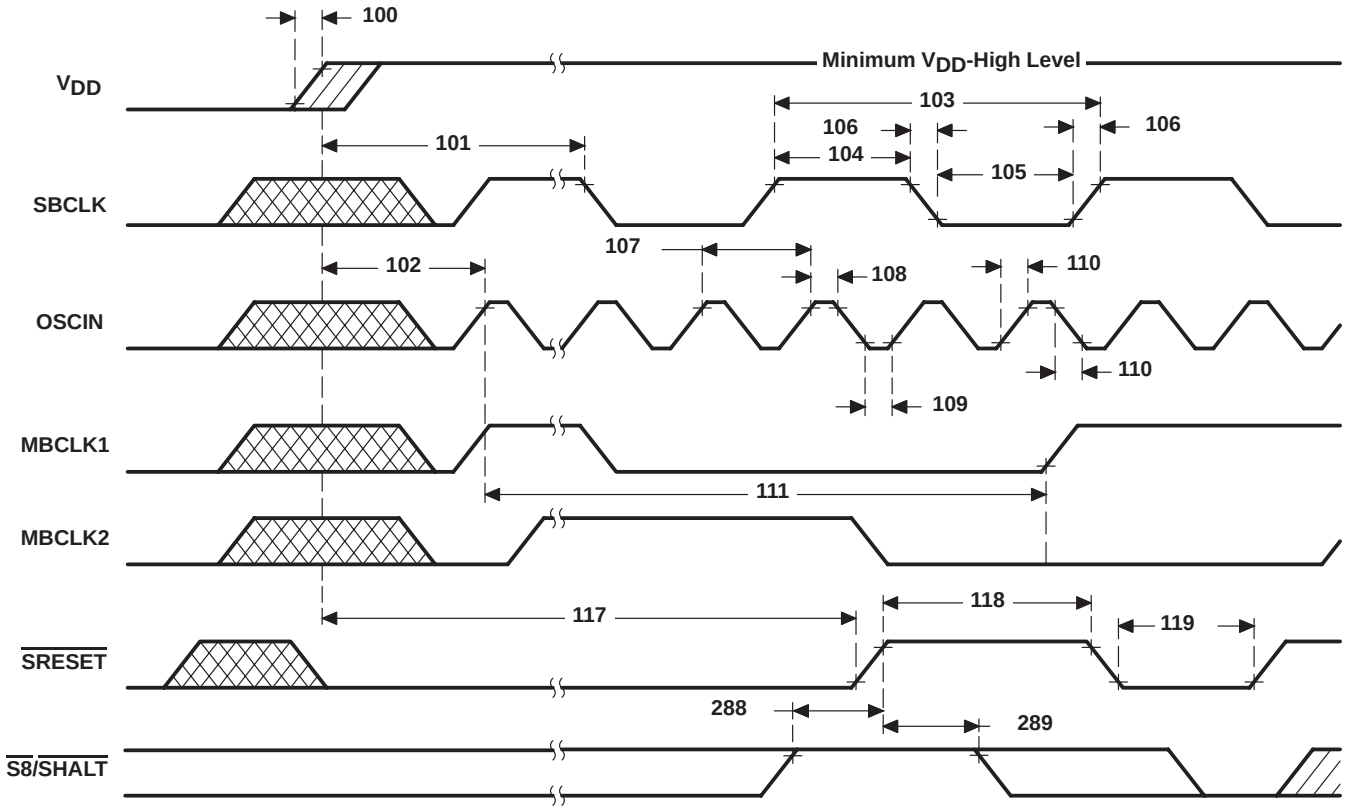
‡ If parameter 101 or 102 cannot be met, parameter 117 must be extended by the larger difference: real value of parameter 101 or 102 minus the max value listed.

NOTES: 13. SBCLK can be any value between 2 MHz to 33 MHz. This data sheet describes the system interface (SIF) timing parameters for the case of SBCLK at 25 MHz and at 33 MHz.

14. The value of OSCIN can be 64 MHz ± 1%, 32 MHz ± 1%, or 48 MHz ± 1%. If OSCIN is used to generate PXTALIN, the OSCIN tolerance must be ± 0.01%.

15. This is to assure a ±5% duty-cycle crystal, provided that OSCIN meets the recommended operating conditions for V_{IH} and V_{IL}.

ADVANCE INFORMATION



NOTE A: In order to represent the information is one illustration, nonactual phase and timebase characteristics are shown. Refer to specified parameters for precise information.

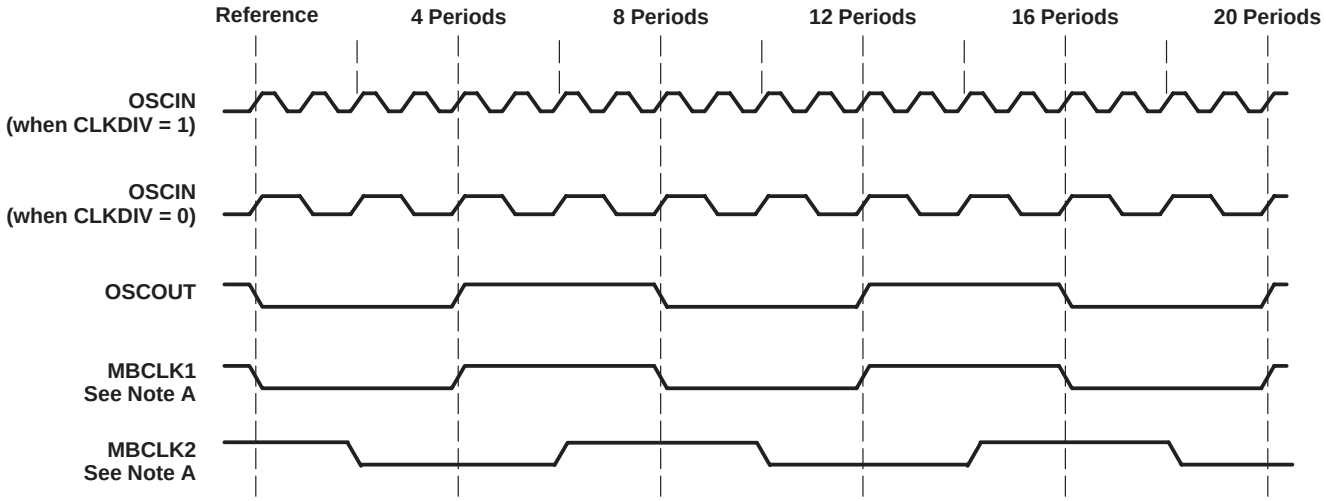
Figure 4. Timing for Power Up, System Clocks, SYNCIN, and SRESET

ADVANCE INFORMATION

memory-bus timing: local-memory clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and ADDRESS

t_M is the cycle time of one-eighth of a local memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
1	Period of MBCLK1 and MBCLK2	$4t_M$		ns
2	Pulse duration, clock high	$2t_M-9$		ns
3	Pulse duration, clock low	$2t_M-9$		ns
4	Hold time, MBCLK2 low after MBCLK1 high	t_M-9		ns
5	Hold time, MBCLK1 high after MBCLK2 high	t_M-9		ns
6	Hold time, MBCLK2 high after MBCLK1 low	t_M-9		ns
7	Hold time, MBCLK1 low after MBCLK2 low	t_M-9		ns
8	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer high	t_M-9		ns
9	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer high	t_M-14		ns
10	Setup time, address on MADH0–MADH7 before MBCLK1 no longer high	t_M-14		ns
11	Setup time, $\overline{\text{MAL}}$ high before MBCLK1 no longer high	13		ns
12	Setup time, address on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before MBCLK1 no longer low	$0.5t_M-9$		ns
13	Setup time, column address on MADL0–MADL7, MAXPH, and MAXPL before MBCLK1 no longer low	$0.5t_M-9$		ns
14	Setup time, status on MADH0–MADH7 before MBCLK1 no longer low	$0.5t_M-9$		ns
120	Setup time, $\overline{\text{NMI}}$ valid before MBCLK1 low	30		ns
121	Hold time, $\overline{\text{NMI}}$ valid after MBCLK1 low	0		ns
126	Delay time, MBCLK1 no longer low to $\overline{\text{MRESET}}$ valid	0	20	ns
129	Hold time, column address/status after MBCLK1 no longer low	t_M-7		ns



NOTE A: MBCLK1 and MBCLK2 have no timing relationship to OSCOUT. MBCLK1 and MBCLK2 can start on any OSCIN rising edge, depending on when the memory cycle starts execution.

Figure 5. Clock Waveforms After Clock Stabilization

ADVANCE INFORMATION

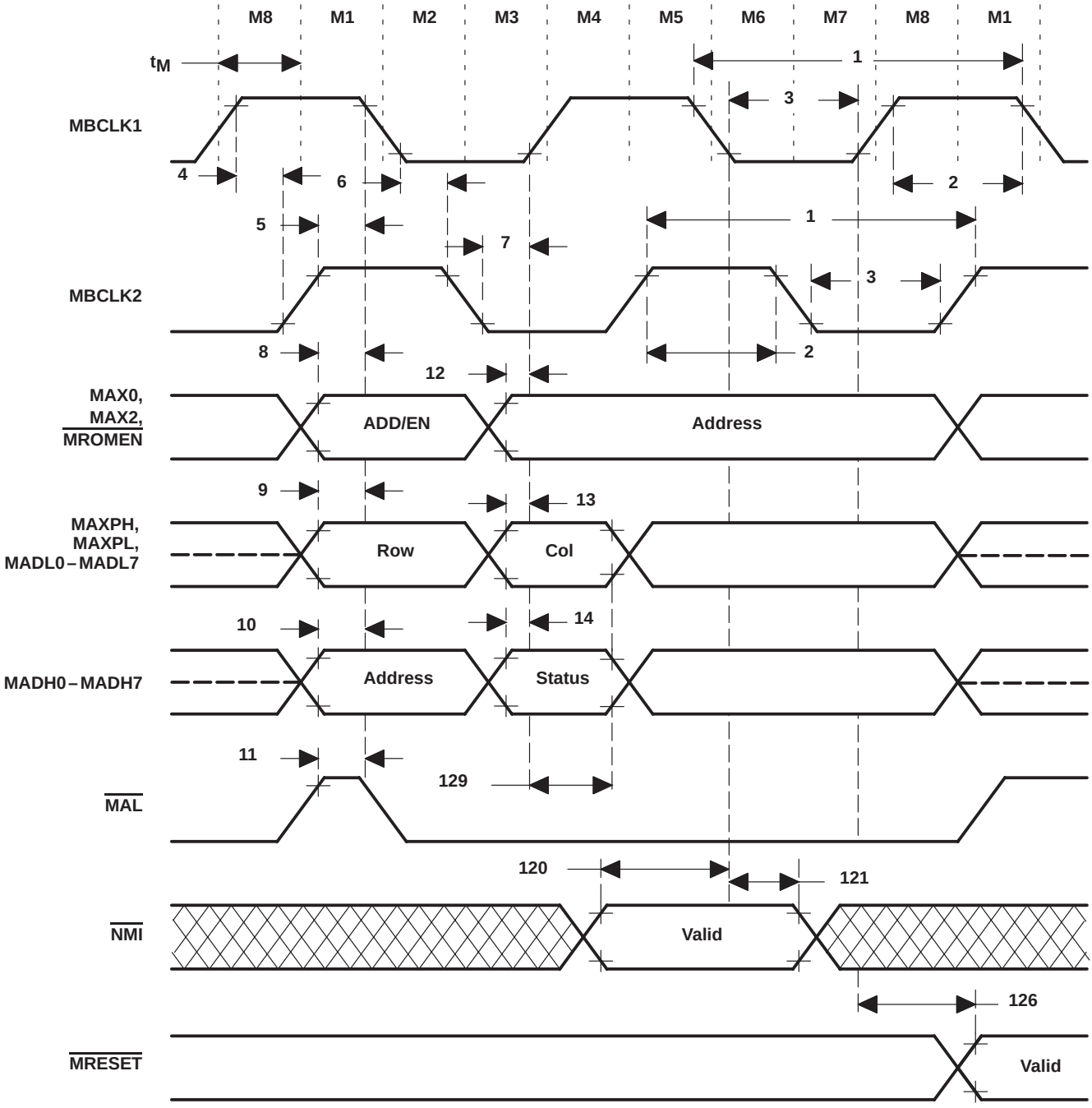


Figure 6. Memory-Bus Timing: Local-Memory Clocks, $\overline{\text{MAL}}$, $\overline{\text{MROMEN}}$, $\overline{\text{MBIAEN}}$, $\overline{\text{NMI}}$, $\overline{\text{MRESET}}$, and ADDRESS

ADVANCE INFORMATION

memory-bus timing: clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

t_M is the cycle time of one-eighth of a local memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M - 6.5$		ns
17	Delay time, $\overline{\text{MRAS}}$ no longer high to $\overline{\text{MRAS}}$ no longer high in the next memory cycle	$8t_M$		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M - 5$		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M - 5$		ns
20	Setup time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) before $\overline{\text{MCAS}}$ no longer high	$0.5t_M - 9$		ns
21	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MCAS}}$ low	$t_M - 5$		ns
22	Hold time, column address (MADL0–MADL7, MAXPH, and MAXPL) and status (MADH0–MADH7) after $\overline{\text{MRAS}}$ no longer high	$2.5t_M - 6.5$		ns
23	Pulse duration, $\overline{\text{MCAS}}$ low	$3t_M - 9$		ns
24	Pulse duration, $\overline{\text{MCAS}}$ high, refresh cycle follows read or write cycle	$2t_M - 9$		ns
25	Hold time, row address on MAXL0–MAXL7, MAXPH, and MAXPL after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
26	Setup time, row address on MAXL0–MAXL7, MAXPH, and MAXPL before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
27	Pulse duration, $\overline{\text{MAL}}$ high	$t_M - 9$		ns
28	Setup time, address/enable on MAX0, MAX2, and $\overline{\text{MROMEN}}$ before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
29	Hold time, address/enable of MAX0, MAX2, and $\overline{\text{MROMEN}}$ after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
30	Setup time, address on MADH0–MADH7 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
31	Hold time, address on MADH0–MADH7 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns

ADVANCE INFORMATION

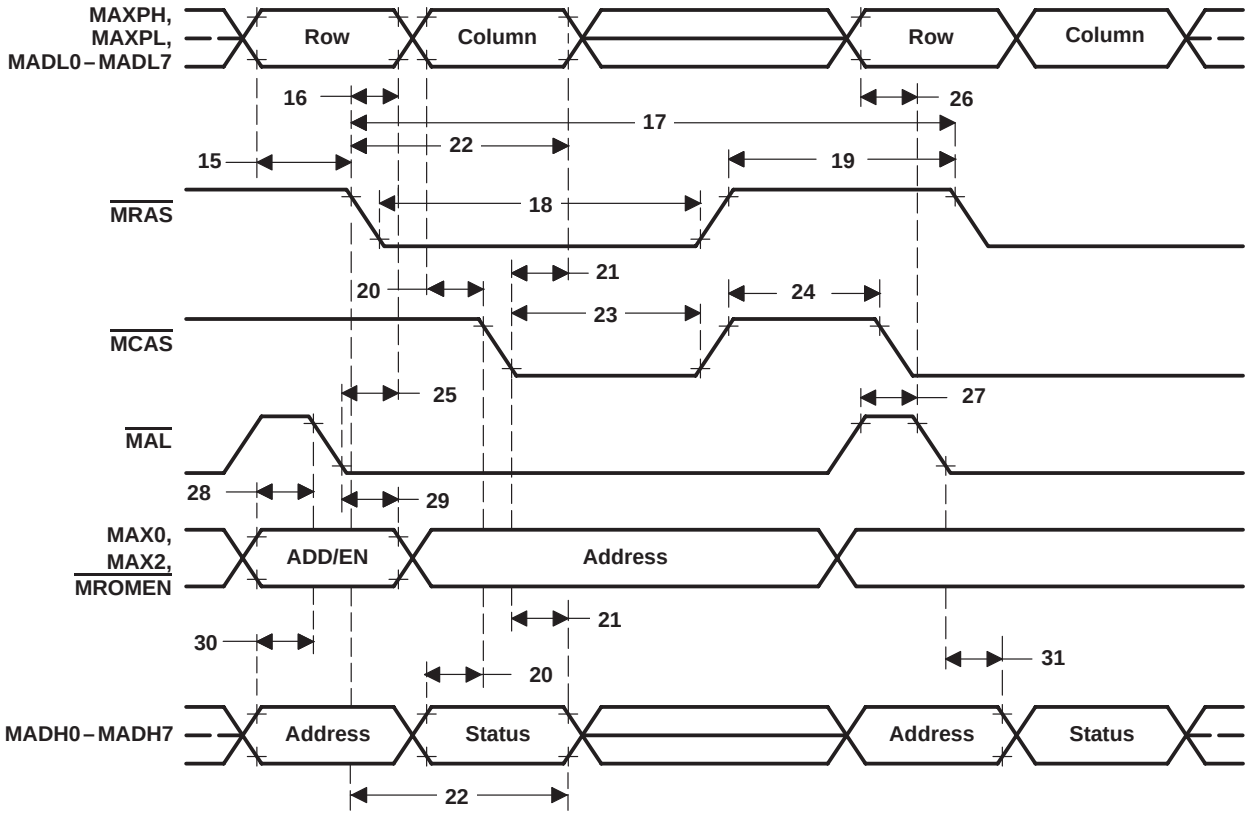


Figure 7. Memory-Bus Timing: Clocks, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

ADVANCE INFORMATION

memory-bus timing: read cycle

t_M is the cycle time of one-eighth of a local memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
32	Access time, address/enable valid on MAX0, MAX2, and $\overline{\text{MROMEN}}$ to valid data/parity		$6t_M - 23$	ns
33	Access time, address valid on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 to valid data/parity		$6t_M - 23$	ns
35	Access time, $\overline{\text{MRAS}}$ low to valid data/parity		$4.5t_M - 21.5$	ns
36	Hold time, valid data/parity after $\overline{\text{MRAS}}$ no longer low	0		ns
37†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7 and MADL0–MADL7 after $\overline{\text{MRAS}}$ high (see Note 16)	$2t_M - 10.5$		ns
38	Access time, $\overline{\text{MCAS}}$ low to valid data/parity		$3t_M - 23$	ns
39	Hold time, valid data/parity after $\overline{\text{MCAS}}$ no longer low	0		ns
40†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MCAS}}$ high (see Note 16)	$2t_M - 13$		ns
41	Delay time, $\overline{\text{MCAS}}$ no longer high to $\overline{\text{MOE}}$ low		$t_M + 13$	ns
42†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 before $\overline{\text{MOE}}$ no longer high	0		ns
43	Access time, $\overline{\text{MOE}}$ low to valid data/parity		$2t_M - 20$	ns
44	Pulse duration, $\overline{\text{MOE}}$ low	$2t_M - 9$		ns
45	Delay time, $\overline{\text{MCAS}}$ low to $\overline{\text{MOE}}$ no longer low	$3t_M - 9$		ns
46	Hold time, valid data/parity in after $\overline{\text{MOE}}$ no longer low	0		ns
47†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MOE}}$ high (see Note 16)	$2t_M - 15$		ns
48†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7, before $\overline{\text{MBEN}}$ no longer high	0		ns
48a†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0–MADL7, and MADH0–MADH7 and before $\overline{\text{MBIAEN}}$ no longer high	0		ns
49	Access time, $\overline{\text{MBEN}}$ low to valid data/parity		$2t_M - 25$	ns
49a	Access time, $\overline{\text{MBIAEN}}$ low to valid data/parity		$2t_M - 25$	ns
50	Pulse duration, $\overline{\text{MBEN}}$ low	$2t_M - 9$		ns
50a	Pulse duration, $\overline{\text{MBIAEN}}$ low	$2t_M - 9$		ns
51	Hold time, valid data/parity after $\overline{\text{MBEN}}$ no longer low	0		ns
51a	Hold time, valid data/parity after $\overline{\text{MBIAEN}}$ no longer low	0		ns
52†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBEN}}$ high (see Note 16)	$2t_M - 15$		ns
52a†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0–MADH7, and MADL0–MADL7 after $\overline{\text{MBIAEN}}$ high	$2t_M - 15$		ns
53	Hold time, MDDIR high after $\overline{\text{MBEN}}$ high, read follows write cycle	$1.5t_M - 12$		ns
54	Setup time, MDDIR low before $\overline{\text{MBEN}}$ no longer high	$3t_M - 5$		ns
55	Hold time, MDDIR low after $\overline{\text{MBEN}}$ high, write follows read cycle	$3t_M - 12$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

NOTE 16: The data/parity that exists on the address lines will most likely reach the high-impedance state sometime later than the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ (between MIN and MAX of timing parameter 36) and will be a function of the memory being read. The MIN time given represents the time from the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ to the beginning of the next address, and does not represent the actual high-impedance period on the address bus.

ADVANCE INFORMATION

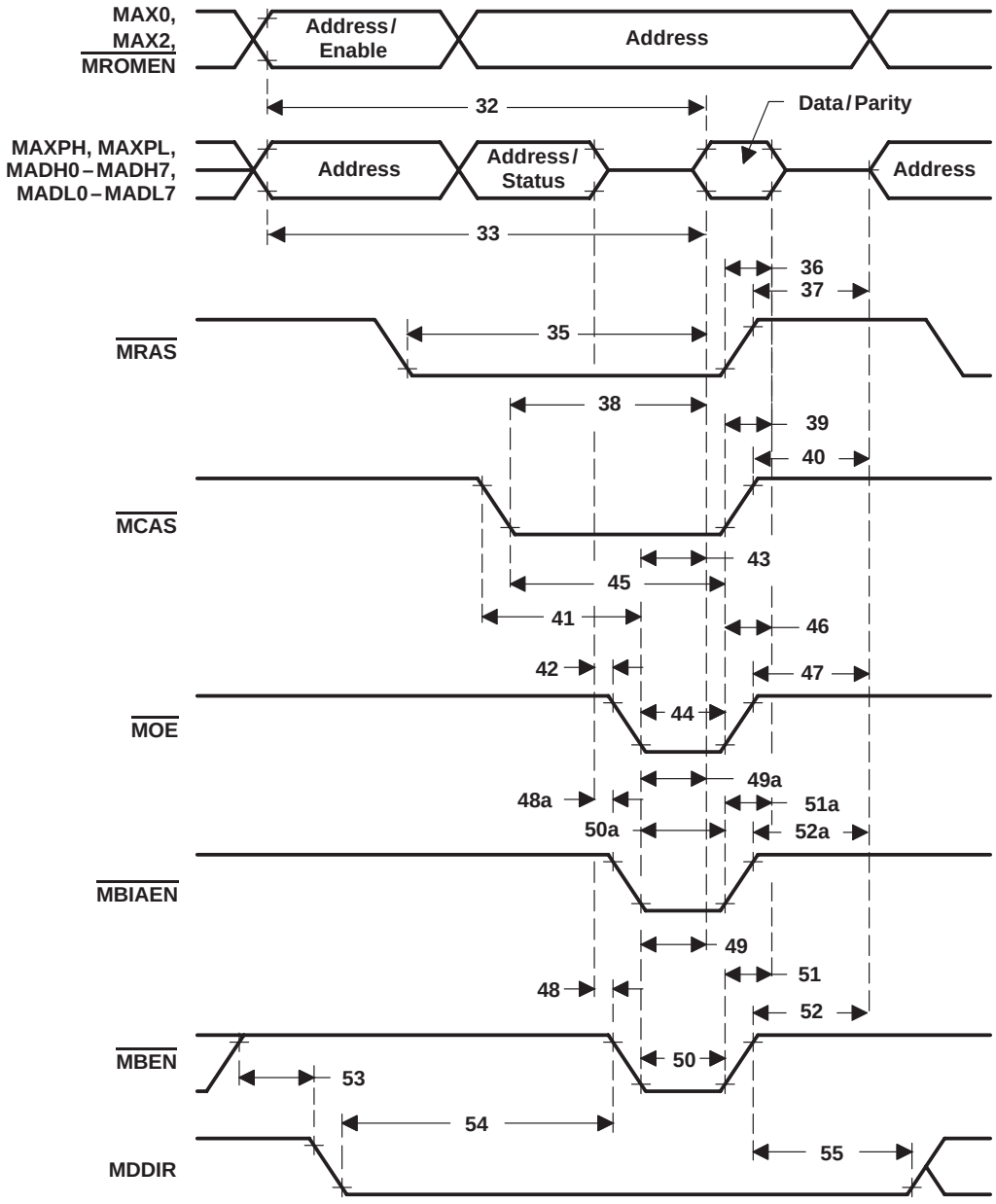


Figure 8. Memory-Bus Timing: Read Cycle

memory-bus timing: write cycle

t_M is the cycle time of one-eighth of a local memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
58	Setup time, $\overline{MW}$ low before $\overline{MRAS}$ no longer low	t_M		ns
60	Setup time, $\overline{MW}$ low before $\overline{MCAS}$ no longer low	$1.5t_M-6.5$		ns
63	Setup time, valid data/parity before $\overline{MW}$ no longer high	5.1		ns
64	Pulse duration, $\overline{MW}$ low	$2.5t_M-9$		ns
65	Hold time, data/parity out valid after $\overline{MW}$ high	$0.5t_M-10.5$		ns
66	Setup time, address valid on MAX0, MAX2, and $\overline{MROMEN}$ before $\overline{MW}$ no longer low	$7t_M-11.5$		ns
67	Hold time, $\overline{MRAS}$ low to $\overline{MW}$ no longer low	$5.5t_M-9$		ns
69	Hold time, $\overline{MCAS}$ low to $\overline{MW}$ no longer low	$4t_M-11.5$		ns
70	Setup time, $\overline{MBEN}$ low before $\overline{MW}$ no longer high	$1.5t_M-13.5$		ns
71	Hold time, $\overline{MBEN}$ low after $\overline{MW}$ high	$0.5t_M-6.5$		ns
72	Setup time, MDDIR high before $\overline{MBEN}$ no longer high	$2t_M-9$		ns
73	Hold time, MDDIR high after $\overline{MBEN}$ high	$1.5t_M-12$		ns

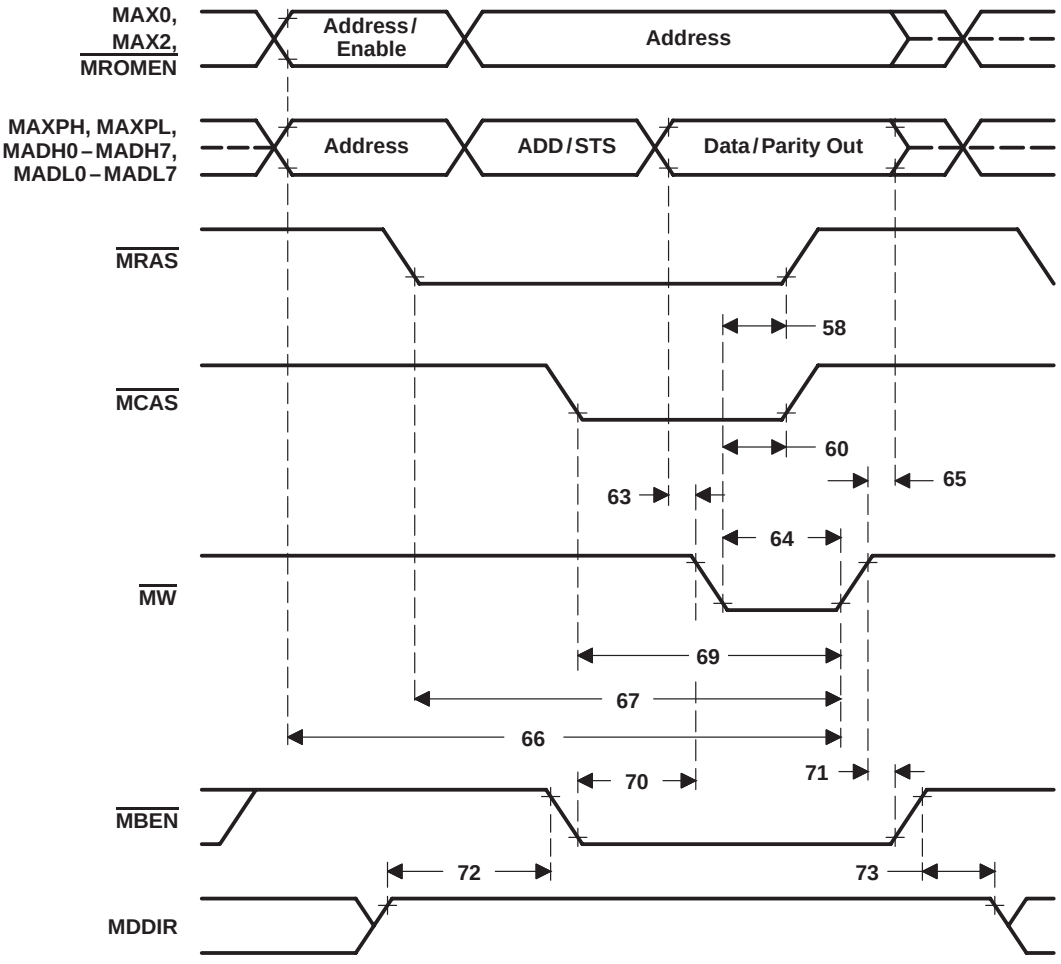


Figure 9. Memory-Bus Timing: Write Cycle

memory-bus timing: DRAM-refresh timing

t_M is the cycle time of one-eighth of a local memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0–MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$		ns
16	Hold time, row address on MADL0–MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M - 6.5$		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M - 5$		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M - 5$		ns
73a	Setup time, $\overline{\text{MCAS}}$ low before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$		ns
73b	Hold time, $\overline{\text{MCAS}}$ low after $\overline{\text{MRAS}}$ low	$4.5t_M - 6.5$		ns
73c	Setup time, MREF high before $\overline{\text{MCAS}}$ no longer high	14		ns
73d	Hold time, MREF high after $\overline{\text{MCAS}}$ high	$t_M - 9$		ns

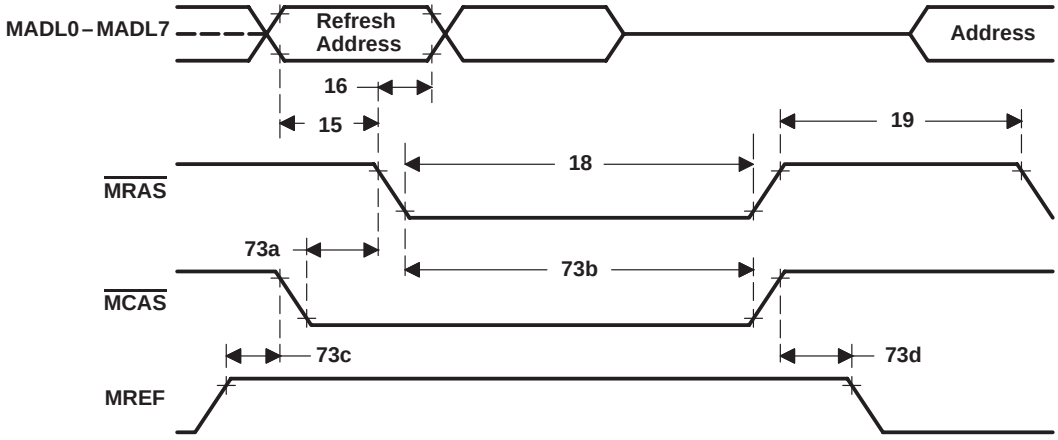


Figure 10. Memory Bus Timing: DRAM-Refresh Cycle

XMATCH and XFAIL timing

t_M is the cycle time of one-eighth of a local memory cycle (31.25 ns minimum for a 4-MHz local bus or 20.83 ns minimum for a 6-MHz local bus).

NO.		MIN	MAX	UNIT
127	Delay time, status bit 7 high to XMATCH and XFAIL recognized	$7t_M$		ns
128	Pulse duration, XMATCH or XFAIL high	50		ns

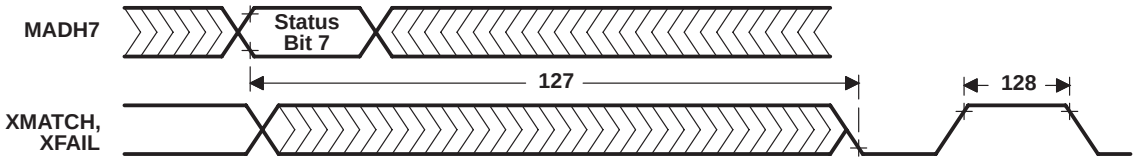


Figure 11. XMATCH and XFAIL Timing

ADVANCE INFORMATION

token ring: ring-interface timing

NO.			MIN	TYP	MAX	UNIT
153	Period of RCLK (see Note 17)	4Mbps		125		ns
		16 Mbps		31.25		ns
154L	Pulse duration, RCLK low	4 Mbps nominal: 62.5 ns	46			ns
		16 Mbps nominal: 15.625 ns	15			ns
154H	Pulse duration, RCLK high	4 Mbps nominal: 62.5 ns	35			ns
		16 Mbps nominal: 15.625 ns	8			ns
155	Setup time, RCVR valid before rising edge (1.8 V) of RCLK at 16 Mbps		10			ns
156	Hold time, RCVR valid after rising edge (1.8 V) of RCLK at 16 Mbps		4			ns
158L	Pulse duration, ring baud clock low	4 Mbps	40			ns
		16 Mbps	9			ns
158H	Pulse duration, ring baud clock high	4 Mbps	40			ns
		16 Mbps	9			ns
165	Period of OSCOUT and PXTALIN (see Note 17)	4 Mbps		125		ns
		16 Mbps (for PXTALIN only)		31.25		ns
	Tolerance of PXTALIN input frequency (see Note 17)				± 0.01	%

NOTE 17: This parameter is not tested but is required by the IEEE 802.5 specification.

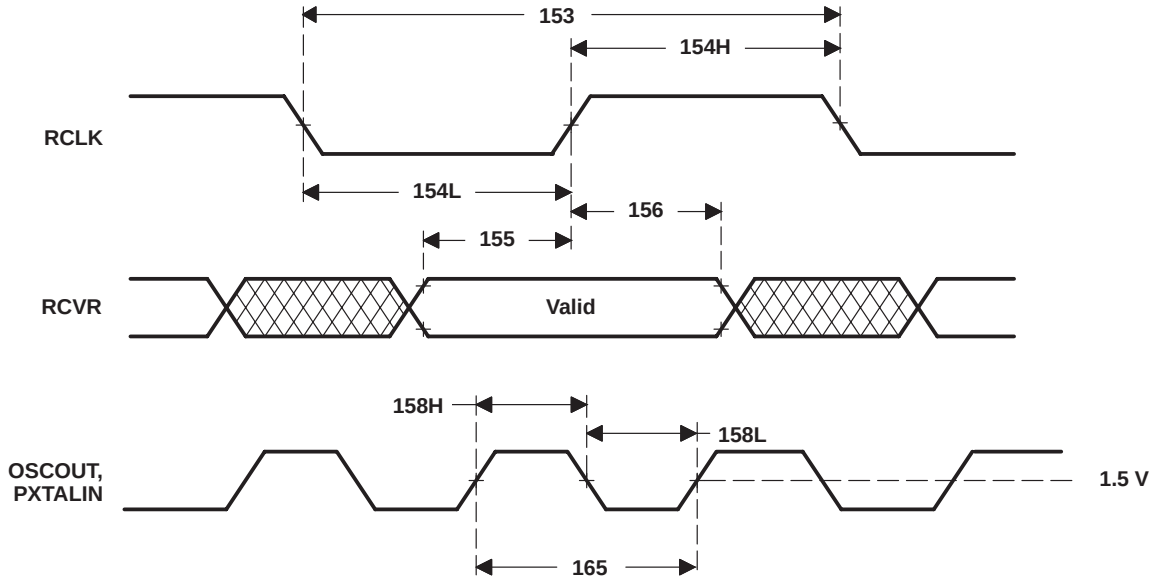


Figure 12. Ring-Interface Timing

token ring: transmitter timing

NO.			MIN	MAX	UNIT
159	$t_{sk(DR)}$	Delay from DRVR rising edge (1.8 V) to $\overline{\text{DRVR}}$ falling edge (1 V) or DRVR falling edge (1 V) to $\overline{\text{DRVR}}$ rising edge (1.8 V)		±2	ns
160	$t_{d(DR)H}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to DRVR rising edge (1.8 V)	See Note 18		ns
161	$t_{d(DR)L}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to DRVR falling edge (1 V)	See Note 18		ns
162	$t_{d(DRN)H}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to $\overline{\text{DRVR}}$ falling edge (1 V)	See Note 18		ns
163	$t_{(DRN)L}$†	Delay from RCLK (or PXTALIN) falling edge (1 V) to $\overline{\text{DRVR}}$ rising edge (1.8 V)	See Note 18		ns
164	DRVR / $\overline{\text{DRVR}}$ asymmetry	$\frac{t_{d(DR)L} + t_{d(DRN)H}}{2} - \frac{t_{d(DR)H} + t_{d(DRN)L}}{2}$		±1.5	ns

† When in active-monitor mode, the clock source is PXTALIN; otherwise, the clock-source is either RCLK or PXTALIN.
NOTE 18: This parameter is not tested to a minimum or a maximum but is measured and used as a component required for parameter 164.

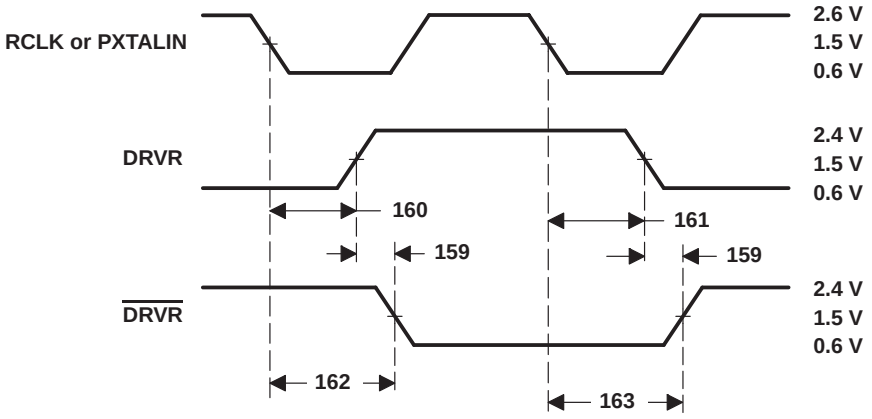


Figure 13. Skew and Asymmetry From RCLK or PXTALIN to DRVR and $\overline{\text{DRVR}}$

ethernet timing of clock signals

NO.			MIN	MAX	UNIT
300	CLKPHS	Pulse duration, TXC	45		ns
301	CLKPER	Cycle time, TXC	95	1000	ns

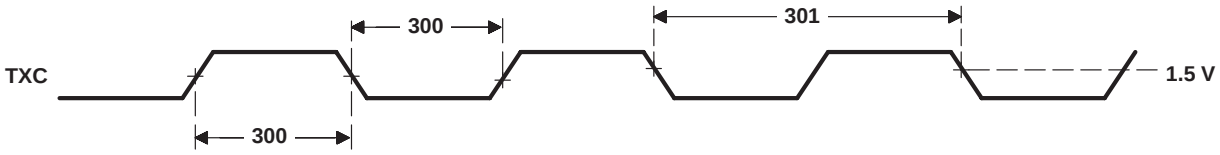


Figure 14. Ethernet Timing of TXC

ADVANCE INFORMATION

ethernet timing of XMIT signals: TXD

NO.			MIN	MAX	UNIT
305	t_{XDHLD}	Hold time, TXD after TXC high	5		ns
306	t_{XDVLD}	Delay time, TXC high to TXD valid and TXC high to TXEN high		40	ns

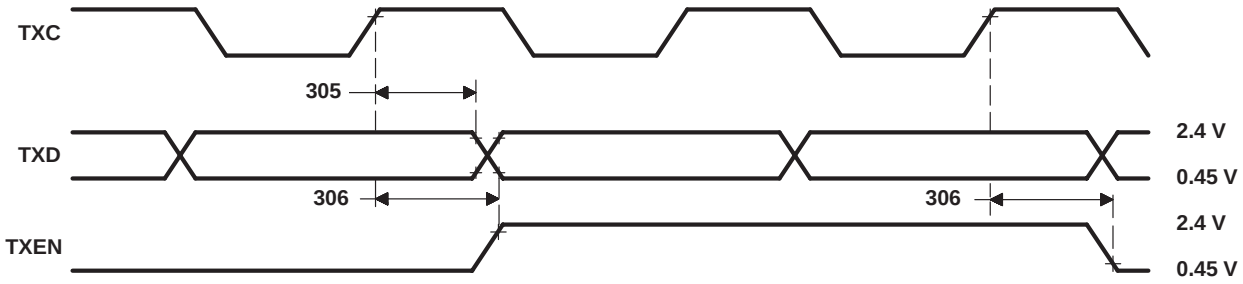


Figure 15. Ethernet Timing of XMIT Signals: TXD

ethernet timing of RCV signals: start of frame

NO.			MIN	TYP	MAX	UNIT
310	RXDSET	Setup time, RXD before RXC no longer low	20			ns
311	RXDHLD	Hold time, RXD after RXC high	5			ns
312	CRSSET	Setup time, $\overline{\text{CRS}}$ high before RXC no longer low for first valid data sample	20			ns
313	SAMDLY	Delay time, $\overline{\text{CRS}}$ internally recognized to first valid data sample (see Notes 19 and 20)		3		clock cycles
314	RXCHI	Pulse duration, RXC high	36			ns
315	RXCL0	Pulse duration, RXC low	36			ns

NOTES: 19. For valid frame synchronization, one of the following data sequences must be received. Any other pattern delays frame synchronization until after the next $\overline{\text{CRS}}$ rising edge.

a) 0 followed by n occurrences of 10 followed by 11, where n is on integer ≥ 3. For example, if n = 3, the data sequence is 010101011.

b) 10 followed by n occurrences of 10 followed by 11, where n is an integer ≥ 3. For example, if n = 3, the data sequence is 1010101011.

20. If a previous frame or frame fragment is completed without extra RXC clock cycles (XTRCVC = 0), SAMDLY = 2 clock cycles.

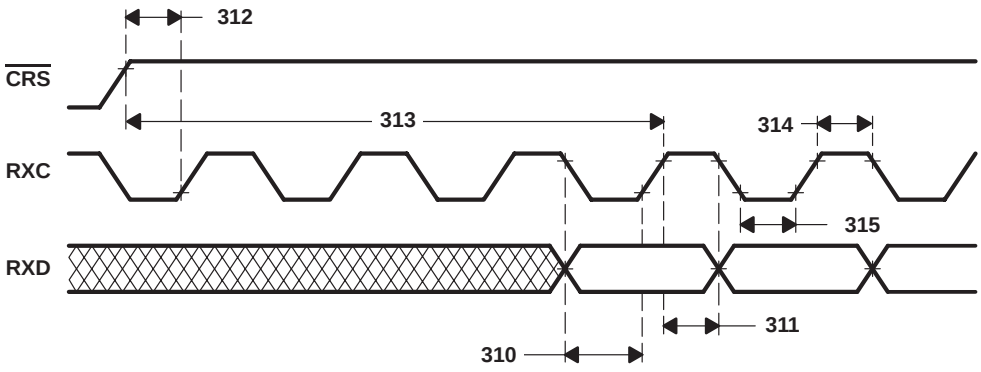


Figure 16. Ethernet Timing of RCV Signals: Start Of Frame

ethernet timing of RCV signals: end of frame

NO.			MIN	TYP	MAX	UNIT
320	CRSSET	Setup time, $\overline{\text{CRS}}$ low before RXC no longer low to determine if last data bit seen on previous RXC no longer low (see Note 21)	20			ns
321	CRSHLD	Hold time, $\overline{\text{CRS}}$ low after RXC no longer low to determine if last data bit seen on previous RXC no longer low	0			ns
322	XTRCYC	Number of extra RXC clock cycles after last data bit ($\overline{\text{CRS}}$ is low) (see Note 21)	0	5		cycle

NOTE 21: The TI380C27 operates correctly even with no extra RXC clock cycles, provided that $\overline{\text{CRS}}$ does not remain asserted longer than 2 μs (see timing spec NORXC). Provided no extra clocks affect receive-startup timing, see timing spec SAMDLY.

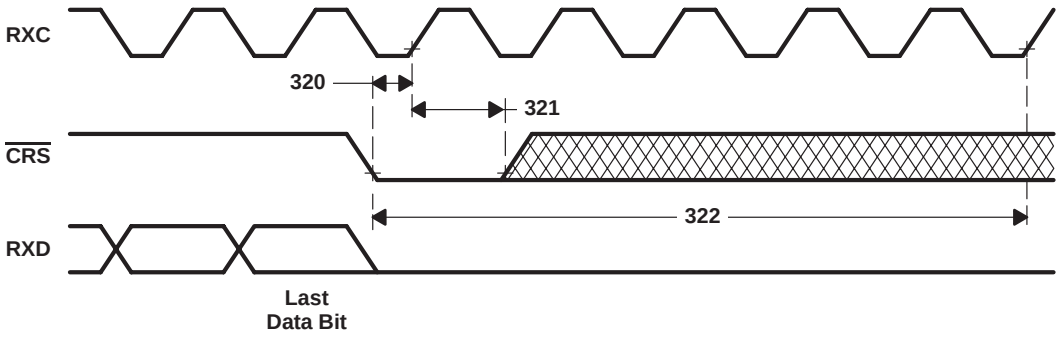


Figure 17. Ethernet Timing of RCV Signals: End of Frame

ethernet timing of RCV signals: no RXC

NO.			MIN	MAX	UNIT
330	NORXC	Time with no clock pulse on RXC, when CRS is high (see Note 22)		2	μs

NOTE 22: If NORXC is exceeded, local-clock-failure circuitry may become activated, resetting the device.

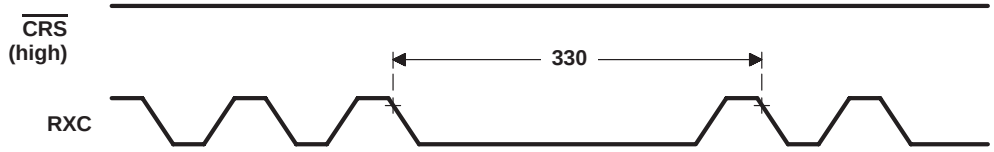


Figure 18. Ethernet Timing of RCV Signals: No RXC

ADVANCE INFORMATION

ethernet timing of XMIT signals: COLL

NO.			MIN	MAX	UNIT
340	HBWIN	Delay time from TXC high of the last transmitted data bit (TXEN is high) to COLL sampled high, so not to generate a heart-beat error		47	cycles
341	COLPUL	Minimum pulse duration of COLL high for assured sample	20 ns + 1 cycle		ns
342	COLSET	Setup of COLL high to TXC high	20		ns

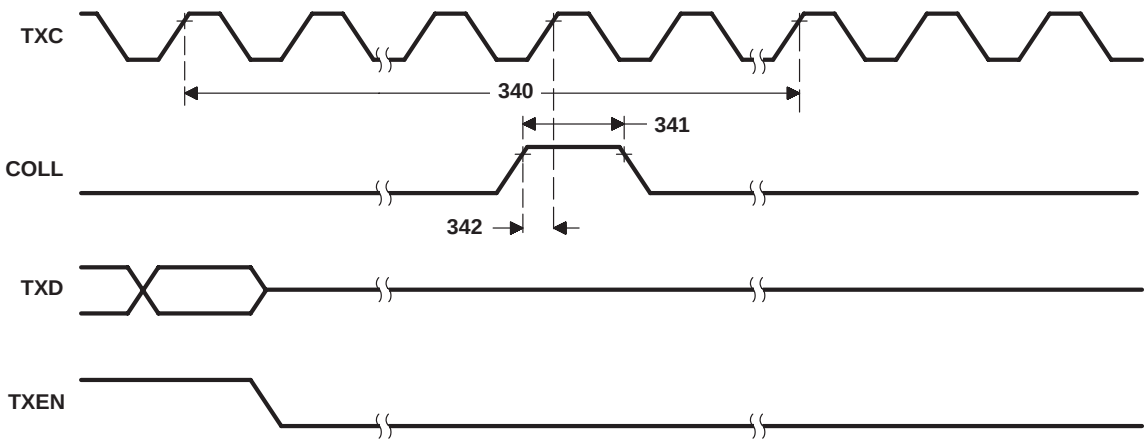


Figure 19. Ethernet Timing of XMIT Signals: COLL

ethernet timing of XMIT signals: JAM

NO.			MIN	MAX	UNIT
350	JAMTIM	Time from COLL sampled high (TXC high) to first transmitted JAM bit on TXD (see Note 23)		4	cycles
351	COLSET	Setup time, COLL high before TXC high	20		ns
352	COLPUL	Pulse duration, COLL high for assured sample, minimum	20 ns + 1 cycle		ns

NOTE 23: The JAM pattern is delayed until after the completion of the preamble pattern. The TI380C27 transmits a JAM pattern of all 1s.

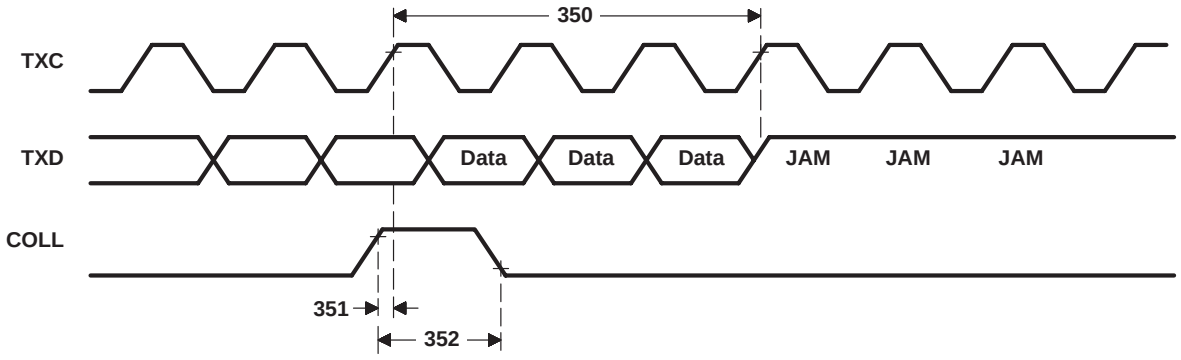


Figure 20. Ethernet Timing of XMIT Signals: JAM

80x8x DIO read-cycle timing

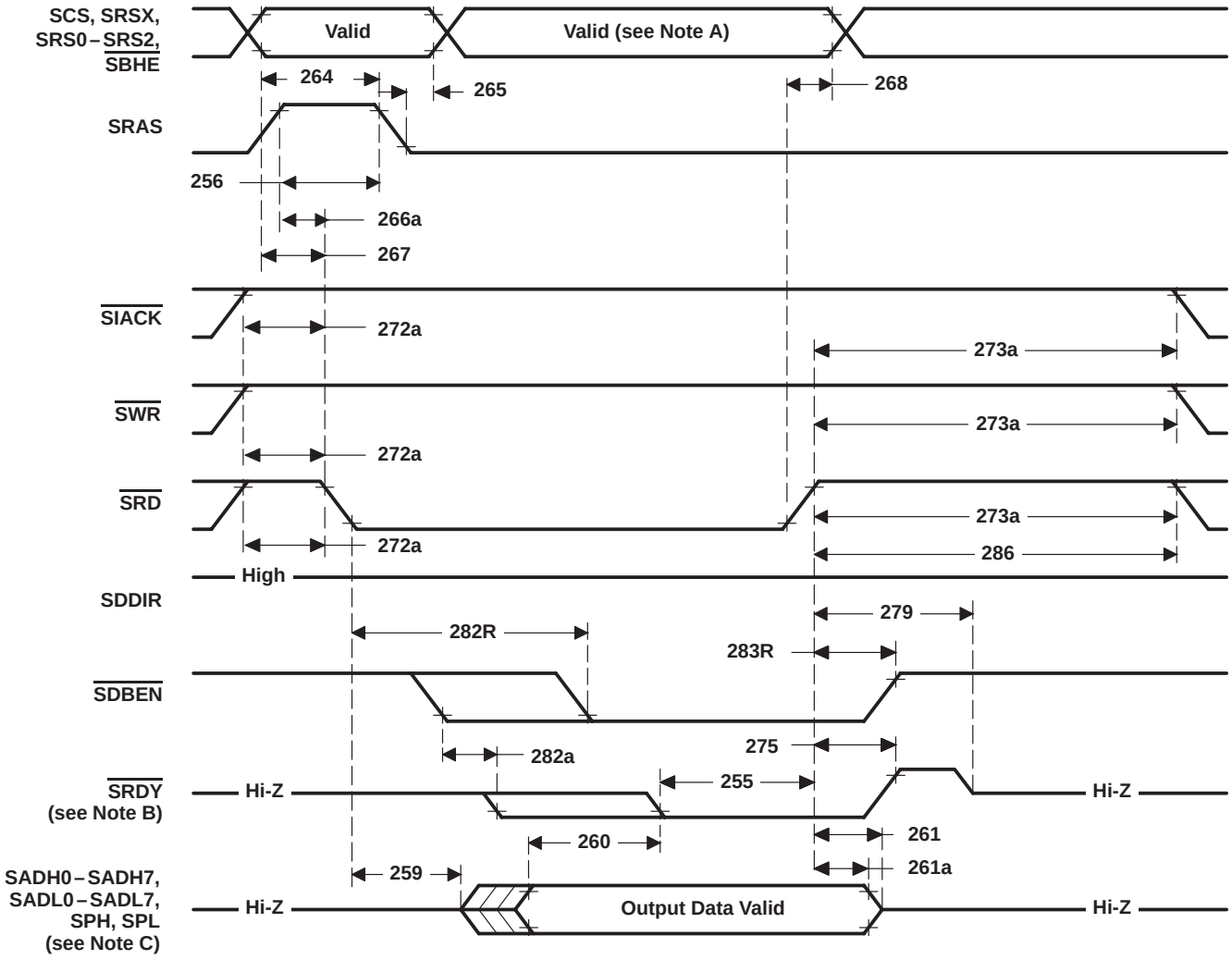
NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to either $\overline{\text{SCS}}$ or $\overline{\text{SRD}}$ high	15		15		ns
256	Pulse duration, SRAS high	30		30		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SRD}}$ low (see Note 24)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{\text{SRDY}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SRD}}$ or $\overline{\text{SCS}}$ high to SAD in the high-impedance state (see Note 24)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SRD}}$ or $\overline{\text{SCS}}$ high (see Note 24)	0		0		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ valid to SRAS no longer high (see Note 25)	30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ valid after SRAS low	10		10		ns
266a	Setup time, SRAS high to $\overline{\text{SRD}}$ no longer high (see Note 25)	15		15		ns
267‡	Setup time, SRSX, SRS0–SRS2 valid before $\overline{\text{SRD}}$ no longer high (see Note 24)	15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{\text{SRD}}$ no longer low (see Note 25)	0		0		ns
272a	Setup time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high from previous cycle to $\overline{\text{SRD}}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high after $\overline{\text{SRD}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$, or $\overline{\text{SCS}}$ high to $\overline{\text{SRDY}}$ high (see Note 24)	0	25	0	25	ns
279†	Delay time, $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$, high to $\overline{\text{SRDY}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low in a read cycle	0	$t_{c(SCK)}$ / 2 + 4	0	$t_{c(SCK)}$ / 2 + 4	ns
282R	Delay time, $\overline{\text{SRD}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)}$ +3	0	$t_{c(SCK)}$ +3	ns
283R	Delay time, $\overline{\text{SRD}}$ high to $\overline{\text{SDBEN}}$ high (see Note 24)	0	$t_{c(SCK)}$ / 2 + 4	0	$t_{c(SCK)}$ / 2 + 4	ns
286	Pulse duration, $\overline{\text{SRD}}$ high between DIO accesses (see Note 24)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.

NOTES: 24. The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

25. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0 – SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

ADVANCE INFORMATION



NOTES: A. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

B. When the TI380C27 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

C. In 8-bit 80x8x mode DIO reads, the SADH0–SADH7 contain don't care data.

Figure 21. 80x8x DIO Read-Cycle Timing

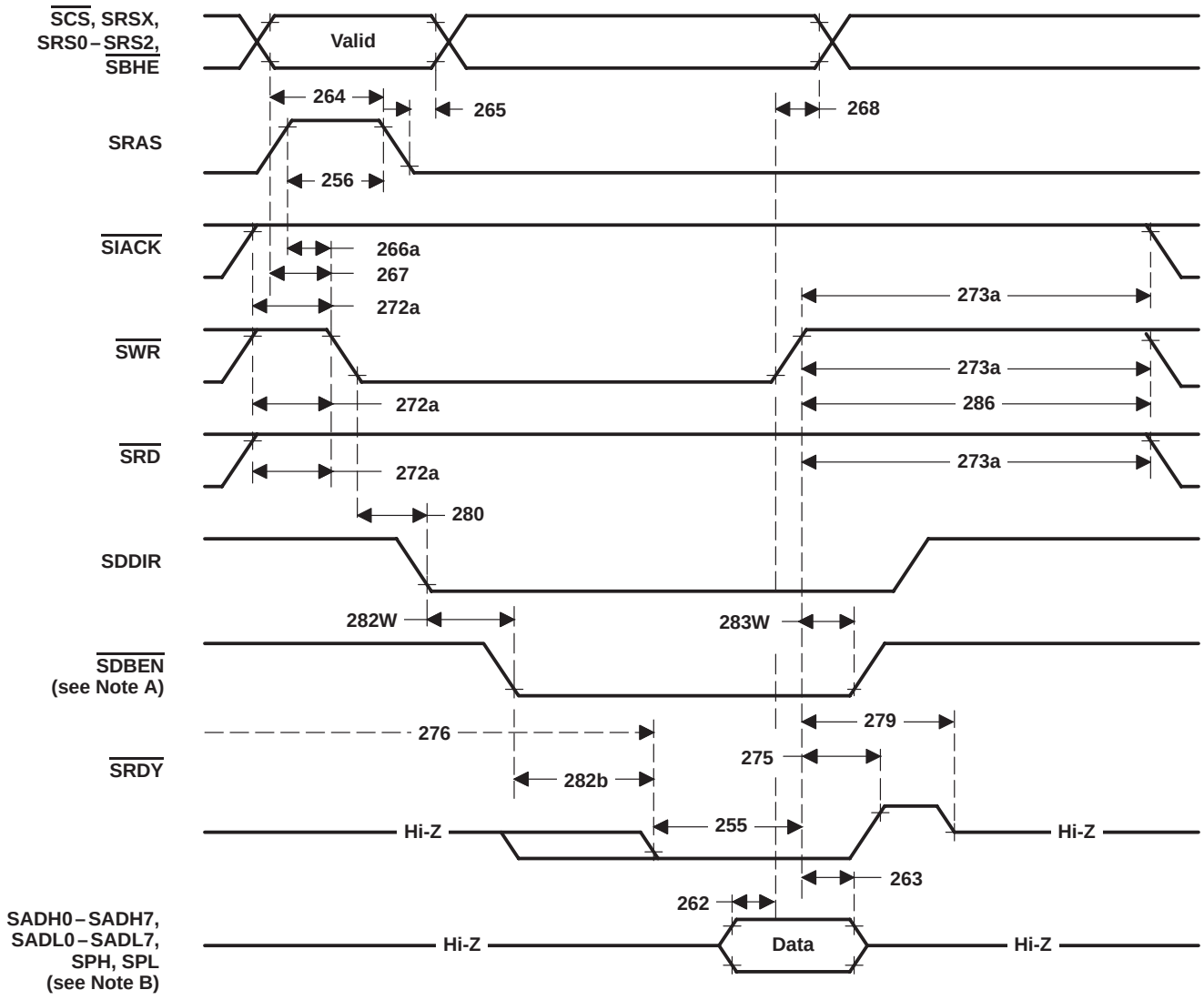
80x8x DIO write-cycle timing

NO.			25-MHz OPERATION		33-MHz OPERATION		UNIT
			MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to either $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ high		15		15		ns
256	Pulse duration, SRAS high		30		30		ns
262	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ no longer low		15		15		ns
263	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ high		15		15		ns
264	Setup time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ to SRAS no longer high (see Note 25)		30		30		ns
265	Hold time, SRSX, SRS0–SRS2, $\overline{\text{SCS}}$, and $\overline{\text{SBHE}}$ after SRAS low		10		10		ns
266a	Setup time, SRAS high to $\overline{\text{SWR}}$ no longer high (see Note 25)		15		15		ns
267†	Setup time, SRSX, SRS0–SRS2 before $\overline{\text{SWR}}$ no longer high (see Note 24)		15		15		ns
268	Hold time, SRSX, SRS0–SRS2 valid after $\overline{\text{SWR}}$ no longer low (see Note 25)		0		0		ns
272a	Setup time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high from previous cycle to $\overline{\text{SWR}}$ no longer high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, $\overline{\text{SRD}}$, $\overline{\text{SWR}}$, and $\overline{\text{SIACK}}$ high after $\overline{\text{SWR}}$ high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
276‡	Delay time, $\overline{\text{SRDY}}$ low in the first DIO access to the SIF register to $\overline{\text{SRDY}}$ low in the immediately following access to the SIF (see *TMS380 Second-Generation Token Ring User's Guide*, SPWU005, subsection 3.4.1.1.1)			4000		4000	ns
275	Delay time, $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ high to $\overline{\text{SRDY}}$ high (see Note 24)		0	25	0	25	ns
279§	Delay time, $\overline{\text{SWR}}$ high to $\overline{\text{SRDY}}$ in the high-impedance state		0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{\text{SWR}}$ low to SDDIR low (see Note 24)		0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
282b	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
		If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{\text{SDBEN}}$ low		0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
283W	Delay time, $\overline{\text{SCS}}$ or $\overline{\text{SWR}}$ high to $\overline{\text{SDBEN}}$ no longer low		0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
286	Pulse duration $\overline{\text{SWR}}$ high between DIO accesses (see Note 24)		$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ This specification is provided as an aid to board design. It is not assured during manufacturing testing.

NOTES: 24. The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.
25. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

ADVANCE INFORMATION



NOTES: A. When the TI380C27 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

B. In 8-bit 80x8x-mode DIO writes, the value placed on SADH0–SADH7 is a don't care.

Figure 22. 80x8x DIO Write-Cycle Timing

ADVANCE INFORMATION

80x8x interrupt-acknowledge-cycle timing: first $\overline{\text{SIACK}}$ pulse

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
286	Pulse duration, $\overline{\text{SIACK}}$ high between DIO accesses (see Note 24)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
287	Pulse duration, $\overline{\text{SIACK}}$ low on first pulse of two pulses	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

NOTE 24: The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

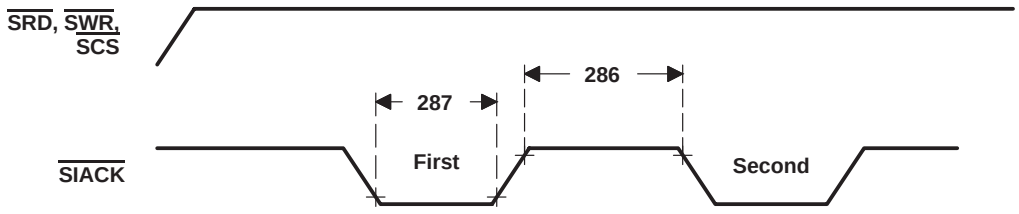


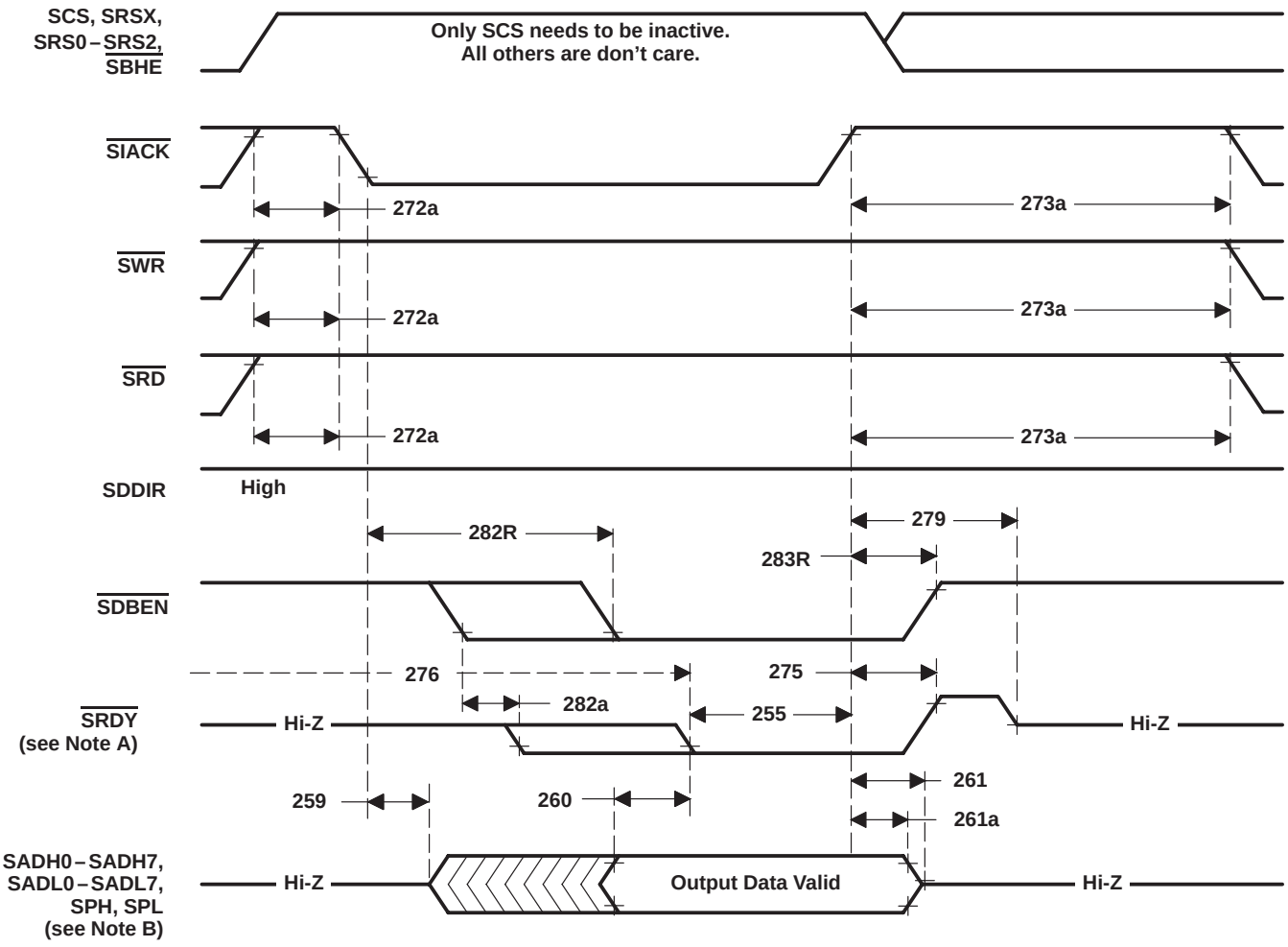
Figure 23. 80x8x Interrupt-Acknowledge-Cycle Timing: First $\overline{\text{SIACK}}$ Pulse

80x8x interrupt-acknowledge-cycle timing: second $\overline{\text{SIACK}}$ pulse

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SRDY}}$ low to $\overline{\text{SCS}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SIACK}}$ low (see Note 24)	0		0		ns
260	Setup time, output data valid before $\overline{\text{SRDY}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SIACK}}$ high to SAD in the high-impedance state (see Note 24)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SIACK}}$ high (see Note 24)	0		0		ns
272a	Setup time, inactive data strobe high to $\overline{\text{SIACK}}$ no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive data strobe high after $\overline{\text{SIACK}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ high (see Note 24)	0	25	0	25	ns
276‡	Delay time, $\overline{\text{SRDY}}$ low in the first DIO access to the SIF register to $\overline{\text{SRDY}}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SRDY}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SRDY}}$ low in a read cycle	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns
282R	Delay time, $\overline{\text{SIACK}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1), provided previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDBEN}}$ high (see Note 24)	0	$t_{c(SCK)} / 2 + 4$	0	$t_{c(SCK)} / 2 + 4$	ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 24: The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

ADVANCE INFORMATION



NOTES: A. $\overline{\text{SRDY}}$ is an active-low bus ready signal. It must be asserted before data output.
B. In 8-bit 80x8x mode DIO writes, the value placed on SADH0 – SADH7 is a don't care.

Figure 24. 80x8x Interrupt-Acknowledge-Cycle Timing: Second $\overline{\text{SIACK}}$ Pulse

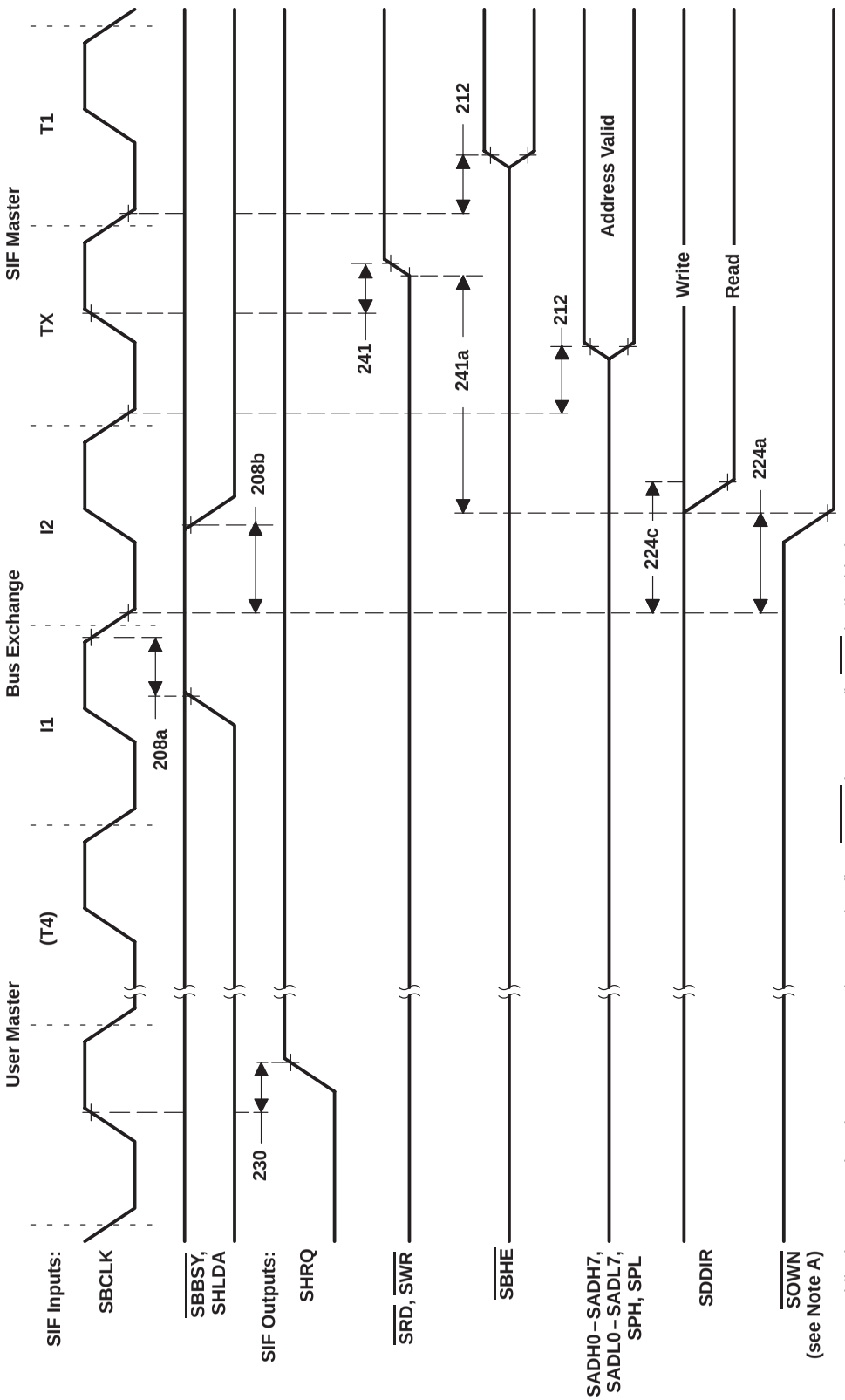
ADVANCE INFORMATION

80x8x-mode bus-arbitration timing, SIF takes control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SBBSY}}$ and SHLDA after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to SHRQ high		20		20	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ high, bus acquisition		25		25	ns
241a†	Hold time, SRD and $\overline{\text{SWR}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}-15$		$t_{c(SCK)}-15$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

ADVANCE INFORMATION



NOTE A: While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

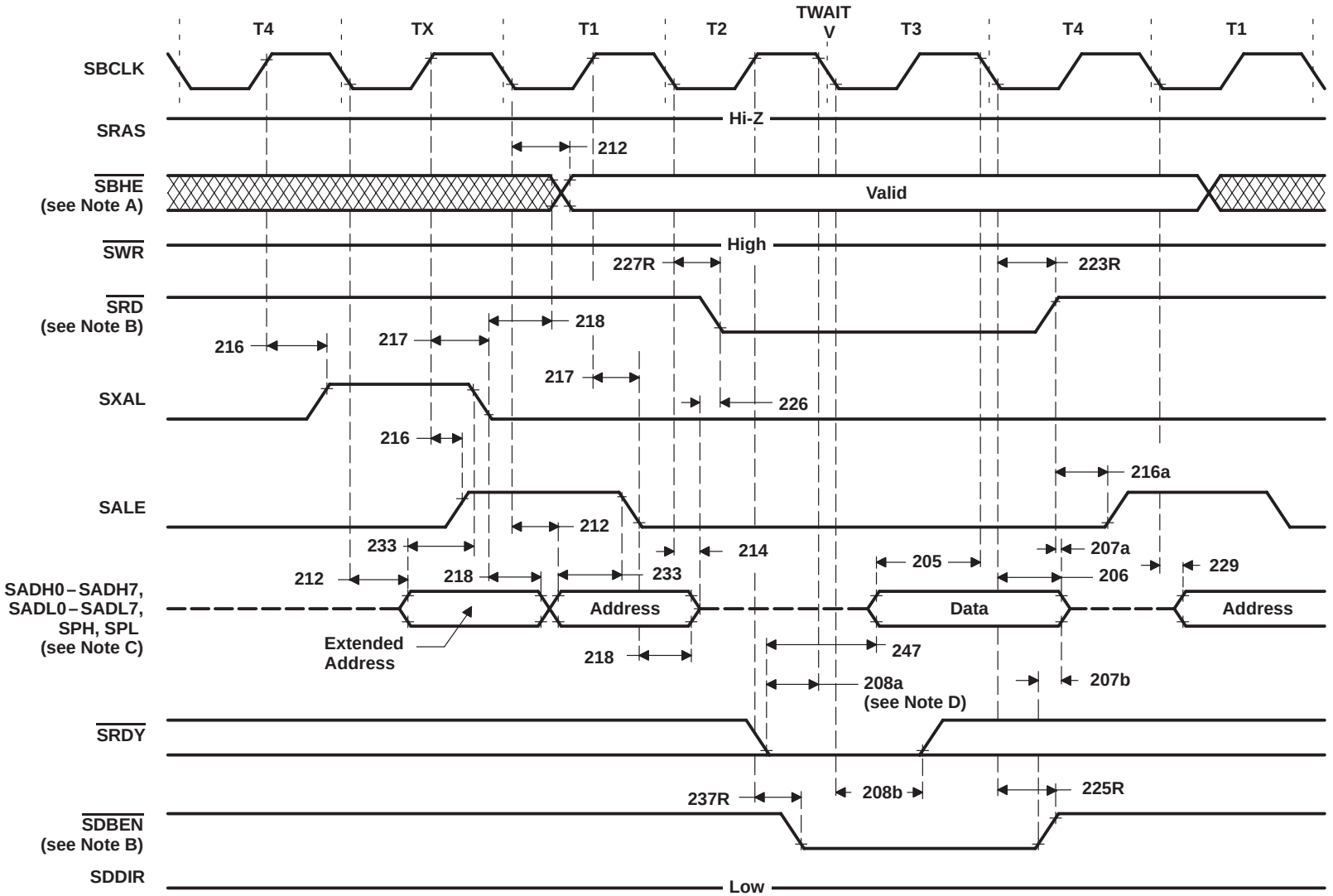
Figure 25. 80x8x-Mode Bus-Arbitration Timing, SIF Takes Control

80x8x-mode DMA read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{\text{SRD}}$ high	0		0		ns
207b	Hold time, SADL0–SADL7, SADH0–SADH7, SPH, and SPL valid after $\overline{\text{SDBEN}}$ no longer low	0		0		ns
208a	Setup time, asynchronous signal $\overline{\text{SRDY}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SRDY}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid		20		20	ns
214†	Delay time, SBCLK low in T1 cycle to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SRD}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after SALE or SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SRD}}$ high (see Note 26)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
226†	Delay time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state to $\overline{\text{SRD}}$ low	0		0		ns
227R	Delay time, SBCLK low in T2 cycle to $\overline{\text{SRD}}$ low	0	15	0	15	ns
229†	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state after SBCLK low in T1 cycle	0		0		ns
231	Pulse duration, $\overline{\text{SRD}}$ low	$2t_{c(SCK)}-25$		$2t_{c(SCK)}-25$		ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237R	Delay time, SBCLK high in the T2 cyle to $\overline{\text{SDBEN}}$ low		16		11	ns
247	Setup time, data valid before $\overline{\text{SRDY}}$ low if parameter 208a not met	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 26: While the system-interface DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.

ADVANCE INFORMATION



NOTES: A. In 8-bit 80x8x mode, $\overline{\text{SBHE}}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
B. Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.
C. In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 21; i.e., held after T4 high.
D. If parameter 208a is not met, valid data must be present before $\overline{\text{SRDY}}$ goes low.

Figure 26. 80x8x-Mode DMA Read-Cycle Timing

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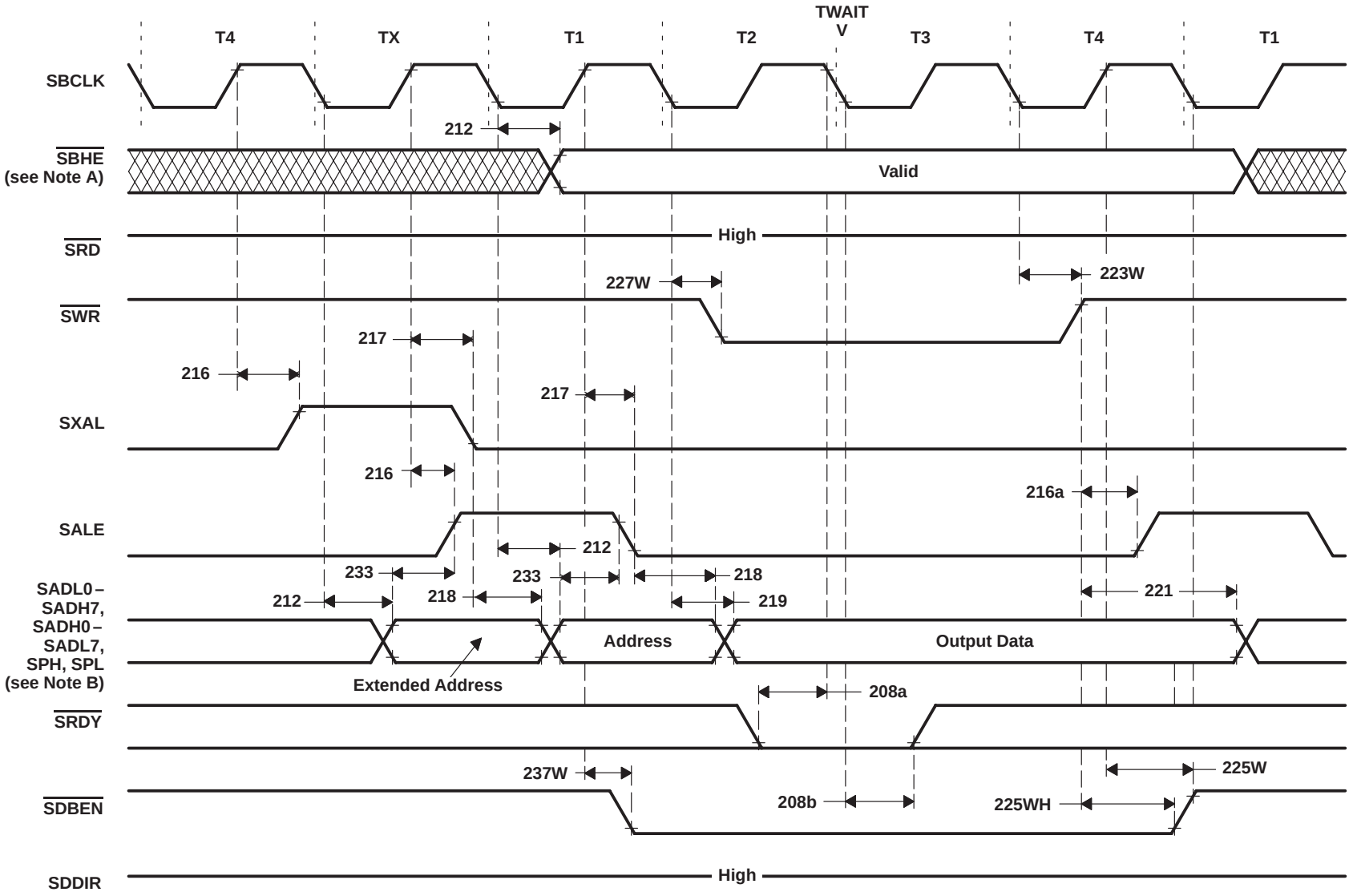
80x8x-mode DMA write-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous signal $\overline{\text{SRDY}}$ before SBCLK no longer high to assure recognition on that cycle	10		10		ns
208b	Hold time, asynchronous signal $\overline{\text{SRDY}}$ after SBCLK low to assure recognition on that cycle	10		10		ns
212	Delay time, SBCLK low to SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SWR}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid after $\overline{\text{SWR}}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
223W	Delay time, SBCLK low to $\overline{\text{SWR}}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
225WH	Hold time, $\overline{\text{SDBEN}}$ low after $\overline{\text{SWR}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
227W	Delay time, SBCLK low in T2 cycle to $\overline{\text{SWR}}$ low	0	20	0	15	ns
233	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before SALE, SXAL no longer high	10		10		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns

ADVANCE INFORMATION



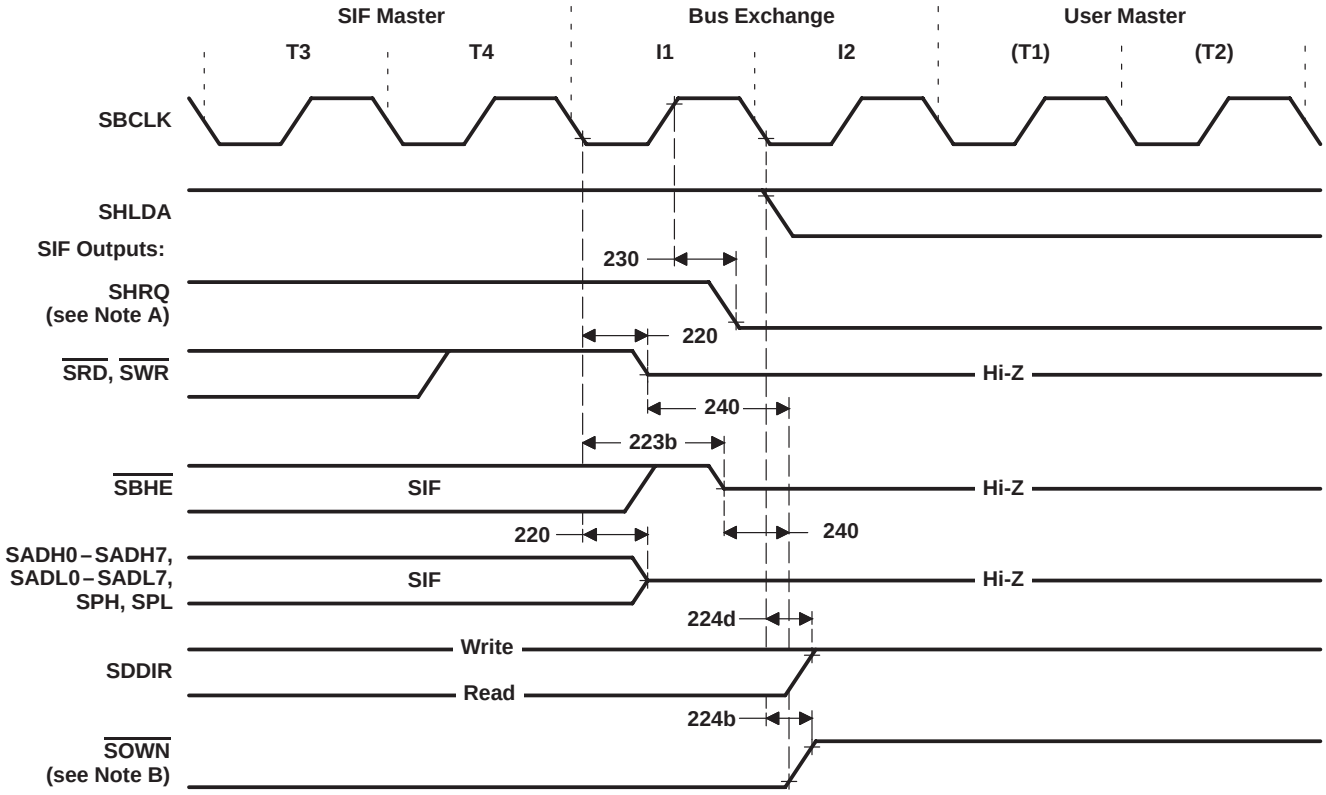
NOTES: A. In 8-bit 80x8x mode, $\overline{\text{SBHE}}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
B. In 8-bit 80x8x mode, the most significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to parameter 21; i.e., held after T4 high.

Figure 27. 80x8x-Mode DMA Write-Cycle Timing

80x8x-mode bus-arbitration timing, SIF returns control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220†	Delay time, SBCLK low in I1 cycle to SADH0–SADH7, SADL0–SADL7, SPL, SPH, $\overline{SRD}$, and $\overline{SWR}$ in the high-impedance state		35		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{SBHE}$ in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{SOWN}$ high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high in cycle I1 to SHRQ low		20		15	ns
240†	Setup time, $\overline{SRD}$, $\overline{SWR}$, and $\overline{SBHE}$ in the high-impedance state before $\overline{SOWN}$ no longer low	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.



NOTES: A. In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts $\overline{SBRQ}$ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.

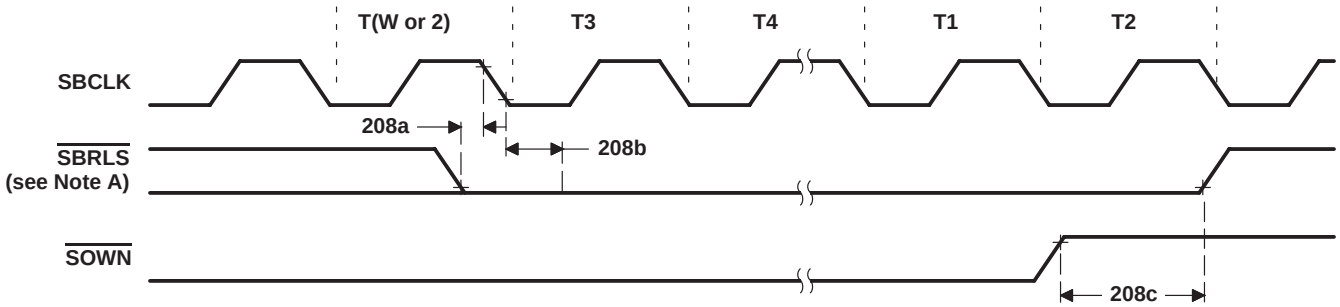
B. While the system-interface DMA controls are active (i.e., $\overline{SOWN}$ is asserted), $\overline{SCS}$ is disabled.

Figure 28. 80x8x-Mode Bus-Arbitration Timing, SIF Returns Control

ADVANCE INFORMATION

80x8x-mode bus-release timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBRLS}}$ low before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$ low after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		0		ns



NOTES: A. The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquishes control of the bus. If no DMA transfer has internally started, the system interface releases the bus before starting another.

B. If $\overline{\text{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed regardless of the value of $\overline{\text{SRDY}}$. If the BERETRY register is non zero, the cycle is retried. If the BERETRY register is zero, the system interface releases control of the system bus. The system interface ignores the assertion of $\overline{\text{SBERR}}$ if it is not performing a DMA bus cycle on the system bus. When $\overline{\text{SBERR}}$ is properly asserted and BERETRY is zero, however, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

C. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

D. $\overline{\text{SDTACK}}$ is not sampled to verify that it is deasserted.

E. Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

Figure 29. 80x8x-Mode Bus-Release Timing

68xxx DIO read-cycle timing

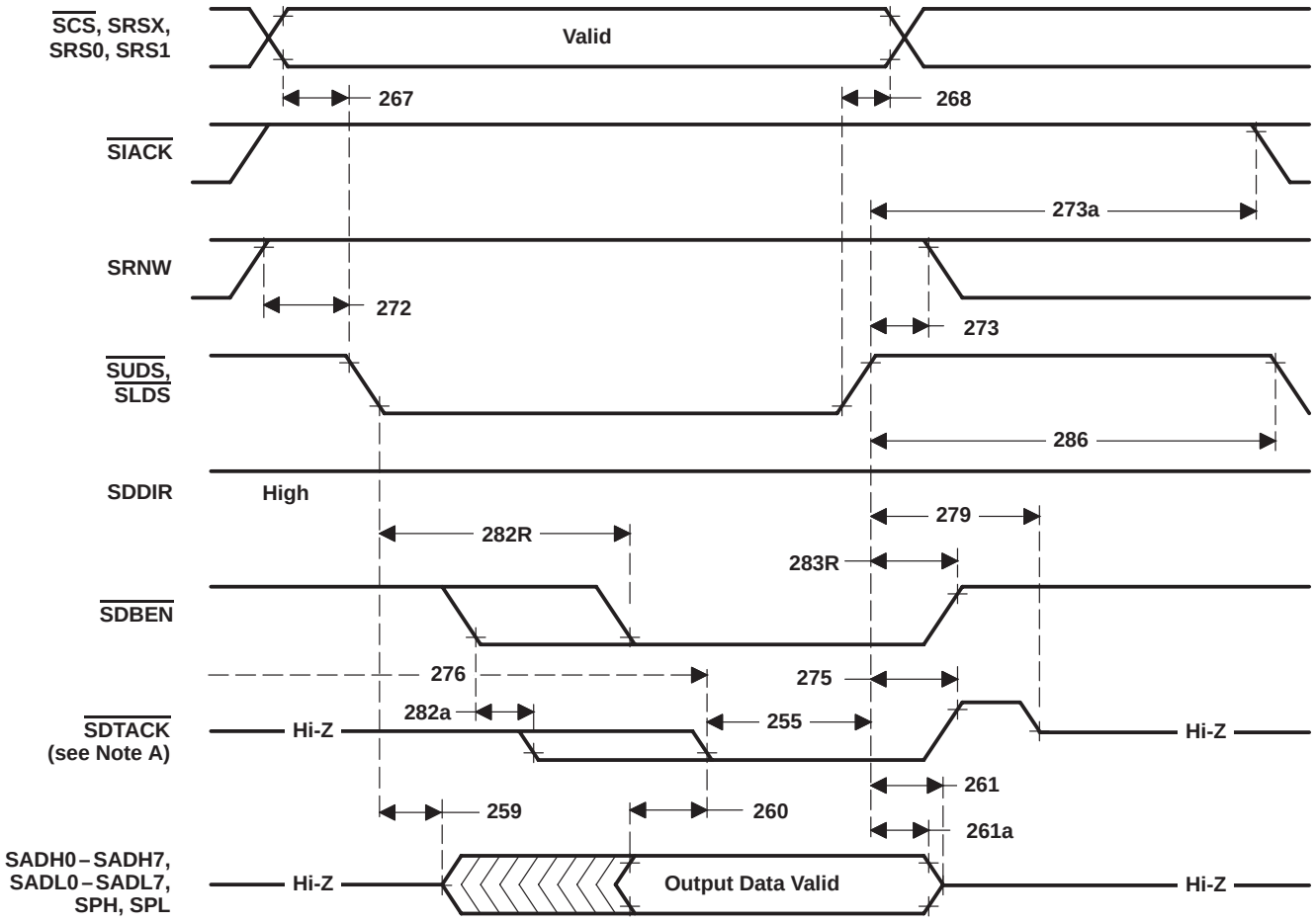
NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SDTACK}}$ low to either $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ low (see Note 24)	0		0		ns
260	Setup time, SADH0–SADH7, SADL0–SADL7, SPH, and SPL valid before $\overline{\text{SDTACK}}$ low	0		0		ns
261†	Delay time, $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high to SADH0–SADH7, SADL0–SADL7, SPH, and SPL in the high-impedance state (see Note 24)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low (see Note 24)	0		0		ns
267	Setup time, register address before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 24)	15		15		ns
268	Hold time, register address valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low (see Note 25)	0		0		ns
272	Setup time, SRNW before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 24)	12		12		ns
273	Hold time, SRNW after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high	0		0		ns
273a	Hold time, $\overline{\text{SIACK}}$ high after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$, or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ high (see Note 24)	0	25	0	25	ns
276‡	Delay time, $\overline{\text{SDTACK}}$ low in the first DIO access to the SIF register to $\overline{\text{SDTACK}}$ low in the immediately following access to the SIF		4000		4000	ns
279†	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SDTACK}}$ low	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
282R	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1) provided the previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDBEN}}$ high (see Note 24)	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
286	Pulse duration, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high between DIO accesses (see Note 24)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

NOTES: 24. The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

25. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

ADVANCE INFORMATION



NOTE A: SDTACK is an active-low bus ready signal. It must be asserted before data output.

Figure 30. 68xxx DIO Read-Cycle Timing

ADVANCE INFORMATION

68xxx DIO write-cycle timing

NO.			25-MHz OPERATION		33-MHz OPERATION		UNIT
			MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SDTACK}}$ low to either $\overline{\text{SCS}}$, SUDS or $\overline{\text{SLDS}}$ high		15		15		ns
262	Setup time, write data valid before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low		15		15		ns
263	Hold time, write data valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high		15		15		ns
267§	Setup time, register address before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 24)		15		15		ns
268	Hold time, register address valid after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer low (see Note 25)		0		0		ns
272	Setup time, SRNW before $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ no longer high (see Note 24)		12		12		ns
272a	Setup time, inactive $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to active data strobe no longer high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273	Hold time, SRNW after $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high		0		0		ns
273a	Hold time, inactive $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high after active data strobe high		$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SCS}}$, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ high (see Note 24)		0	25	0	25	ns
276‡	Delay time, $\overline{\text{SDTACK}}$ low in the first DIO access to the SIF register to $\overline{\text{SDTACK}}$ low in the immediately following access to the SIF			4000		4000	ns
279†	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDTACK}}$ in the high-impedance state		0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
280	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ low to SDDIR low (see Note 24)		0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
282b	Delay time, SDBEN low to SDTACK low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1)	If SIF register is ready (no waiting required)	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
		If SIF register is not ready (waiting required)	0	4000	0	4000	
282W	Delay time, SDDIR low to $\overline{\text{SDBEN}}$ low		0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
283W	Delay time, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high to $\overline{\text{SDBEN}}$ no longer low		0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
286	Pulse duration, $\overline{\text{SUDS}}$ or $\overline{\text{SLDS}}$ high between DIO accesses (see Note 24)		$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.

NOTES: 24. The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

25. In 80x8x mode, SRAS can be used to strobe the values of $\overline{\text{SBHE}}$, SRSX, SRS0–SRS2, and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter 266a, and $\overline{\text{SBHE}}$, SRS0–SRS2, and $\overline{\text{SCS}}$ must meet parameter 264. If SRAS is strapped high, parameters 266a and 264 are irrelevant and parameter 268 must be met.

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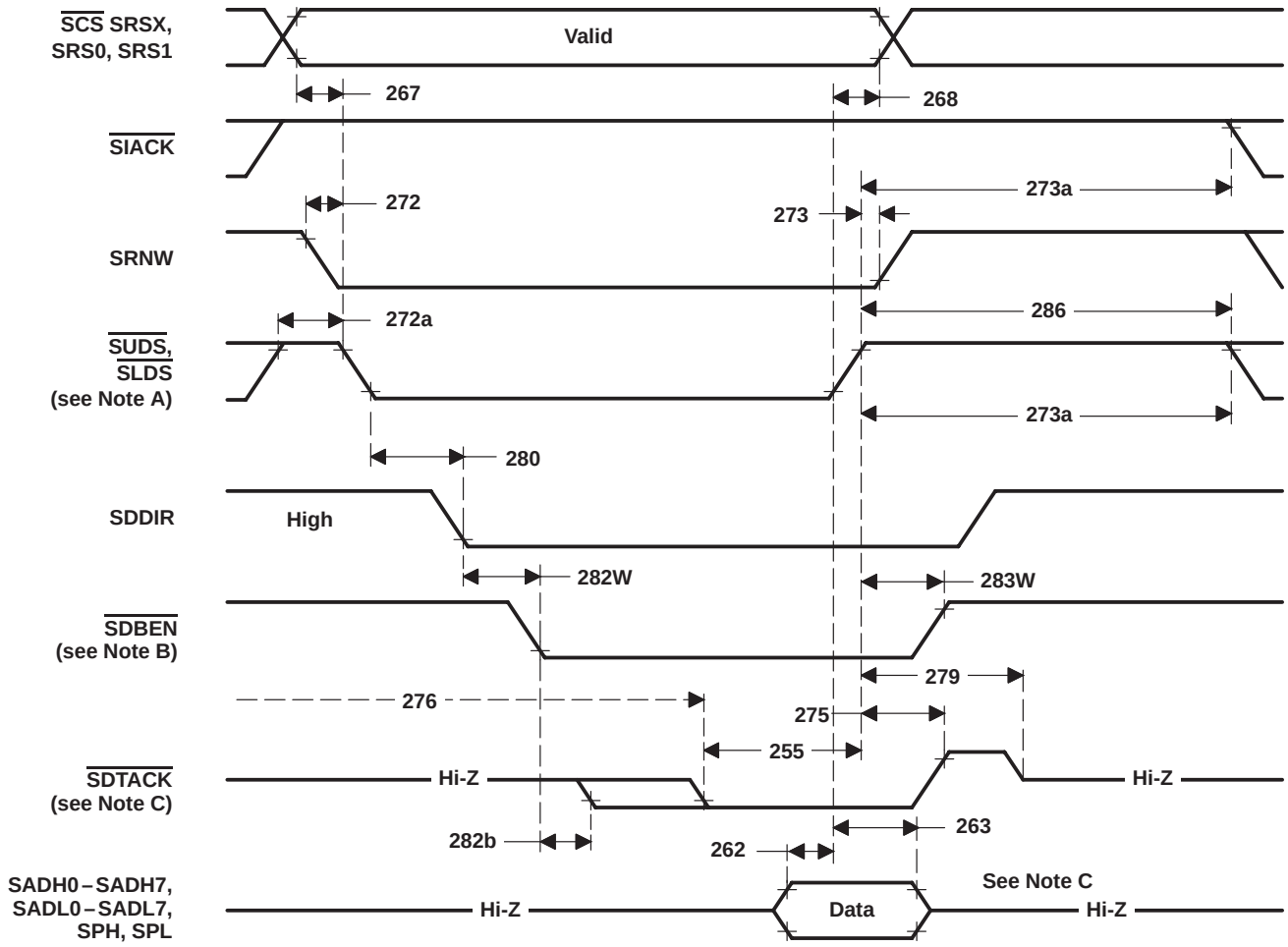

NOTES: A. For 68xxx mode, skew between $\overline{\text{SLDS}}$ and $\overline{\text{SUDS}}$ must not exceed 10 ns. Provided this limitation is observed, all events referenced to a data-strobe edge use the later occurring edge. Events defined by two data strobes edges, such as parameter 286, are measured between latest and earlier edges.

B. When the TI380C27 begins to drive $\overline{\text{SDBEN}}$ inactive, it has already latched the write data internally. Parameter 263 must be met to the input of the data buffers.

C. $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.

Figure 31. 68xxx DIO Write-Cycle Timing

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68xxx interrupt-acknowledge-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
255	Delay time, $\overline{\text{SDTACK}}$ low to either $\overline{\text{SCS}}$ or $\overline{\text{SUDS}}$, or $\overline{\text{SIACK}}$ high	15		15		ns
259†	Hold time, SAD in the high-impedance state after $\overline{\text{SIACK}}$ no longer high (see Note 24)	0		0		ns
260	Setup time, output data valid before $\overline{\text{SDTACK}}$ no longer high	0		0		ns
261†	Delay time, $\overline{\text{SIACK}}$ high to SAD in the high-impedance state (see Note 24)		35		35	ns
261a	Hold time, output data valid after $\overline{\text{SCS}}$ or $\overline{\text{SIACK}}$ no longer low (see Note 24)	0		0		ns
267§	Setup time, register address before $\overline{\text{SIACK}}$ no longer high (see Note 24)	15		15		ns
272a	Setup time, inactive high $\overline{\text{SIACK}}$ to active data strobe no longer high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
273a	Hold time, inactive SRNW high after active data strobe high	$t_{c(SCK)}$		$t_{c(SCK)}$		ns
275	Delay time, $\overline{\text{SCS}}$ or $\overline{\text{SRNW}}$ high to $\overline{\text{SDTACK}}$ high (see Note 24)	0	25	0	25	ns
276‡	Delay time, $\overline{\text{SDTACK}}$ low in the first DIO access to the SIF register to $\overline{\text{SDTACK}}$ low in the immediately following access to the SIF	0	4000	0	4000	ns
279†	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDTACK}}$ in the high-impedance state	0	$t_{c(SCK)}$	0	$t_{c(SCK)}$	ns
282a	Delay time, $\overline{\text{SDBEN}}$ low to $\overline{\text{SDTACK}}$ low in a read cycle	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
282R	Delay time, $\overline{\text{SIACK}}$ low to $\overline{\text{SDBEN}}$ low (see *TMS380 Second Generation Token-Ring User's Guide,* SPWU005, subsection 3.4.1.1.1) provided the previous cycle completed	0	$t_{c(SCK)} + 3$	0	$t_{c(SCK)} + 3$	ns
283R	Delay time, $\overline{\text{SIACK}}$ high to $\overline{\text{SDBEN}}$ high (see Note 24)	0	$t_{c(SCK)}/2 + 4$	0	$t_{c(SCK)}/2 + 4$	ns
286	Pulse duration, $\overline{\text{SIACK}}$ high between DIO accesses (see Note 24)	$t_{c(SCK)}$		$t_{c(SCK)}$		ns

† This specification is provided as an aid to board design. It is not assured during manufacturing testing.
‡ This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
§ It is the later of $\overline{\text{SRD}}$ and $\overline{\text{SRD}}$ or $\overline{\text{SCS}}$ low that indicates the start of the cycle.
NOTE 24: The inactive chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ is the inactive chip select in interrupt-acknowledge cycles.

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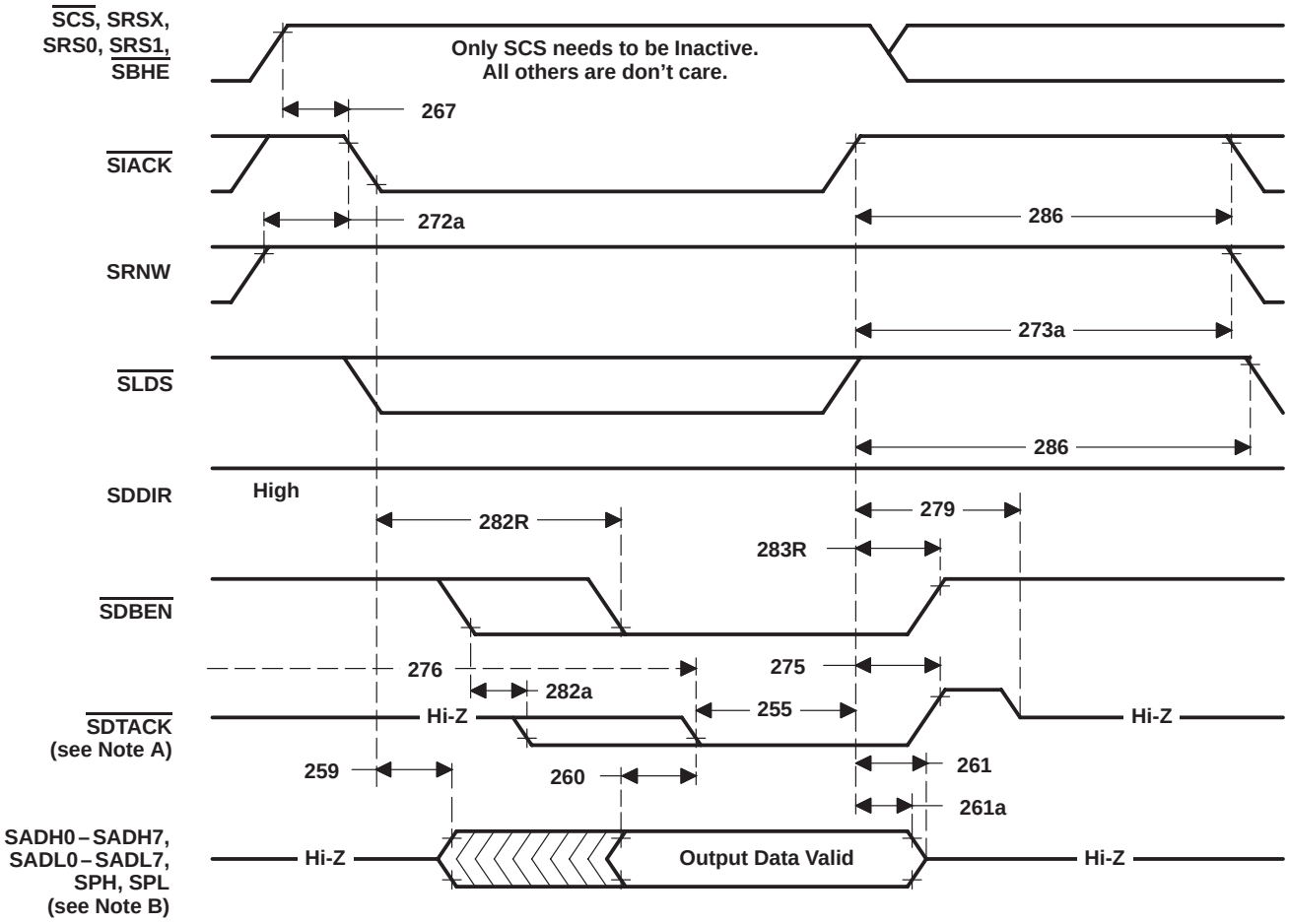

NOTES: A. $\overline{\text{SDTACK}}$ is an active-low bus ready signal. It must be asserted before data output.
B. Internal logic drives $\overline{\text{SDTACK}}$ high and verifies that it has reached a valid high level before making it a 3-state signal.

Figure 32. 68xxx Interrupt-Acknowledge-Cycle Timing

ADVANCE INFORMATION

68xxx-mode bus-arbitration timing, SIF takes control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SBGR}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBGR}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
212	Delay time, SBCLK low to address valid	0	20	0	20	ns
224a	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ low (see Note 27)	0	20	0	15	ns
224c	Delay time, SBCLK low in cycle I2 to SDDIR low in DMA read		28		23	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		20		15	ns
241	Delay time, SBCLK high in TX cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high		25		25	ns
241a†	Hold time, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ in the high-impedance state after $\overline{\text{SOWN}}$ low, bus acquisition	$t_{c(SCK)}-15$		$t_{c(SCK)}-15$		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 27: Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.

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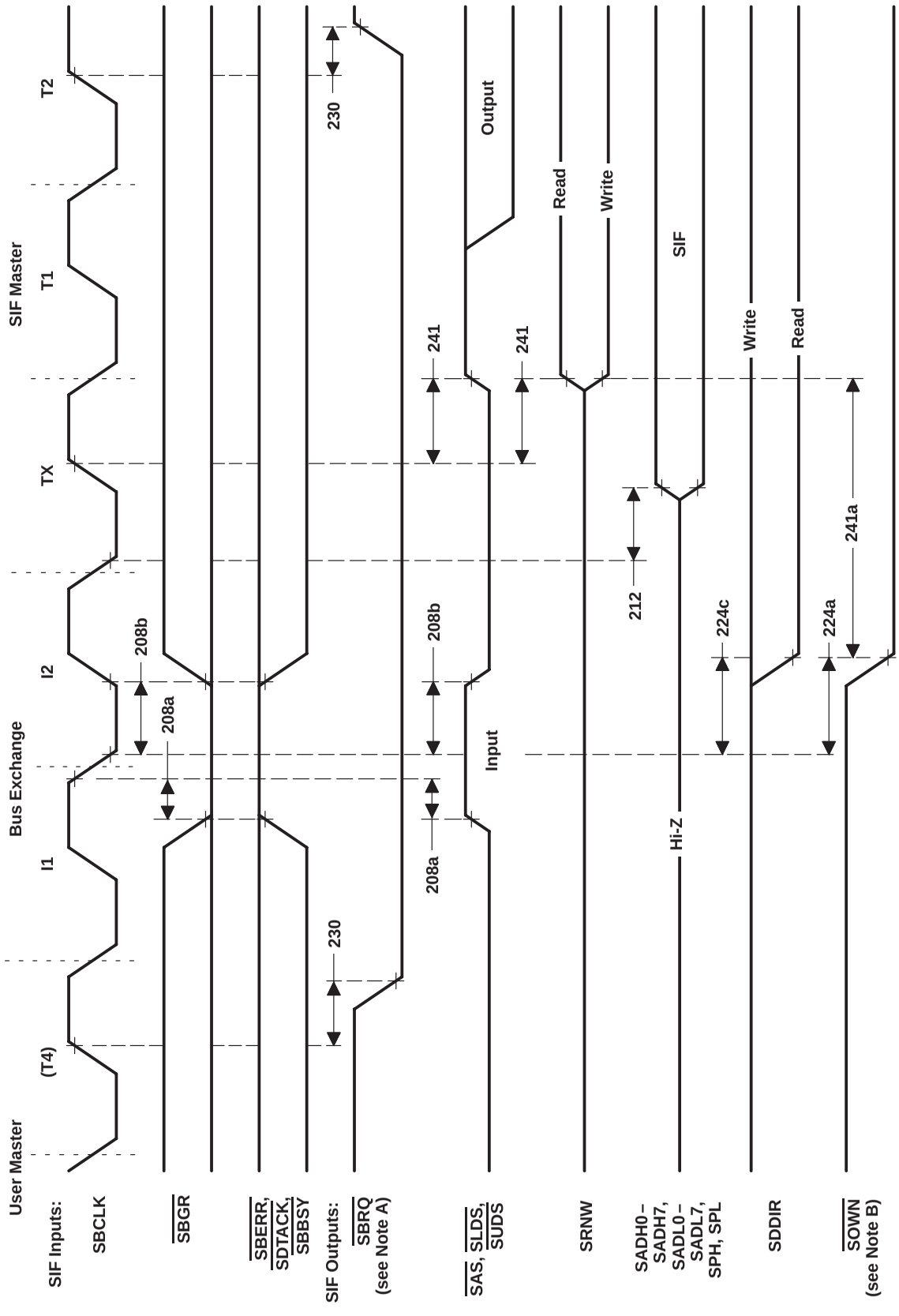

NOTES: A. In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.
B. While the system interface DMA controls are active (i.e., SOWN is asserted), the SCS input is disabled.

Figure 33. 68xxx-Mode Bus-Arbitration Timing, SIF Takes Control

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68xxx-mode DMA read-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
205	Setup time, input data valid before SBCLK in T3 cycle no longer high	10		10		ns
206	Hold time, input data valid after SBCLK low in T4 cycle if parameters 207a and 207b not met	10		10		ns
207a	Hold time, input data valid after data strobe no longer low	0		0		ns
207b	Hold time, input data valid after $\overline{\text{SDBEN}}$ no longer low	0		0		ns
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+t_{w(SCKL)}-18$		$t_{c(SCK)}+t_{w(SCKL)}-18$		ns
210	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		16		11	ns
212	Delay time, SBCLK low to address valid		20		20	ns
214†	Delay time, SBCLK low in T2 cycle to SAD in the high-impedance state		20		15	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		20		15	ns
223R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high (see Note 28)	0	16	0	11	ns
225R	Delay time, SBCLK low in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
229†	Hold time, SAD in the high-impedance state after SBCLK low in T4 cycle	0		0		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237R	Delay time, SBCLK high in the T2 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns
247	Setup time, data valid before $\overline{\text{SDTACK}}$ low if parameter 208a not met	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.
NOTE 28: While the system-interface DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), $\overline{\text{SCS}}$ is disabled.

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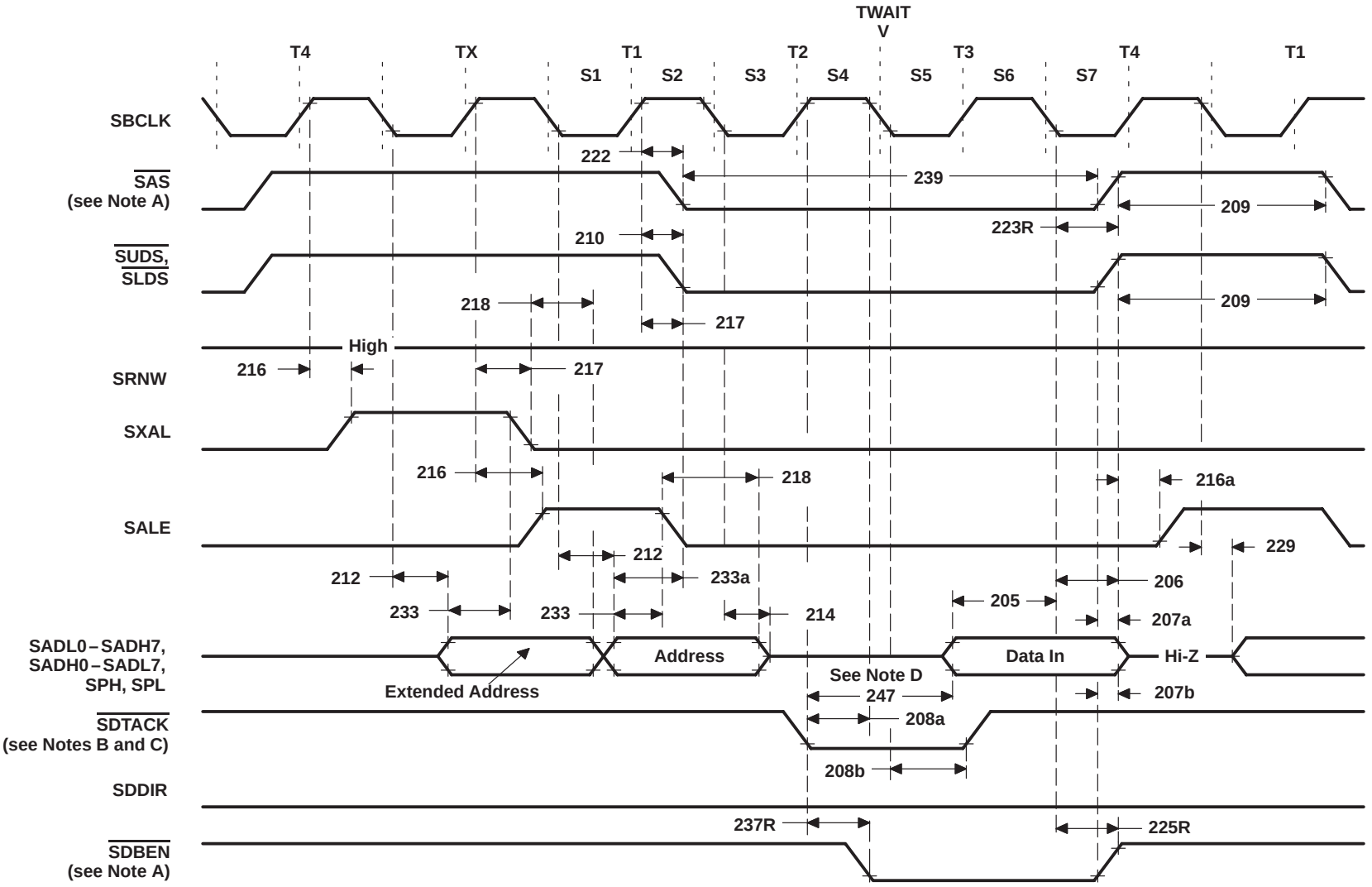

NOTES: A. Motorola-style bus slaves hold $\overline{\text{SDTACK}}$ active until the bus master deasserts $\overline{\text{SAS}}$.
B. All V_{SS} pins should be routed to minimize inductance to system ground.
C. On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data can be removed when either the read strobe or $\overline{\text{SDBEN}}$ becomes no longer active.
D. If parameter 208a is not met, valid data must be present before $\overline{\text{SDTACK}}$ goes low.

Figure 34. 68xxx-Mode DMA Read-Cycle Timing

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68xxx-mode DMA write-cycle timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input $\overline{\text{SDTACK}}$ before SBCLK no longer high to assure recognition on this cycle	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SDTACK}}$ after SBCLK low to assure recognition on this cycle	10		10		ns
209	Pulse duration, $\overline{\text{SAS}}$, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}+t_{w(SCKL)}-18$		$t_{c(SCK)}+t_{w(SCKL)}-18$		ns
211	Delay time, SBCLK high in T2 cycle to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ active		25		25	ns
211a	Delay time, output data valid to $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
212	Delay time, SBCLK low to address valid		20		20	ns
216	Delay time, SBCLK high to SALE or SXAL high		20		20	ns
216a	Hold time, SALE or SXAL low after $\overline{\text{SUDS}}$ and $\overline{\text{SAS}}$ high	0		0		ns
217	Delay time, SBCLK high to SXAL low in the TX cycle or SALE low in the T1 cycle	0	25	0	25	ns
218	Hold time, address valid after SALE, SXAL low	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	$t_{w(SCKH)}-15$	$t_{c(SCK)}/2-4$	ns
219	Delay time, SBCLK low in T2 cycle to output data and parity valid		29		29	ns
221	Hold time, output data, parity valid after $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}-12$		$t_{c(SCK)}-12$		ns
222	Delay time, SBCLK high to $\overline{\text{SAS}}$ low		20		15	ns
223W	Delay time, SBCLK low to $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, and $\overline{\text{SAS}}$ high	0	16	0	11	ns
225W	Delay time, SBCLK high in T4 cycle to $\overline{\text{SDBEN}}$ high		16		11	ns
225WH	Hold time, $\overline{\text{SDBEN}}$ low after $\overline{\text{SUDS}}$ and $\overline{\text{SLDS}}$ high	$t_{c(SCK)}/2-7$		$t_{c(SCK)}/2-7$		ns
233	Setup time, address valid before SALE or SXAL no longer high	10		10		ns
233a	Setup time, address valid before $\overline{\text{SAS}}$ no longer high	$t_{w(SCKL)}-15$		$t_{w(SCKL)}-15$		ns
237W	Delay time, SBCLK high in T1 cycle to $\overline{\text{SDBEN}}$ low		16		11	ns

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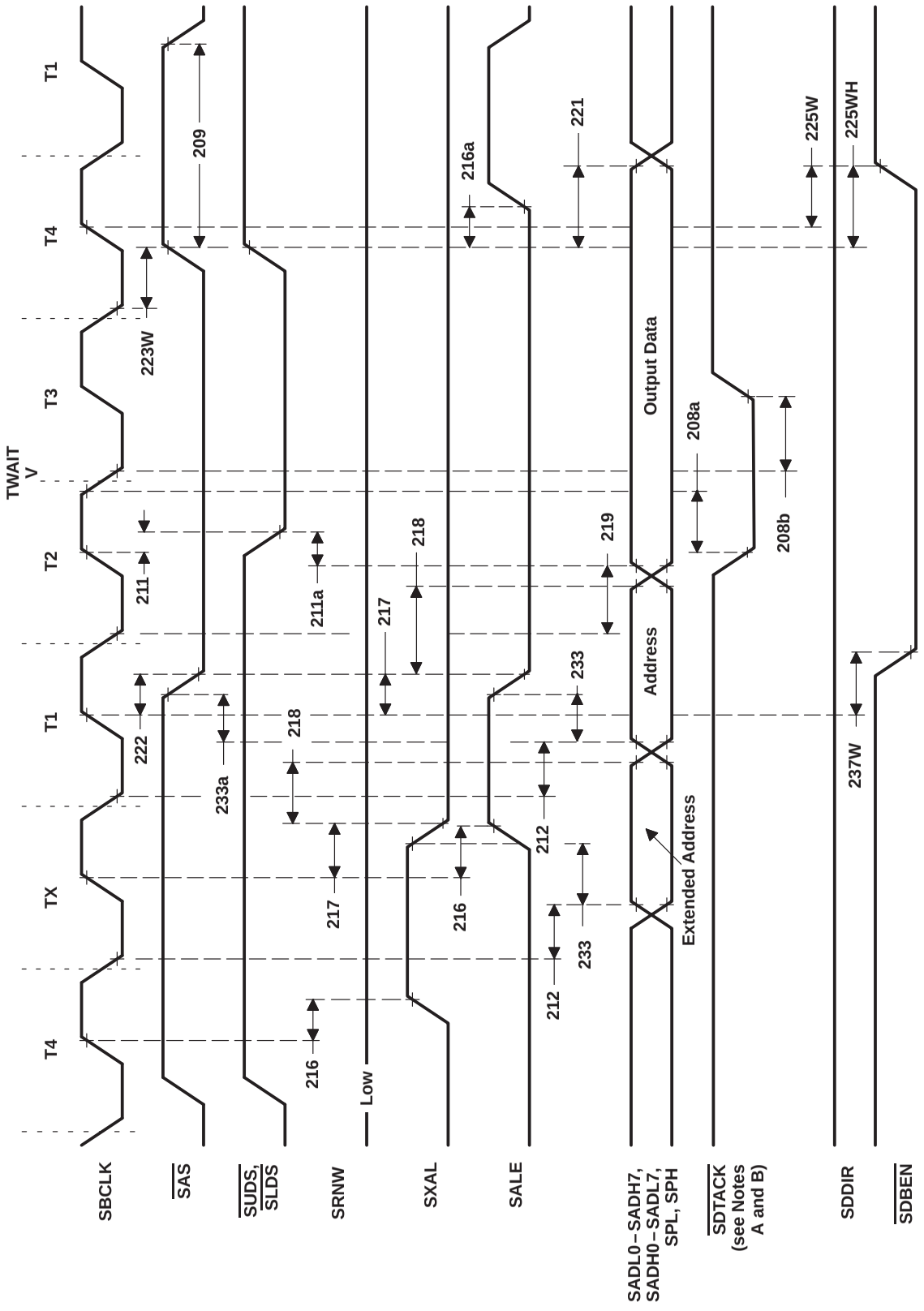

NOTES: E. All V_{SS} pins should be routed to minimize inductance to system ground.
F. On a read cycle, the read strobe remains active until the internal sample of incoming data is completed. Input data can be removed when either the read strobe or SDBEN becomes no longer active.

Figure 35. 68xxx-Mode DMA Write-Cycle Timing

68xxx-mode bus arbitration timing, SIF returns control

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
220†	Delay time, SBCLK low in I1 cycle to SAD, SPL, SPH, $\overline{\text{SUDS}}$, and $\overline{\text{SLDS}}$ in the high-impedance state, bus release		35		35	ns
223b†	Delay time, SBCLK low in I1 cycle to $\overline{\text{SBHE}}$/SRNW in the high-impedance state		45		45	ns
224b	Delay time, SBCLK low in cycle I2 to $\overline{\text{SOWN}}$ high	0	20	0	15	ns
224d	Delay time, SBCLK low in cycle I2 to SDDIR high		27		22	ns
230	Delay time, SBCLK high to either SHRQ low or $\overline{\text{SBRQ}}$ high		20		15	ns
240†	Setup from, $\overline{\text{SUDS}}$, $\overline{\text{SLDS}}$, SRNW, and $\overline{\text{SAS}}$ control signals in the high-impedance state before $\overline{\text{SOWN}}$ no longer low	0		0		ns

† This specification has been characterized to meet stated value. It is not assured during manufacturing testing.

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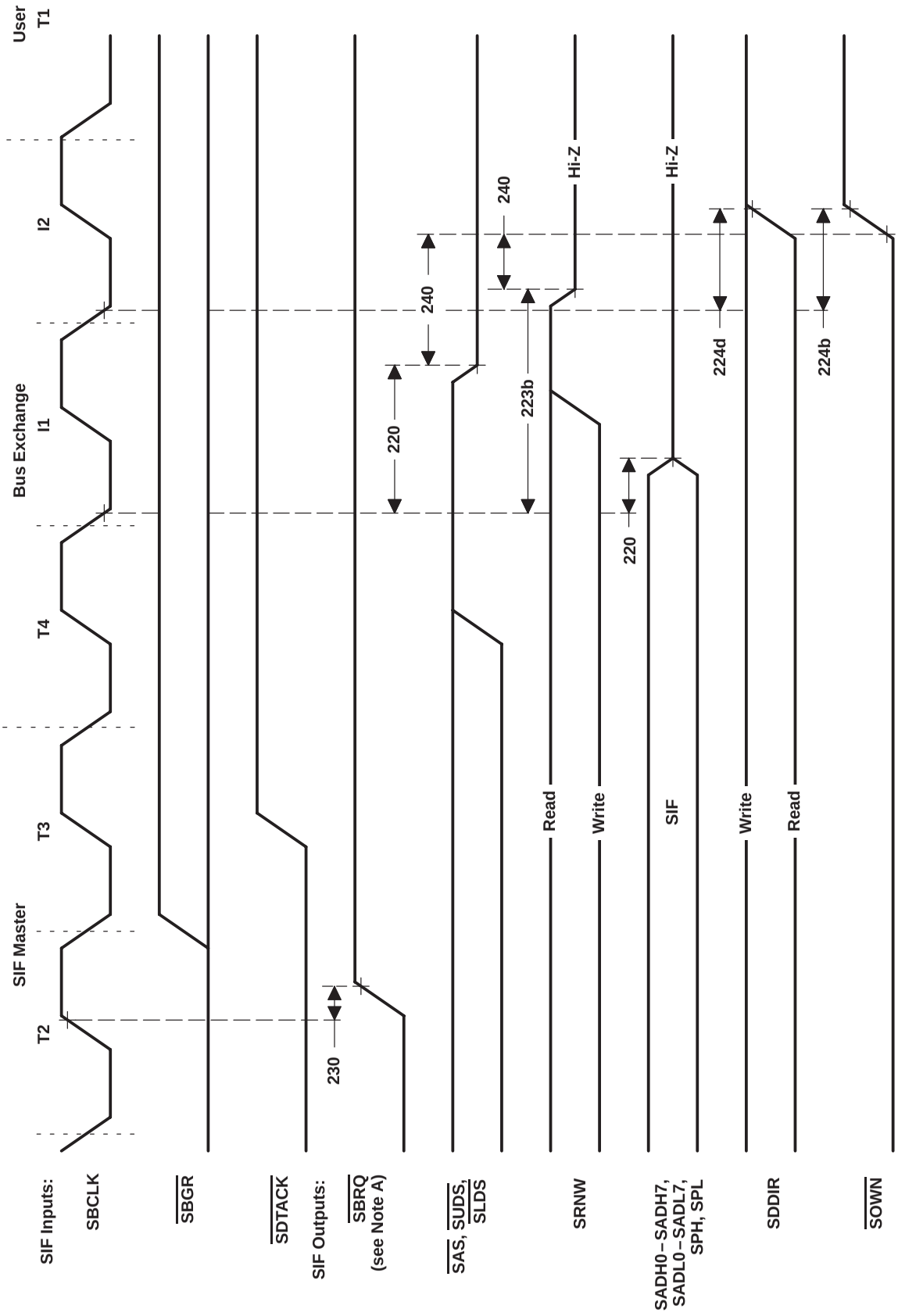
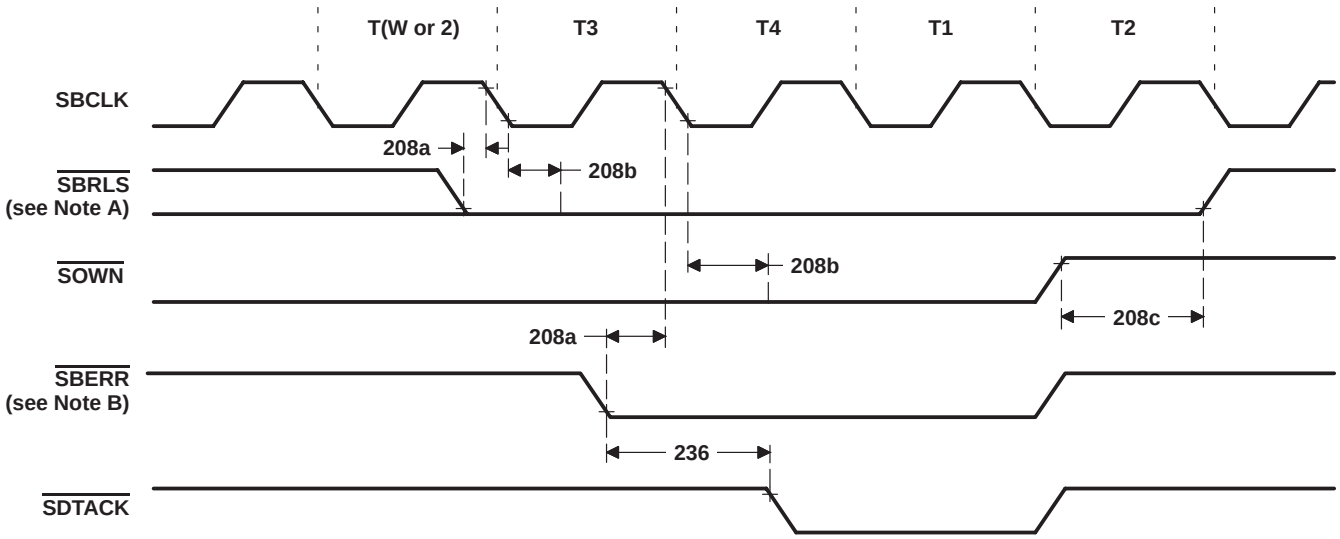


NOTE A: In 80x8x mode, the system interface deasserts SHRQ on the rising edge of SBCLK following the T4 state of the last system bus transfer it controls. In 68xxx mode, the system interface deasserts SBRQ on the rising edge of SBCLK in state T2 of the first system bus transfer it controls.

Figure 36. 68xxx-Mode Bus-Arbitration Timing, SIF Returns Control

68xxx-mode bus-release and error timing

NO.		25-MHz OPERATION		33-MHz OPERATION		UNIT
		MIN	MAX	MIN	MAX	
208a	Setup time, asynchronous input before SBCLK no longer high to assure recognition	10		10		ns
208b	Hold time, asynchronous input $\overline{\text{SBRLS}}$, $\overline{\text{SOWN}}$, or $\overline{\text{SBERR}}$ after SBCLK low to assure recognition	10		10		ns
208c	Hold time, $\overline{\text{SBRLS}}$ low after $\overline{\text{SOWN}}$ high	0		0		ns
236	Setup time, $\overline{\text{SBERR}}$ low before $\overline{\text{SDTACK}}$ no longer high if parameter 208a not met	30		30		ns



NOTES: A. The system interface ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the bus when it detects the assertion of $\overline{\text{SBRLS}}$, it completes any internally started DMA cycle and relinquishes control of the bus. If no DMA transfer has internally started, the system interface releases the bus before starting another.

B. If $\overline{\text{SBERR}}$ is asserted when the system interface controls the system bus, the current bus transfer is completed, regardless of the value of $\overline{\text{SDTACK}}$. If the BERETRY register is nonzero, the cycle is retried. If the BERETRY register is zero, the system interface then releases control of the system bus. The system interface ignores the assertion of $\overline{\text{SBERR}}$ if it is not performing a DMA bus cycle on the system bus. When $\overline{\text{SBERR}}$ is properly asserted and BERETRY is zero, however, the system interface releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the local bus and DMA stops on the local sides. The value of the SDMAADR, SDMADDRX, and SDMALEN registers in the system interface are not defined after a system-bus error.

C. In cycle-steal mode, state TX is present on every system-bus transfer. In burst mode, state TX is present on the first bus transfer and whenever the increment of the DMA address register carries beyond the least significant 16 bits.

D. $\overline{\text{SDTACK}}$ is not sampled to verify that it is deasserted.

E. Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including high impedance) until the start of that SBCLK transition.

Figure 37. 68xxx-Mode Bus-Release and Error Timing

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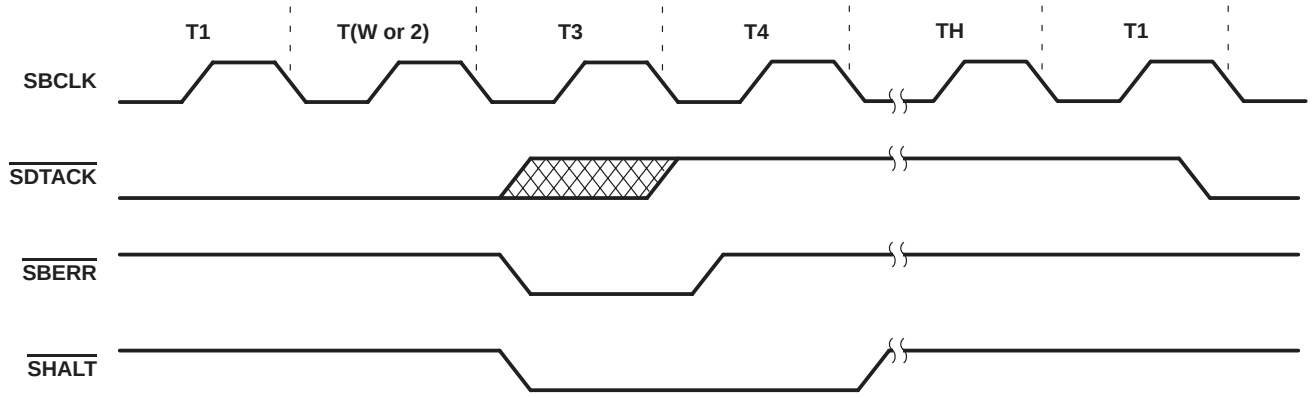
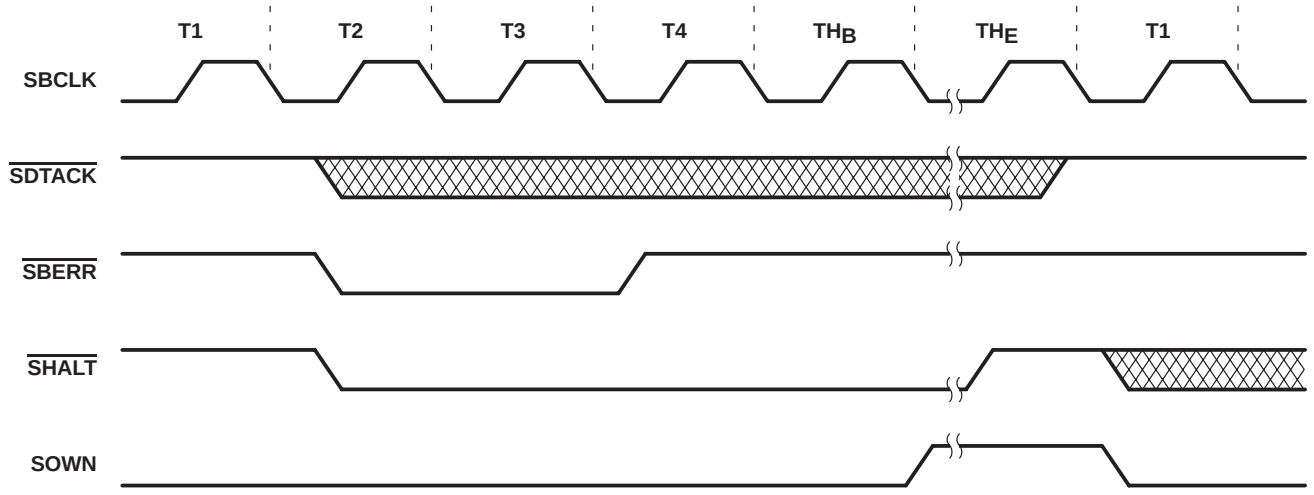


NOTE A: Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement may vary from waveforms shown.

Figure 38. 68xxx-Mode Bus-Halt and Retry, Normal Completion With Delayed Start



NOTE A: Only the relative placement of the edges to SBCLK falling edge is shown. Actual signal edge placement may vary from waveforms shown.

Figure 39. 68xxx-Mode Bus-Halt and Retry, Rerun Cycle With Delayed Start

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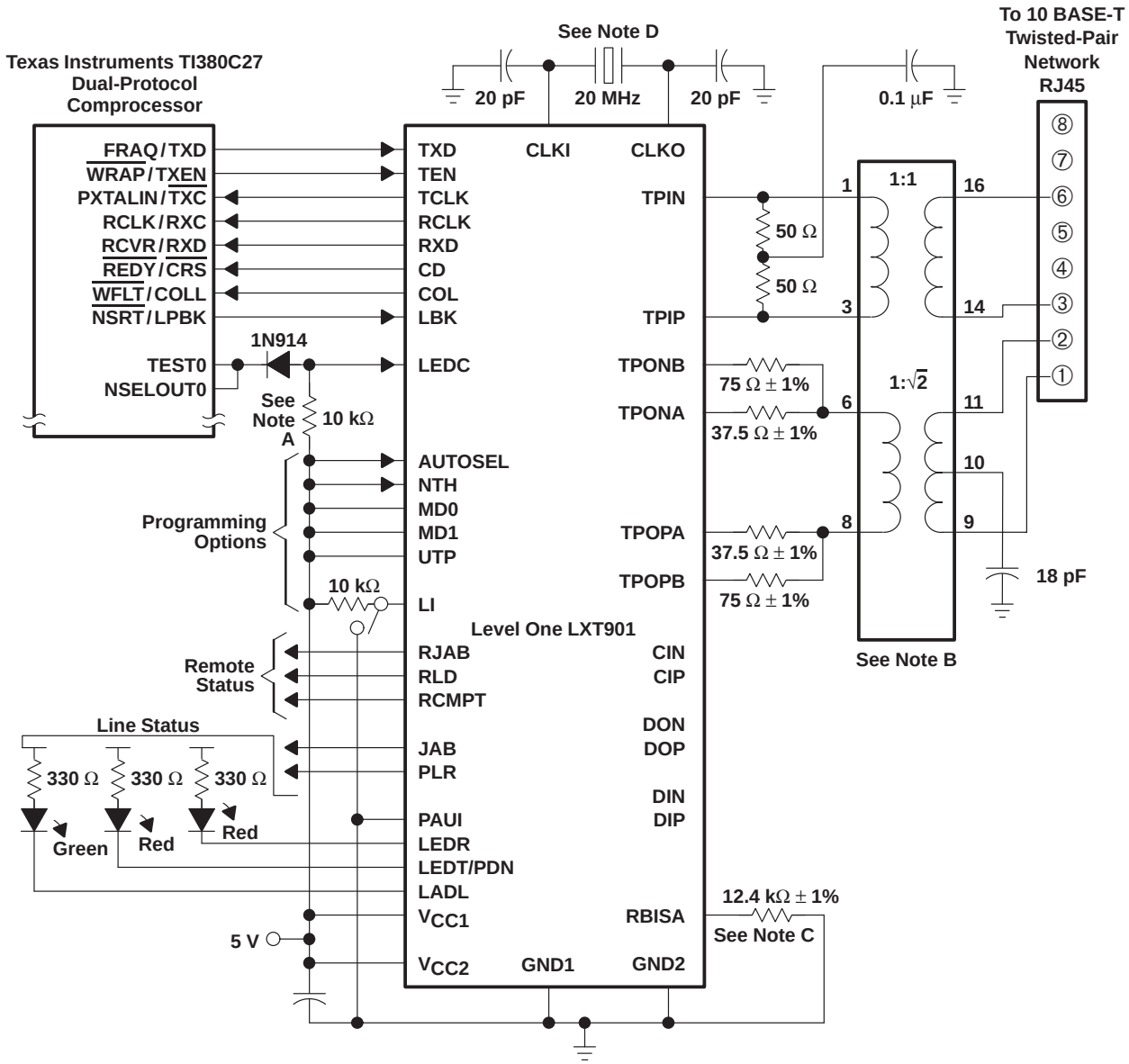
APPLICATION INFORMATION

Figure 40 shows the TI380C27 connected to a LEVEL ONE LXT901™ universal Ethernet interface adapter. The LXT901 provides all of the active circuitry for interfacing the TI380C27 to the 10 Base-T twisted-pair network.



NOTES: A. Half/full duplex selection controlled by TI380C27 pins TEST0 and NSELOUT0.
NSELOUT0 = L (full duplex)
NSELOUT0 = H (half duplex)
For half-duplex operation, diode 1N914 and associate 10-kΩ resistor are not needed: these components can be removed.

B. Suitable TP transformers include the Fil-Mag 23Z128, and SM23Z128; Valor PT4069 and ST7011; Pulse Engineering PE65994 and PE65745; Belfuse S553-0716 and A553-0716; and Halo Electronics TD42-2006Q and TD42-2006W1.

C. RBIAS should be located close to the pin and isolated from other signals.

D. Suitable crystals include the MTRON MP-1 and MP-2.

Figure 40. Typical Schematic for Full-Duplex Operation With the TI380C27

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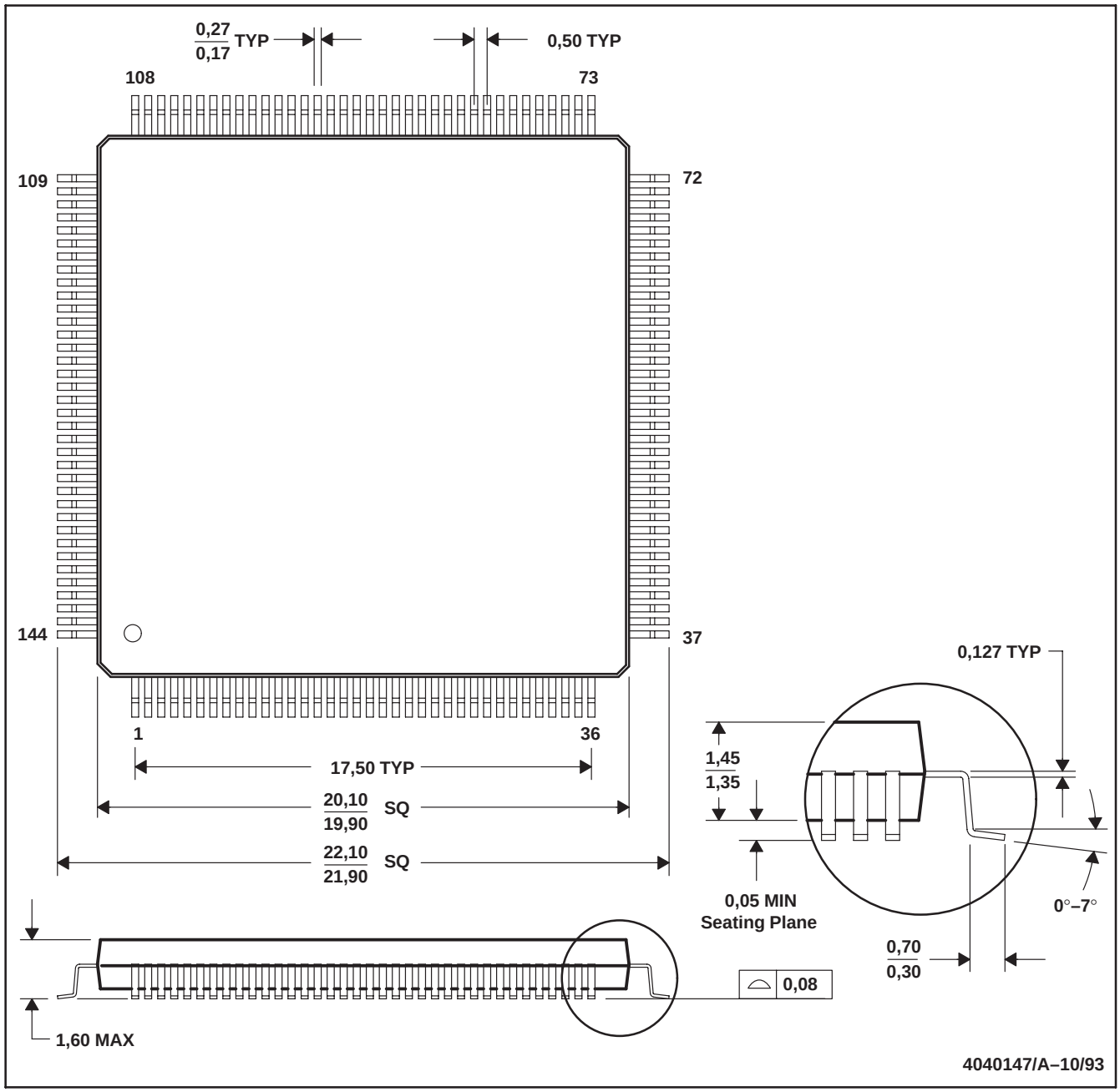
MECHANICAL DATA

PGE/S-PQFP-G144 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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