

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J114TU

- High-Speed Switching Applications
- Power Management Switch Applications

- 1.5 V drive
- Low on-resistance

$$\begin{aligned}
 R_{on} &= 526 \text{ m}\Omega \text{ (max)} (@ V_{GS} = -1.5 \text{ V}) \\
 R_{on} &= 321 \text{ m}\Omega \text{ (max)} (@ V_{GS} = -1.8 \text{ V}) \\
 R_{on} &= 199 \text{ m}\Omega \text{ (max)} (@ V_{GS} = -2.5 \text{ V}) \\
 R_{on} &= 149 \text{ m}\Omega \text{ (max)} (@ V_{GS} = -4.0 \text{ V})
 \end{aligned}$$

Absolute Maximum Ratings (Ta = 25°C)

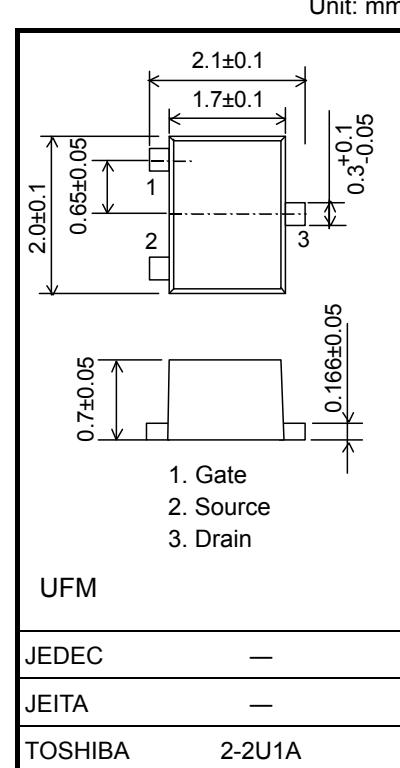
Characteristics	Symbol	Rating	Unit
Drain-Source voltage	V _{DS}	-20	V
Gate-Source voltage	V _{GSS}	± 8	V
Drain current	DC	I _D	A
	Pulse	I _{DP}	
Drain power dissipation	P _D (Note 1)	800	mW
	P _D (Note 2)	500	
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

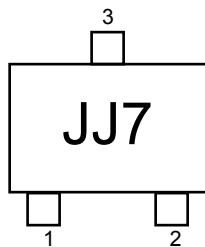
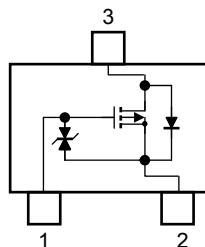
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Mounted on ceramic board
(25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 mm²)

Note 2: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm²)



Weight: 6.6 mg (typ.)

Marking**Equivalent Circuit (top view)**Start of commercial production
2005-10

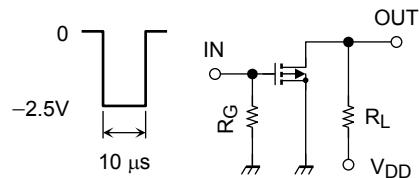
Electrical Characteristics ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$I_D = -1 \text{ mA}, V_{GS} = 0$	-20	—	—	V
	$V_{(\text{BR})\text{DSX}}$	$I_D = -1 \text{ mA}, V_{GS} = +8 \text{ V}$	-12	—	—	
Drain cut-off current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0$	—	—	-10	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$	—	—	± 1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	—	-1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -0.6 \text{ A}$ (Note 3)	1.9	3.9	—	S
Drain-Source ON-resistance	$R_{\text{DS}(\text{ON})}$	$I_D = -0.6 \text{ A}, V_{GS} = -4.0 \text{ V}$ (Note 3)	—	100	149	$\text{m}\Omega$
		$I_D = -0.6 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note 3)	—	133	199	
		$I_D = -0.6 \text{ A}, V_{GS} = -1.8 \text{ V}$ (Note 3)	—	183	321	
		$I_D = -0.1 \text{ A}, V_{GS} = -1.5 \text{ V}$ (Note 3)	—	220	526	
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0$ $f = 1 \text{ MHz}$	—	331	—	pF
Output capacitance	C_{oss}		—	48	—	pF
Reverse transfer capacitance	C_{rss}		—	39	—	pF
Switching time	Turn-on time	t_{on}	$V_{DD} = -10 \text{ V}, I_D = -0.6 \text{ A}$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_G = 4.7 \Omega$	—	19	ns
	Turn-off time	t_{off}		—	18	
Total gate charge	Q_g	$V_{DS} = -16 \text{ V}, I_{DS} = -1.2 \text{ A}$ $V_{GS} = -4 \text{ V}$	—	7.7	—	nC
Gate-Source charge	Q_{gs}		—	4.9	—	
Gate-Drain charge	Q_{gd}		—	2.8	—	
Drain-Source forward voltage	V_{DSF}	$I_D = 1.8 \text{ A}, V_{GS} = 0$ (Note 3)	—	0.8	1.2	V

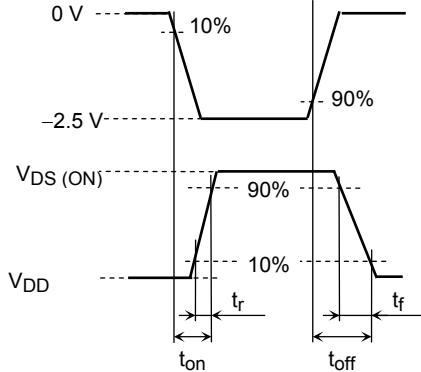
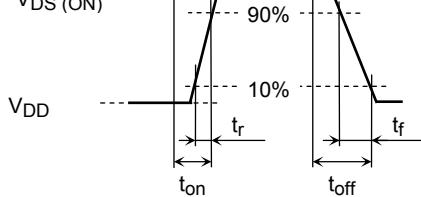
Note 3: Pulse test

Switching Time Test Circuit

(a) Test Circuit



$V_{DD} = -10 \text{ V}$
 $R_G = 4.7 \Omega$
Duty $\leq 1\%$
 $V_{IN}: t_r, t_f < 5 \text{ ns}$
Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN} (c) V_{OUT} 

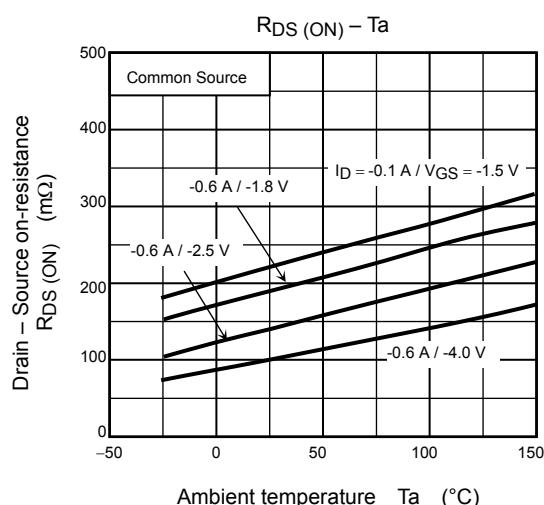
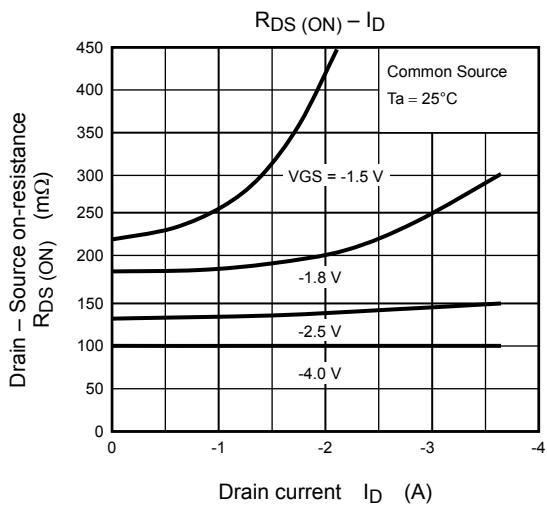
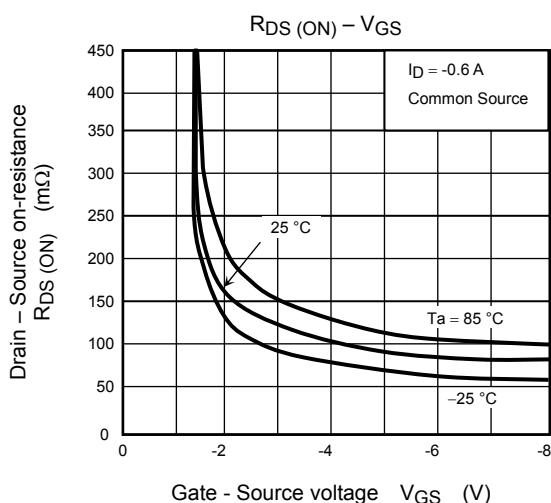
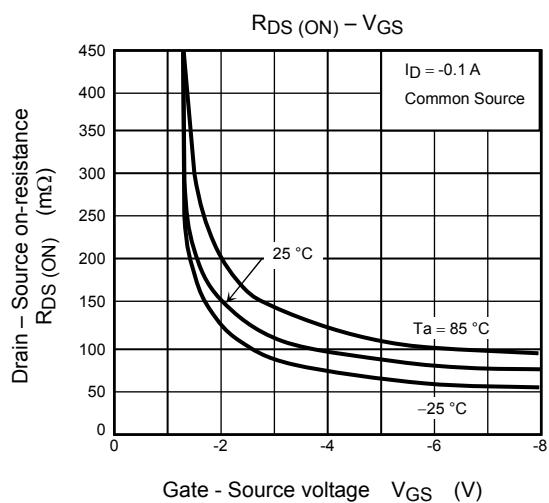
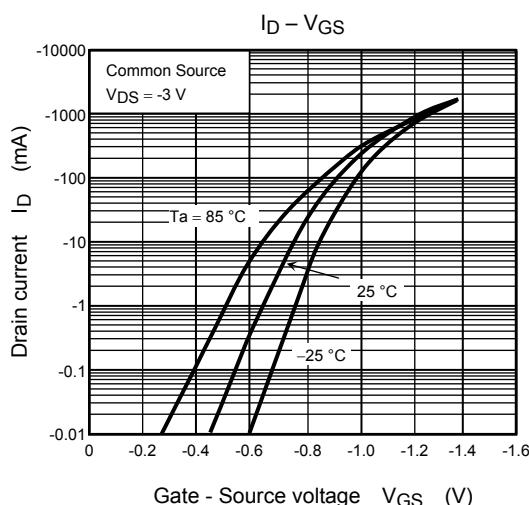
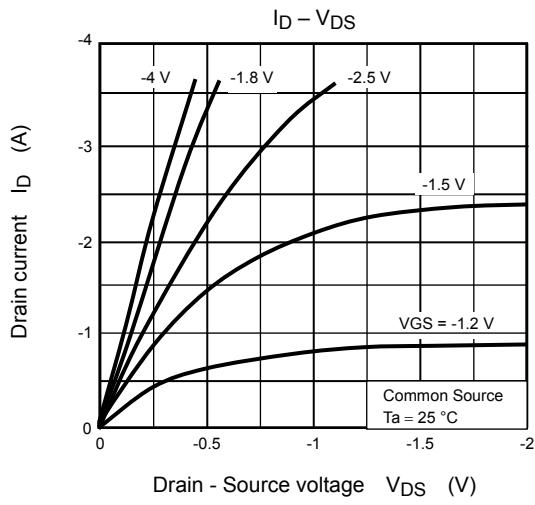
Precaution

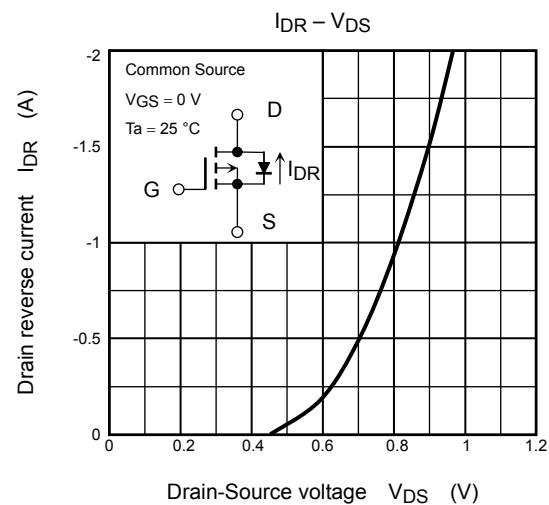
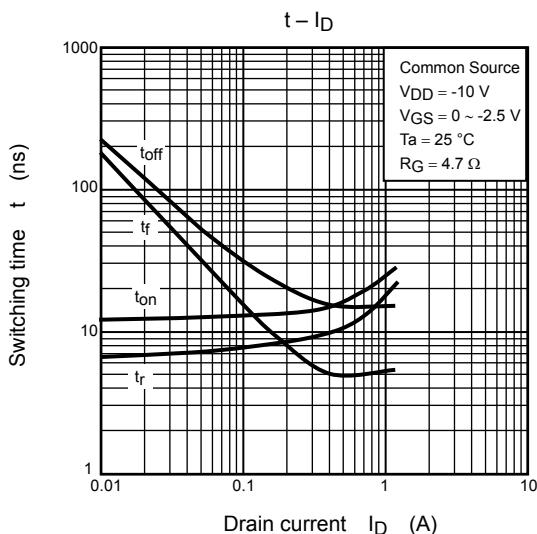
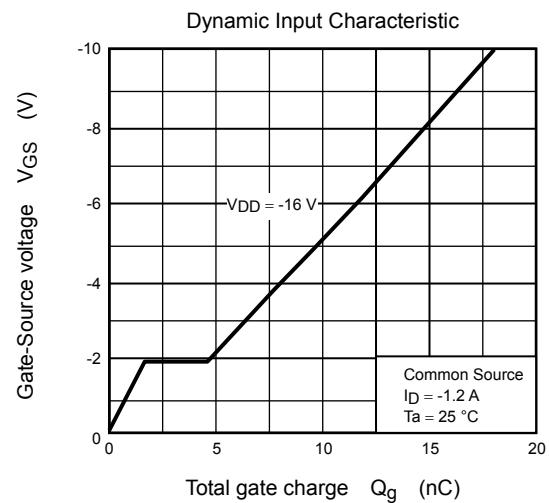
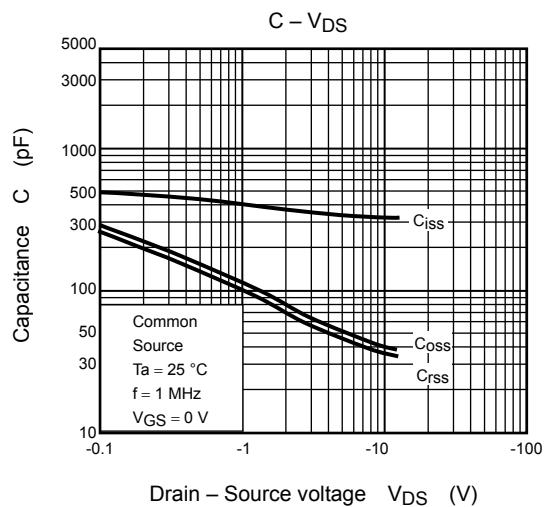
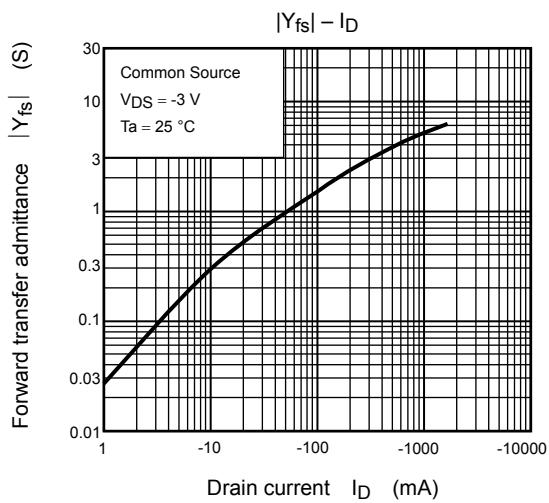
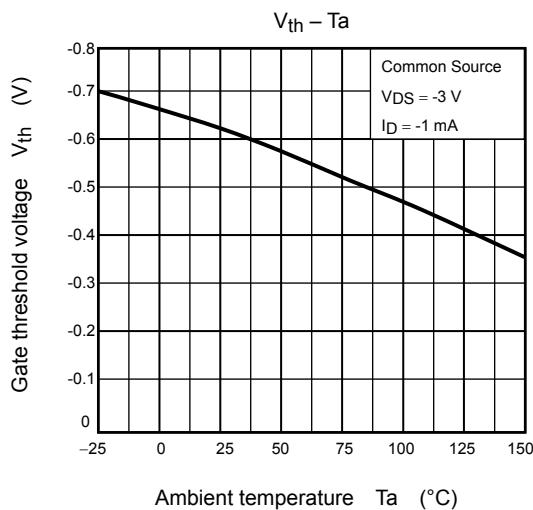
V_{th} can be expressed as the voltage between the gate and source when the low operating current value is $I_D = -1\text{mA}$ for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} . (The relationship can be established as follows: V_{GS} (off) $< V_{\text{th}} < V_{GS}$ (on).)

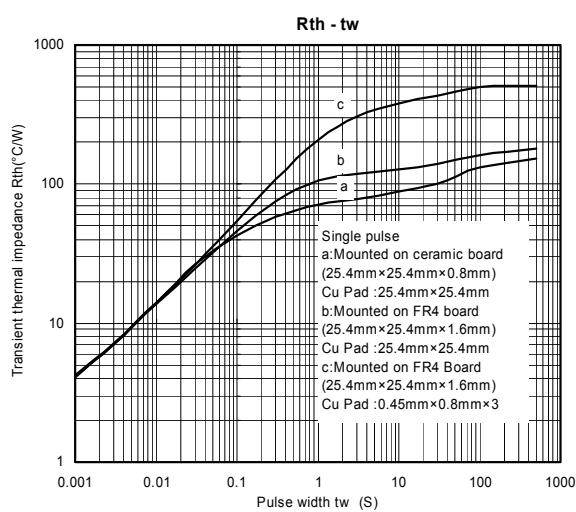
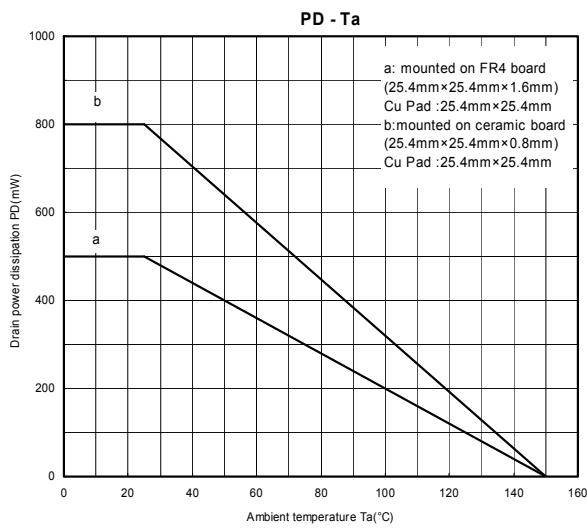
Be sure to take this into consideration when using the device.

Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.







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