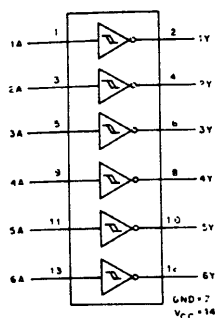


CD54/74HC14

CD54/74HCT14

File Number 1781

High-Speed CMOS Logic



Hex Inverting Schmitt Trigger

Type Features:

- Unlimited input rise and fall times
- Exceptionally high noise immunity

FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

The RCA-CD54/74HC14 and CD54/74HCT14 each contain 6 inverting Schmitt Triggers in one package.

The CD54HC14 and CD54HCT14 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC14 and CD74HCT14 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip form (H suffix).



LOGIC DIAGRAM

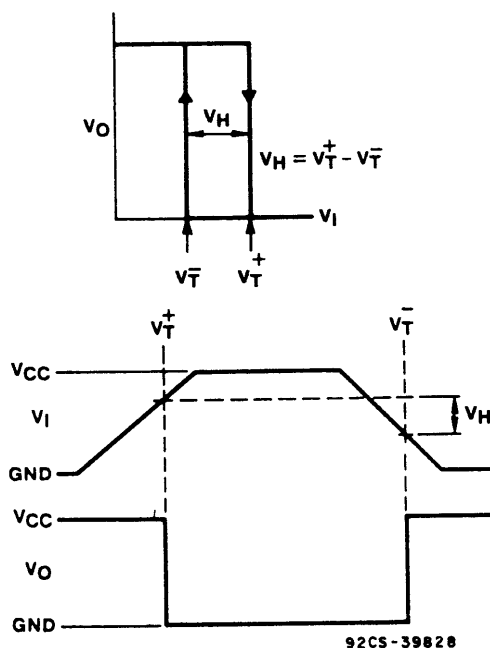


Fig 1 - Hysteresis definition, characteristic, and test setup.

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Sigmetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 37\%$, $N_{IH} = 51\%$ of V_{CC} @ $V_{CC} = 5V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $N_{IL} = 18\%$, $N_{IH} = 67\%$ of V_{CC} @ $V_{CC} = 4.5V$
CMOS Input Compatibility
 $I_I \leq 1 \mu A$ @ V_{OL} , V_{OH}

TRUTH TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = High Level
L = Low Level

CD54/74HC14

CD54/74HCT14

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	-0.5 to +7 V
(Voltages referenced to ground)	
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D)	500 mW
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	400 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	
OPERATING-TEMPERATURE RANGE (T_A)	-55 to $+125^\circ\text{C}$
PACKAGE TYPE F, H	-40 to $+85^\circ\text{C}$
PACKAGE TYPE E, M	-65 to $+150^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	
LEAD TEMPERATURE (DURING SOLDERING)	$+265^\circ\text{C}$
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max	
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)	$+300^\circ\text{C}$
with solder contacting lead tips only	

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC} .*	2	6	V
CD54/74HC Types	4.5	5.5	V
CD54/74HCT Types	0	V_{CC}	V
DC Input or Output Voltage V_i , V_o			
Operating Temperature T_A	-40	+85	$^\circ\text{C}$
CD74 Types	-55	+125	$^\circ\text{C}$
CD54 Types			
Input Rise and Fall Times t_r , t_f	0	Unlimited	ns
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V			

*Unless otherwise specified, all voltages are referenced to Ground

CD54/74HC14

CD54/74HCT14

STATIC ELECTRICAL CHARACTERISTICS

STATIC ELECTRICAL CHARACTERISTICS																			
CHARACTERISTIC	CD74HC14/CD54HC14									CD74HCT14/CD54HCT14									UNITS
	TEST CONDITIONS			74HC/54HC TYPES		74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES		74HCT TYPE		54HCT TYPE			
	V _I V	I _O mA	V _{CC} V	+25°C		-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C		-40/ +85°C		-55/ +125°C			
				Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max		
Input Switch Points	V _{I+}			2	0.7	1.5	0.7	1.5	0.7	1.5			—	—	—	—	—	—	V
				4.5	1.7	3.15	1.7	3.15	1.7	3.15		4.5	1.2	1.9	1.2	1.9	1.2	1.9	
				6	2.1	4.2	2.1	4.2	2.1	4.2		5.5	1.4	2.1	1.4	2.1	1.4	2.1	
				2	0.3	1	0.3	1	0.3	1			—	—	—	—	—	—	
				4.5	0.9	2.2	0.9	2.2	0.9	2.2		4.5	0.5	1.2	0.5	1.2	0.5	1.2	V
				6	1.2	3	1.2	3	1.2	3		5.5	0.6	1.4	0.6	1.4	0.6	1.4	
				2	0.2	1	0.2	1	0.2	1			—	—	—	—	—	—	
				4.5	0.4	1.4	0.4	1.4	0.4	1.4		4.5	0.4	1.4	0.4	1.4	0.4	1.4	V
				6	0.6	1.6	0.6	1.6	0.6	1.6		5.5	0.4	1.5	0.4	1.5	0.4	1.5	
High-Level Output Voltage	V _{I-}			2	1.9	—	1.9	—	1.9	—	V _{I-}		—	—	—	—	—	—	
CMOS Loads	V _{OH}	-0.02		4.5	4.4	—	4.4	—	4.4	—	or	4.5	4.4	—	4.4	—	4.4	—	V
	V _{I+}			6	5.9	—	5.9	—	5.9	—	V _{I+}		—	—	—	—	—	—	
TTL Loads	V _{I-}			—	—	—	—	—	—	—	V _{I-}		—	—	—	—	—	—	
	or	-4	4.5	3.98	—	3.84	—	3.7	—	—	or	4.5	3.98	—	3.84	—	3.7	—	V
	V _{I+}	-5.2	6	5.48	—	5.34	—	5.2	—	—	V _{I+}		—	—	—	—	—	—	
Low-Level Output Voltage	V _{I-}			2	—	0.1	—	0.1	—	0.1	V _{I-}		—	—	—	—	—	—	
CMOS Loads	V _{OL}	0.02		4.5	—	0.1	—	0.1	—	0.1	or	4.5	—	0.1	—	0.1	—	0.1	V
	V _{I+}			6	—	0.1	—	0.1	—	0.1	V _{I+}		—	—	—	—	—	—	
TTL Loads	V _{I-}			—	—	—	—	—	—	—	V _{I-}		—	—	—	—	—	—	
	or	4	4.5	—	0.26	—	0.33	—	0.4	—	or	4.5	—	0.26	—	0.33	—	0.4	V
	V _{I+}	5.2	6	—	0.26	—	0.33	—	0.4	—	V _{I+}		—	—	—	—	—	—	
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	2	—	20	—	40	V _{CC} or Gnd	5.5	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin 1 unit load ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	Min Typ Max	—	450	—	490	μA	

*For dual-supply systems theoretical worst case ($V_i = 2.4$ V, $V_{cc} = 5.5$ V) specification is 1.8 mA

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
nA	0.6

*Unit load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max @ 25°C.

CD54/74HC14

CD54/74HCT14

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input t_r , $t_f = 6\text{ ns}$)

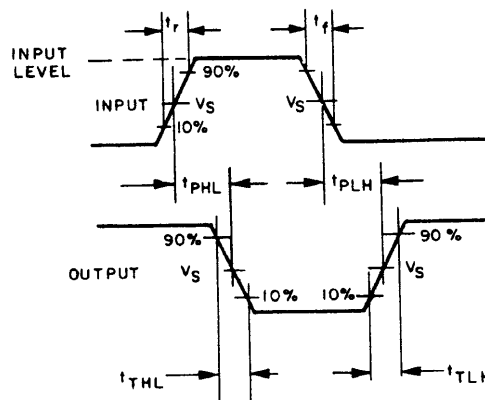
CHARACTERISTIC	CL (pF)	TYPICAL HC HCT		UNITS
Propagation Delay, A to Y t_{PLH}, t_{PLH}	15	11	16	ns
Power Dissipation Capacitance* C_{PD}	—	20	20	pF

* C_{PD} is used to determine the dynamic power consumption, per inverter.

$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input t_r , $t_f = 6\text{ ns}$)

SWITCHING CHARACTERISTICS (CL = 10 pF, TA = 25°C)															
CHARACTERISTIC	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS	
		HC		HCT		74HC		74HCT		54HC		54HCT			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay, A to Y	t _{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	ns
	t _{PHL}	4.5	—	27	—	38	—	34	—	48	—	41	—	57	
		6	—	23	—	—	—	29	—	—	—	35	—	—	
Output Transition Time	t _{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t _{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C ₁	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

92CS-36948RI

Fig. 2 - Transition times and propagation delay times.