

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ max}$	$I_D \text{ max}$ $T_A = +25^\circ\text{C}$
-30V	14m Ω @ $V_{GS} = 10\text{V}$	-12.0A
	25m Ω @ $V_{GS} = 4.5\text{V}$	-8.5A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

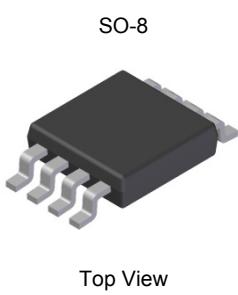
- Backlighting
- Power Management Functions
- DC-DC Converters

Features

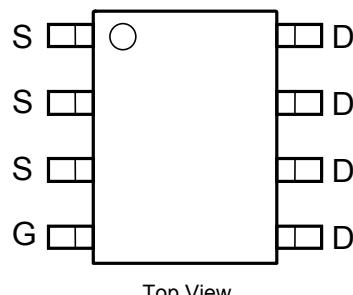
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

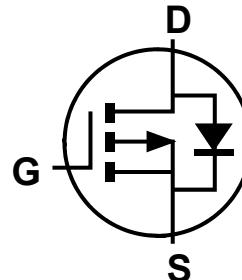
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074g (approximate)



Top View



Top View
Internal Schematic



Equivalent circuit

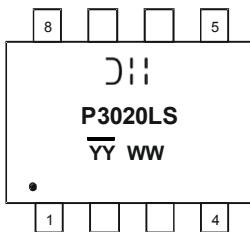
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3020LSS-13	SO-8	2500/Tape & Reel

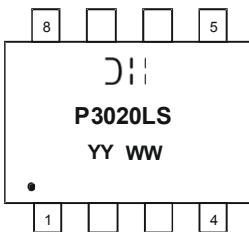
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

Marking Information



Chengdu A/T Site



Shanghai A/T Site

○ = Manufacturer's Marking

P3020LS = Product Type Marking Code

YYWW = Date Code Marking

YY or YY = Year (ex: 13 = 2013)

WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	± 25	V
Drain Current (Note 5)	Steady State	$T_A = +25^\circ\text{C}$	I_D	-12
		$T_A = +70^\circ\text{C}$		-6
Pulsed Drain Current (Note 6)		I_{DM}	-40	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	2.5	W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
		—	—	± 800		$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(\text{th})}$	-1	—	-2	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	11.6	14	$\text{m}\Omega$	$V_{GS} = -10\text{V}, I_D = -8\text{A}$
		—	18.6	25		$V_{GS} = -4.5\text{V}, I_D = -5\text{A}$
Forward Transconductance	g_{fs}	—	12	—	S	$V_{DS} = -10\text{V}, I_D = -12\text{A}$
Diode Forward Voltage (Note 7)	V_{SD}	-0.5	—	-1.1	V	$V_{GS} = 0\text{V}, I_S = -2\text{A}$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	1802	—	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	415	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	295	—	pF	
Gate Resistance	R_G	—	2.3	—	Ω	$V_{GS} = 0\text{V}, V_{DS} = 0\text{V}, f = \text{MHz}$
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_g	—	15.3	—	nC	$V_{DS} = -15\text{V}, V_{GS} = -4.5\text{V}, I_D = -8\text{A}$
		—	30.7	—		$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -8\text{A}$
Gate-Source Charge	Q_{gs}	—	3.5	—		$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -8\text{A}$
Gate-Drain Charge	Q_{gd}	—	7.9	—		$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -8\text{A}$
Turn-On Delay Time	$t_{d(on)}$	—	5.1	—	ns	$V_{GS} = -10\text{V}, V_{DS} = -15\text{V}, R_D = 15\Omega, R_G = 6\Omega$
Rise Time	t_r	—	8	—		
Turn-Off Delay Time	$t_{d(off)}$	—	46	—		
Fall Time	t_f	—	30	—		

Notes: 5. Device mounted on 2 oz. Copper pads on FR-4 PCB with $R_{\theta JA} = 50^\circ\text{C}/\text{W}$.

6. Pulse width $\leq 10\mu\text{s}$, Duty Cycle $\leq 1\%$.

7. Short duration pulse test used to minimize self-heating effect.

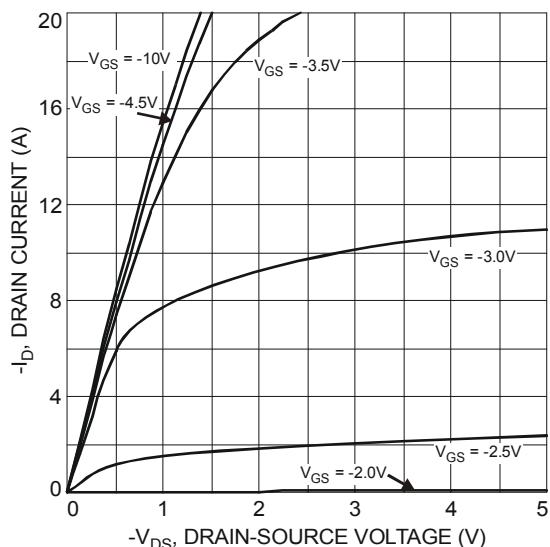


Fig. 1 Typical Output Characteristic

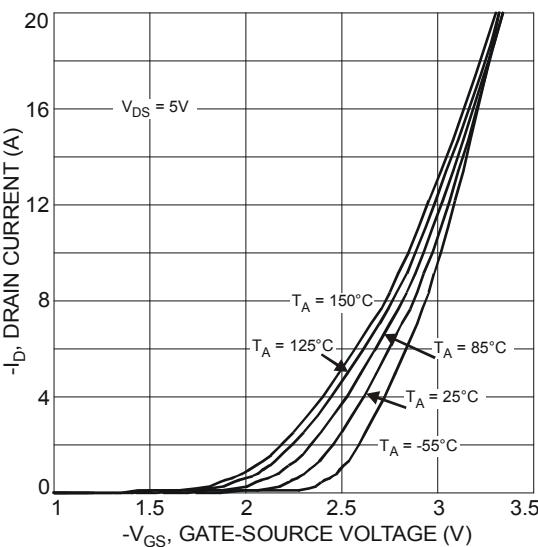
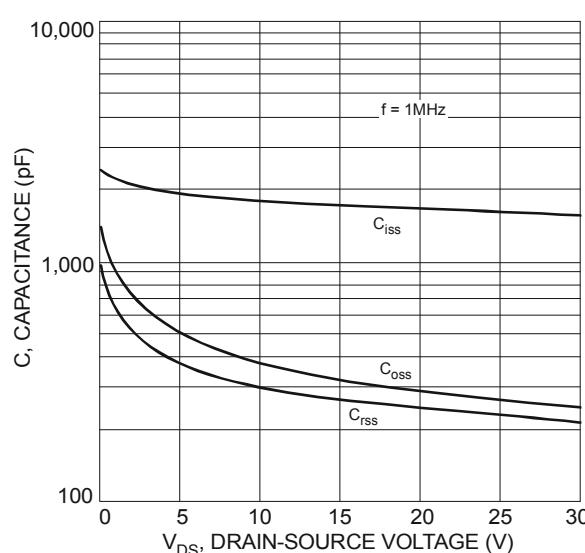
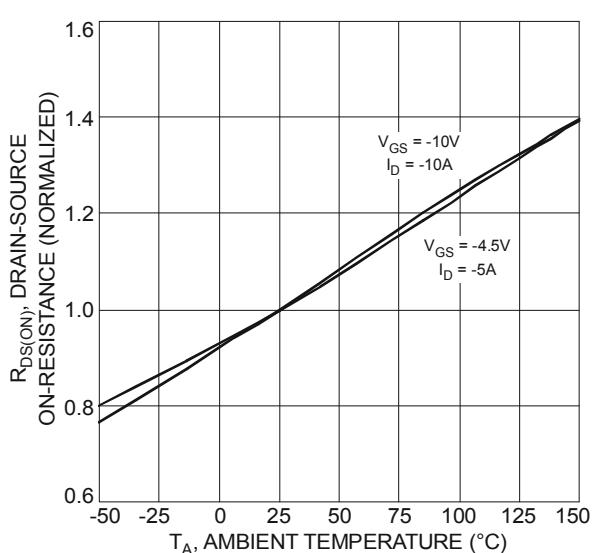
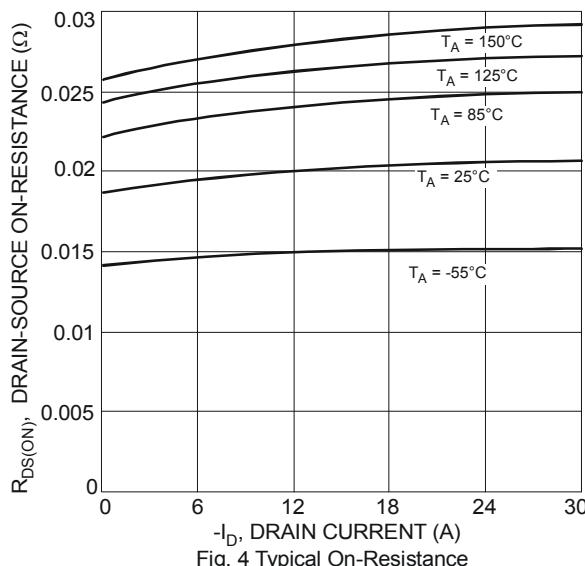
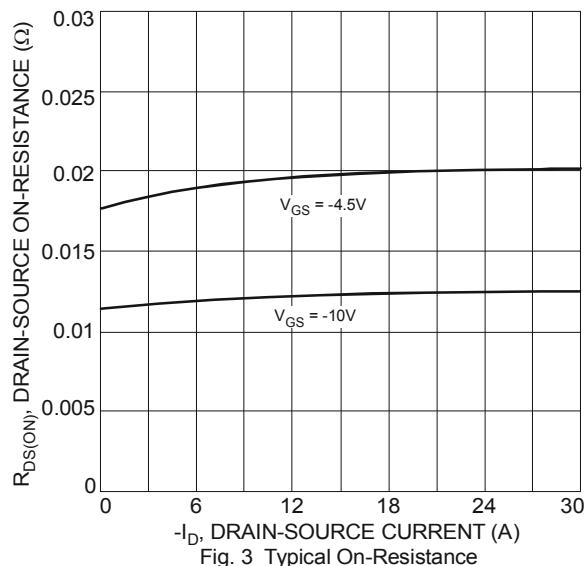


Fig. 2 Typical Transfer Characteristic



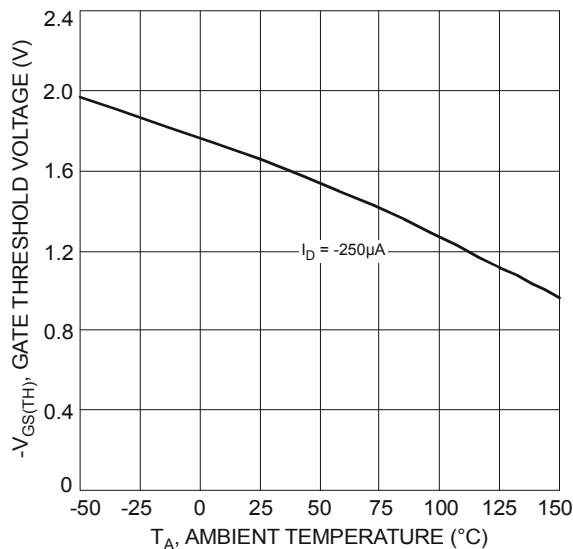


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

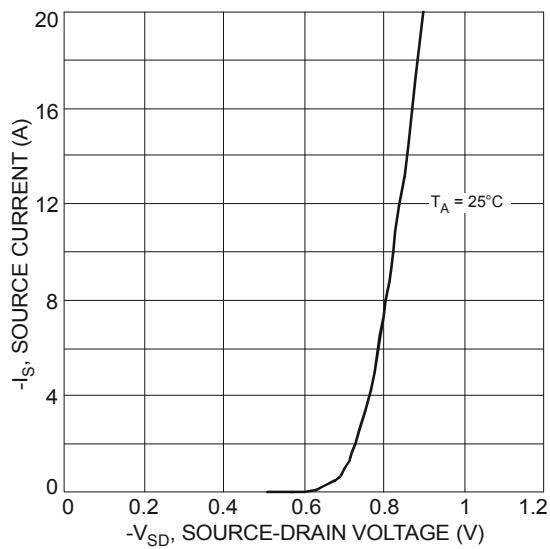


Fig. 8 Diode Forward Voltage vs. Current

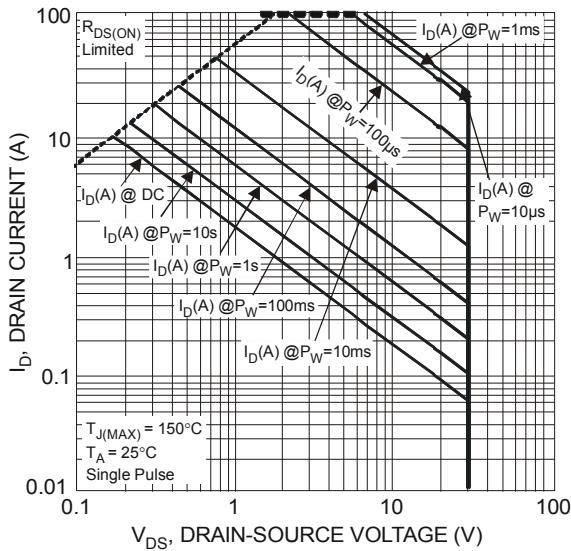


Fig. 9 SOA, Safe Operation Area

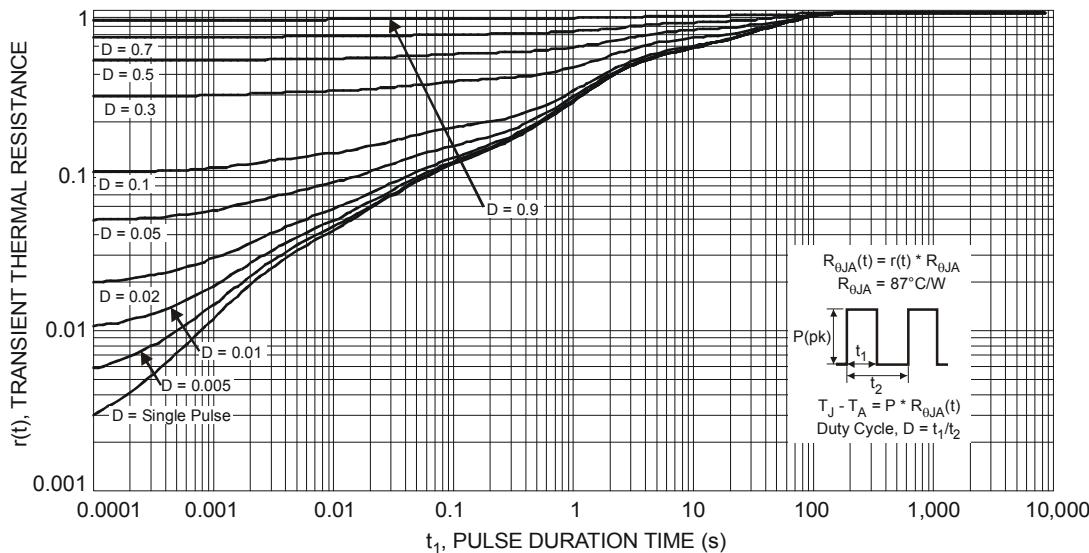
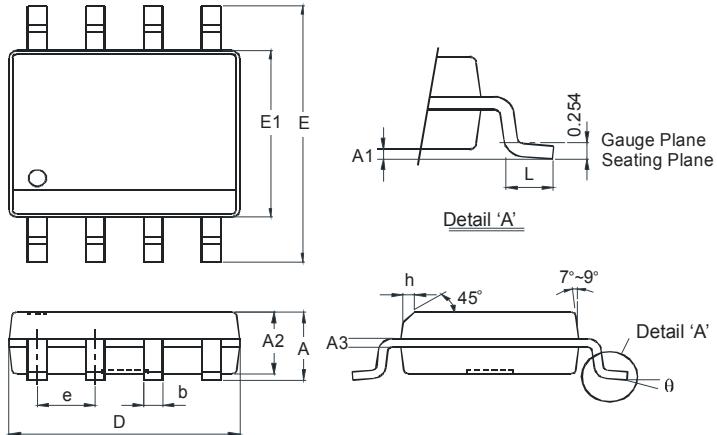


Fig. 10 Transient Thermal Response

Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

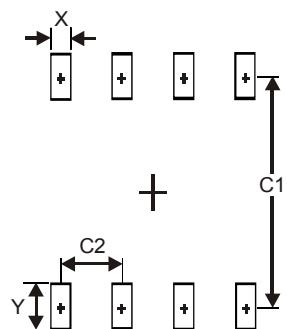


SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°

All Dimensions in mm

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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