



Mobile SDR

H5TC1G43TFR

The H5TC1G43TFR-xxA and H5TC1G83TFR-xxA are a 1Gb low power Double Data Rate III (DDR3L) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density, high bandwidth and low power operation at 1.35V. Hynix DDR3L SDRAM provides backward compatibility with the 1.5V DDR3 based environment without any changes. (Please refer to the SPD information for details.)

Hynix 1Gb DDR3L SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock (falling edges of the clock), data, data strobes and write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Ordering Information

* xx means Speed Bin Grade

Part No.		Configuration							Package
H5TC1G43TFR-xxA		256M x 4							78ball FBGA
H5TC1G83TFR-xxA		128 x 8							
Operating Frequency									
Speed Grade	Frequency [MHz]							Remark	
(Marking)	CL5	CL6	CL7	CL8	CL9	CL10	CL11	(CL-tRCD-tRP)	
-G7		O	O	O				DDR3-1066 7-7-7	
-H9		O	O	O	O	O		DDR3-1333 9-9-9	
<Note>Speed									
G7	DDR3-1066 7-7-7				H9		DDR3-1333 9-9-9		

Technical Data Sheet

Part Number	Rev.	Update Date	Remark
H5TC1G43TFR	0.1	2010-01-22	
Simulation Model			
Part Number	Rev.	Update Date	Remark
IBIS	0.1	2010-01-22	
Verilog	1.3	2010-01-22	
HSpice	1.0	2010-01-22	
Device Operation			
File Name		Update Date	Remark
DDR3L_device_operation_timing_diagram.pdf		2010-01-22	