TWO-CELL Li-ION CHARGE MANAGEMENT IC FOR PDAs AND INTERNET APPLIANCES

Check for Samples: bq24004, bq24005, bq24006

FEATURES

- **Highly Integrated Solution With FET Pass Transistor and Reverse-Blocking Schottky and Thermal Protection**
- **Integrated Voltage and Current Regulation With Programmable Charge Current**
- **High-Accuracy Voltage Regulation (±1%)**
- **Ideal for Low-Dropout Linear Charger Designs for Two-Cell Li-Ion Packs With Coke or Graphite Anodes**
- **Up to 1.2-A Continuous Charge Current**
- **Safety-Charge Timer During Preconditioning and Fast Charge**
- **Integrated Cell Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage of Charge**
- **Optional Temperature or Input-Power Monitoring Before and During Charge**
- **Various Charge-Status Output Options for Driving Single, Double, or Bicolor LEDs or Host-Processor Interface**
- **Charge Termination by Minimum Current and Time**
- **Low-Power Sleep Mode**
- **Packaging: 20-Lead TSSOP PowerPAD™**

APPLICATIONS

- **PDAs**
- **Internet Appliances**
- **MP3 Players**
- **Digital Cameras**

DESCRIPTION

The bq2400x series ICs are advanced Li-Ion linear charge management devices for highly integrated and space-limited applications. They combine high-accuracy current and voltage regulation; FET pass-transistor and reverse-blocking Schottky; battery conditioning, temperature, or input-power monitoring; charge termination; charge-status indication; and charge timer in a small package.

The bq2400x measures battery temperature using an external thermistor. For safety, the bq2400x inhibits charge until the battery temperature is within the user-defined thresholds. Alternatively, the user can monitor the input voltage to qualify charge. The bq2400x series then charge the battery in three phases: preconditioning, constant current, and constant voltage. If the battery voltage is below the internal low-voltage threshold, the bq2400x uses low-current precharge to condition the battery. A preconditioning timer provides additional safety. Following pre- conditioning, the bq2400x applies a constant-charge current to the battery. An external sense-resistor sets the magnitude of the current. The constant-current phase is maintained until the battery reaches the charge-regulation voltage. The bq2400x then transitions to the constant voltage phase. The user can configure the device for cells with either coke or graphite anodes. The accuracy of the voltage regulation is better than ±1% over the operating junction temperature and supply voltage range.

Charge is terminated by maximum time or minimum taper current detection

The bq2400x automatically restarts the charge if the battery voltage falls below an internal recharge threshold.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGE	CHARGE STATUS CONFIGURATION
	20-LEAD HTTSOP PowerPAD™ (PWP)(1) (2)	
–40°C to 125°C	bq24004PWP	Single LED
	bq24005PWP	2 LEDs
	bq24006PWP	Single bicolor LED

(1) The PWP package is available taped and reeled. Add R suffix to device type (e.g., bq24005PWPR) to order. Quantities 2500 devices per reel.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JA}	Θ_{JC}	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$
PWP(1)	30.88°C/W	1.19°C/W	3.238 W	0.0324 W/°C

(1) This data is based on using the JEDEC high-K board and topside traces, top and bottom thermal pad (6,5 × 3,4 mm), internal 1-oz. power and ground planes, 8 thermal via underneath the die connecting to ground plane.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		bq24004 bq24005 bq24006
	Supply voltage (V_{CC} with respect to GND)	13.5 V
	Input voltage (IN, ISNS, EN, APG/THERM/CR/STAT1/STAT2, VSENSE, TMR SEL, VSEL) (all with respect to GND)	13.5 V
	Output current (OUT pins)	2 A
	Output sink/source current (STAT1 and STAT2)	10 mA
T_A	Operating free-air temperature range	–40°C to 70°C
T_{stg}	Storage temperature range	–65°C to 150°C
T_J	Junction temperature range	–40°C to 125°C
	Lead temperature (Soldering, 10 s)	300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	8.4	10	V
V_{IN}	Input voltage	8.4	10	V
	Continuous output current		1.2	A
T_J	Operating junction temperature range	–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature supply and input voltages, and V_I (V_{CC}) ≥ V_I (IN) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} current	V_{CC} > V_{CC_UVLO}, EN ≤ $V_{(IHEN)}$			1	mA
V_{CC} current, standby mode	EN ≤ $V_{(ILEN)}$		1		µA
IN current, standby mode	EN ≤ $V_{(ILEN)}$			10	µA
Standby current (sum of currents into OUT and VSENSE pins)	V_{CC} < V_{CC_UVLO}, $V_{O(OUT)}$ = 8.6 V, VSENSE = 8.6 V		2	8	µA
	EN ≤ $V_{(ILEN)}$, $V_{O(OUT)}$ = 8.6 V, VSENSE = 8.6 V		2	8	
VOLTAGE REGULATION, 0°C ≤ T_J ≤ 125°C					
Output voltage	VSEL = V_{SS}, 0 < I_O ≤ 1.2 A	8.118	8.20	8.282	V
	VSEL = V_{CC}, 0 < I_O ≤ 1.2 A	8.316	8.40	8.484	
Load regulation	1 mA ≤ I_O≤ 1.2 A,V_{CC} = 10 V, $V_{I(IN)}$= 5 V,T_J = 25°C		1		mV
Line regulation	$V_{O(OUT)}$ + V_{DO} + $V_{(ilim)}$MAX < $V_{I(VCC)}$ < 10 V, T_J = 25°C		0.01		%/V
Dropout voltage = VI(IN)-Vout	I_O = 1.2 A, $V_{O(OUT)}$ + $V_{(DO)}$ + $V_{(ilim)}$MAX < $V_{I(VCC)}$ < 10 V			0.5	V
CURRENT REGULATION, 0°C ≤ T_J ≤ 125°C					
Current regulation threshold, $V_{I(limit)}$	VSENSE < $V_{O(VSEL-LOW/HIGH)}$	0.093	0.1	0.107	V
Delay time	VSENSE pulsed above $V_{(LOWV)}$ to I_O = 10% of regulated value(1)			1	ms
Rise time	I_O increasing from 10% to 90% of regulated value, $R_{(SNS)}$ ≥ 0.2 Ω(1)	0.1		1	ms
CURRENT SENSE RESISTOR, 0°C ≤ T_J ≤ 125°C					
External current sense resistor range $R_{(SNS)}$	100 mA ≤ (ilim) ≤ 1.2 A	0.083		1	Ω
PRECHARGE CURRENT REGULATION, 0°C ≤ T_J ≤ 125°C					
Precharge current regulation	VSENSE<$V_{(LOWV)}$, 0.083 ≤ $R_{(SNS)}$≤ 1.0 Ω	40	60	80	mA
V_{CC} UVLO COMPARATOR, 0°C ≤ T_J ≤ 125°C					
Start threshold		8.75	8.9	9.0	V
Stop threshold		8.50	8.66	8.8	V
Hysteresis		50			mV
APG/THERM COMPARATOR, 0°C ≤ T_J ≤ 125°C					
Upper trip threshold		1.480	1.498	1.515	V
Lower trip threshold		0.545	0.558	0.570	V
Input bias current				1	µA
LOWV COMPARATOR, 0°C ≤ T_J ≤ 125°C					
Start threshold		5.60	5.75	5.90	V
Stop threshold		6.10	6.25	6.40	V
Hysteresis		100			mV
HIGHV (RECHARGE) COMPARATOR, 0°C ≤ T_J ≤ 125°C					
Start threshold		7.70	7.85	8.00	V
OVERV COMPARATOR, 0°C ≤ T_J ≤ 125°C					
Start threshold		8.85	9.00	9.15	V
Stop threshold		8.45	8.60	8.75	V
Hysteresis		50			mV
TAPERDET COMPARATOR, 0°C ≤ T_J ≤ 125°C					
Trip threshold		12	18.5	25	mV
EN LOGIC INPUT, 0°C ≤ T_J ≤ 125°C					
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	kΩ

(1) Specified by design, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

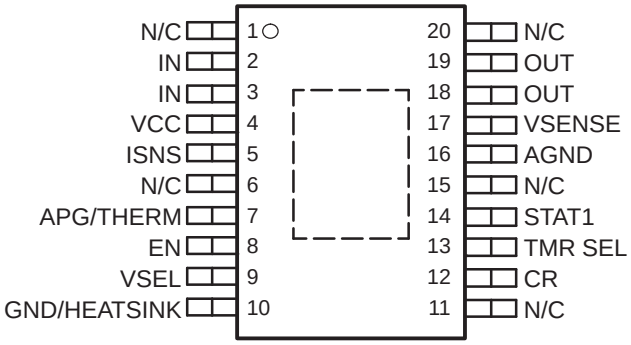
over recommended operating junction temperature supply and input voltages, and V_I (V_{CC}) ≥ V_I (IN) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSEL LOGIC INPUT, 0°C ≤ T_J ≤ 125°C					
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	kΩ
TMR SEL INPUT 0°C ≤ T_J ≤ 125°C					
High-level input voltage		2.7			V
Low-level input voltage				0.6	V
Input bias current	$V_{I(TMR\ SEL)}$ ≤ 5 V			15	µA
STAT1, STAT2 (bq24004, bq24006), 0°C ≤ T_J ≤ 125°C					
Output (low) saturation voltage	I_O = 10 mA			1.5	V
	I_O = 4 mA			0.6	
Output (high) saturation voltage	I_O = –10 mA	V_{CC}–1.5			V
	I_O = –4 mA	V_{CC}–0.5			
Output turn on/off time	I_O = ± 10 mA, C = 100 pF (2)			100	µs
POWER-ON RESET (POR), 0°C ≤ T_J ≤ 125°C					
POR delay	See (2)	1.2		3	ms
POR falling-edge deglitch	See (2)	25		75	µs
APG/THERM DELAY, 0°C ≤ T_J ≤ 125°C					
APG/THERM falling-edge deglitch	See (2)	25		75	µs
TIMERS, 0°C ≤ T_J ≤ 125°C					
User-selectable timer accuracy	T_A = 25°C	15%		15%	
		20%		20%	
Precharge and taper timer			22.5		minute
THERMAL SHUTDOWN, 0°C ≤ T_J ≤ 125°C					
Thermal trip	See (2)		165		°C
Thermal hysteresis	See (2)		10		°C
CR PIN, 0°C ≤ T_J ≤ 125°C					
Output voltage	0 < $I_{O(CR)}$ < 100 µA	2.816	2.85	2.88	V

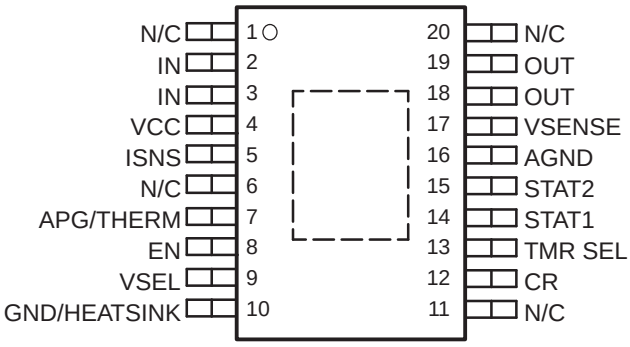
(2) Specified by design, not production tested.

PIN ASSIGNMENTS

bq24004
PWP PACKAGE
(TOP VIEW)



bq24005, bq24006
PWP PACKAGE
(TOP VIEW)

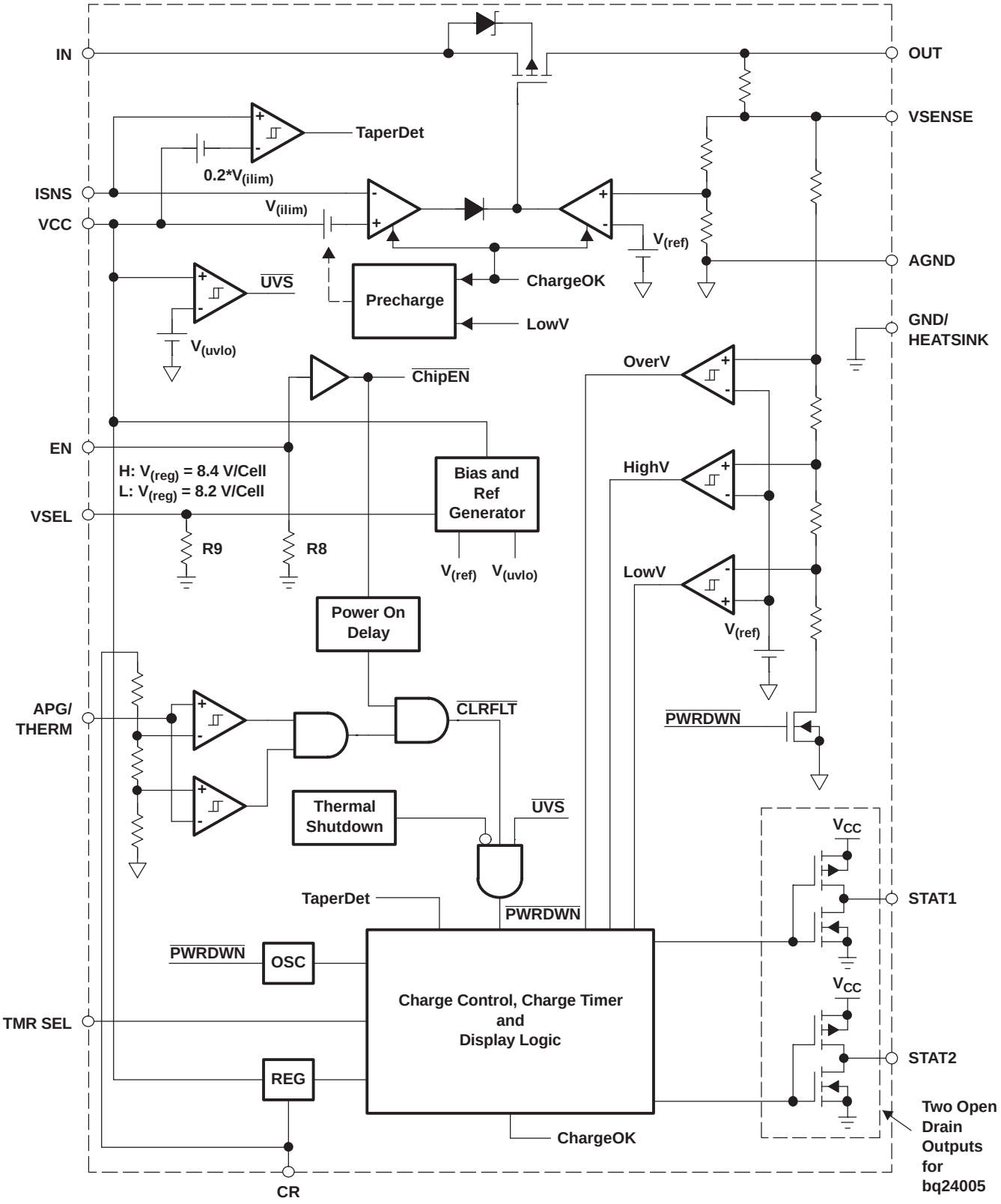


N/C - Do not connect

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	16		Ground pin; connect close to the negative battery terminal.
APG/THERM	7	I	Adapter power good input/thermistor sense input
CR	12	I	Internal regulator bypass capacitor
EN	8	I	Charge-enable input. Active-high enable input with internal pull down. Low-current stand-by mode active when EN is low.
GND/HEATSINK	10		Ground pin; connect to PowerPAD heat-sink layout pattern.
IN	2, 3	I	Input voltage. This input provides the charging voltage for the battery.
ISNS	5	I	Current sense input
N/C	1, 6, 11, 15, 20		No connect. These pins must be left floating. Pin 15 is N/C on bq24004PWP only.
OUT	18, 19	O	Charge current output
STAT1	14	O	Status display output 1
STAT2	15	O	Status display output 2 (for bq24005 and bq24006 only)
TMR SEL	13	I	Charge timer selection input
VCC	4	I	Supply voltage
VSEL	9	I	8.2-V or 8.4-V charge regulation selection input
VSENSE	17	I	Battery voltage sense input

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT CURRENT

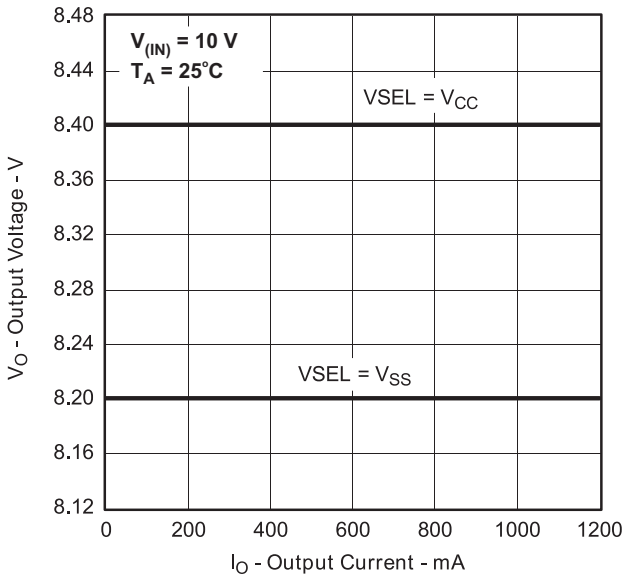


Figure 1.

OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

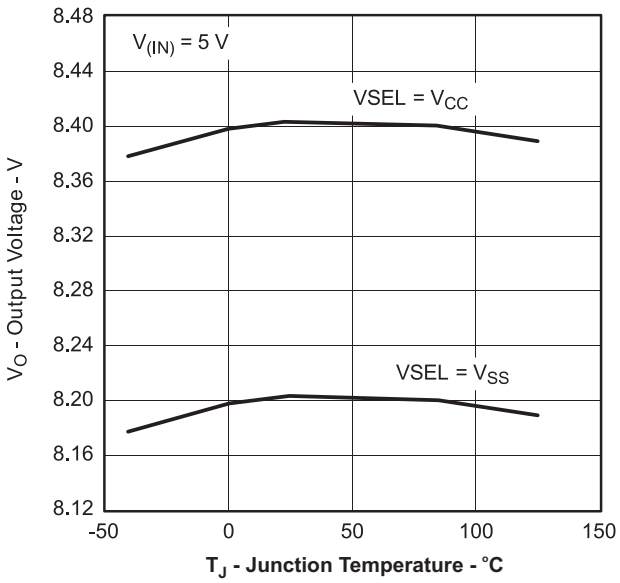


Figure 2.

OUTPUT VOLTAGE vs INPUT VOLTAGE

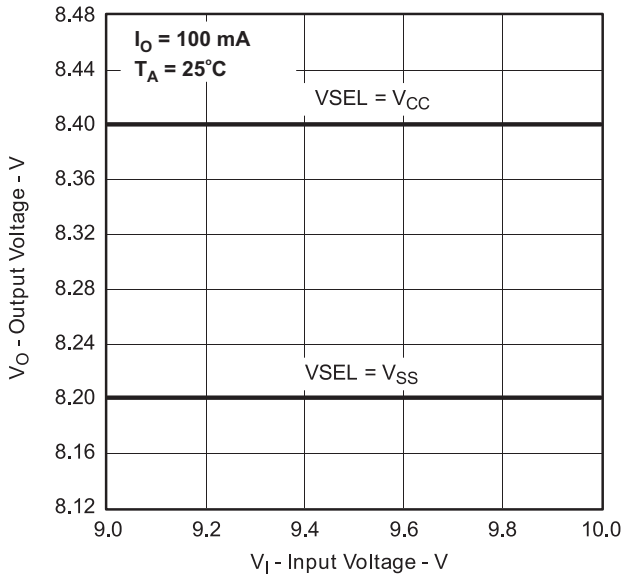


Figure 3.

CURRENT SENSE VOLTAGE vs INPUT VOLTAGE

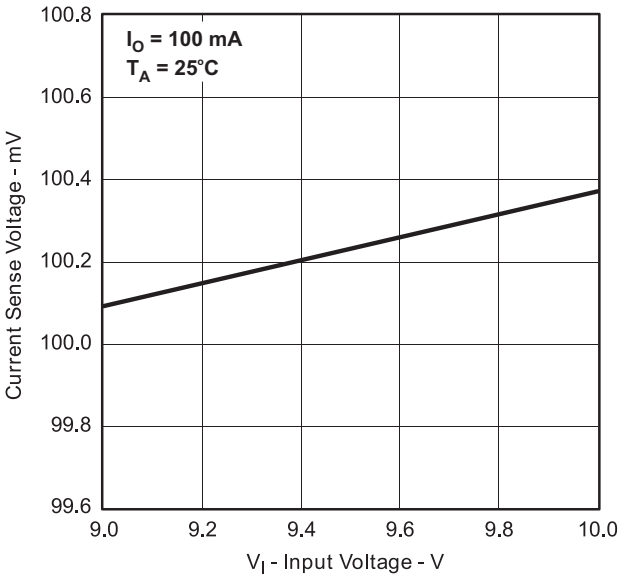


Figure 4.

TYPICAL CHARACTERISTICS (continued)

CURRENT SENSE VOLTAGE vs JUNCTION TEMPERATURE

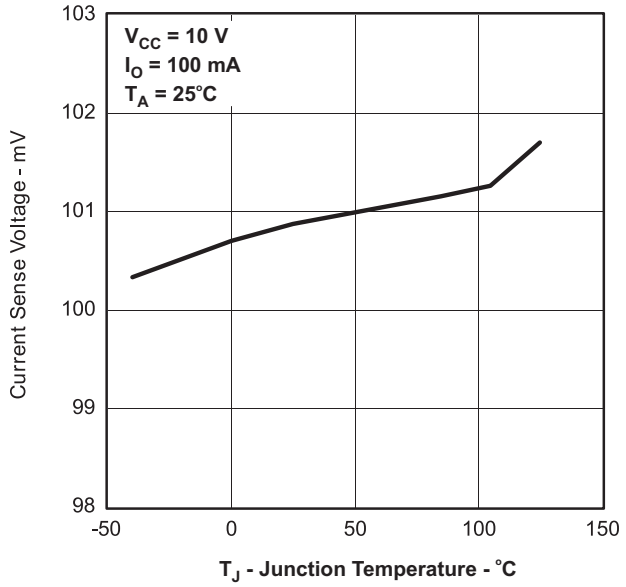


Figure 5.

QUIESCENT CURRENT vs INPUT VOLTAGE

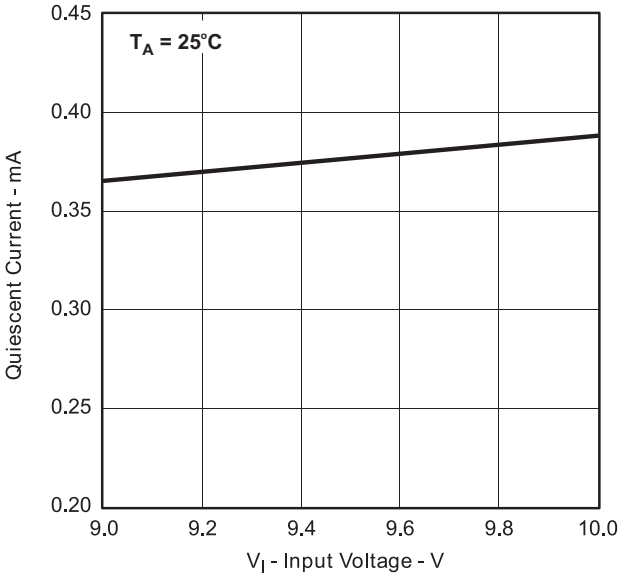


Figure 6.

QUIESCENT CURRENT (POWER DOWN) vs INPUT VOLTAGE

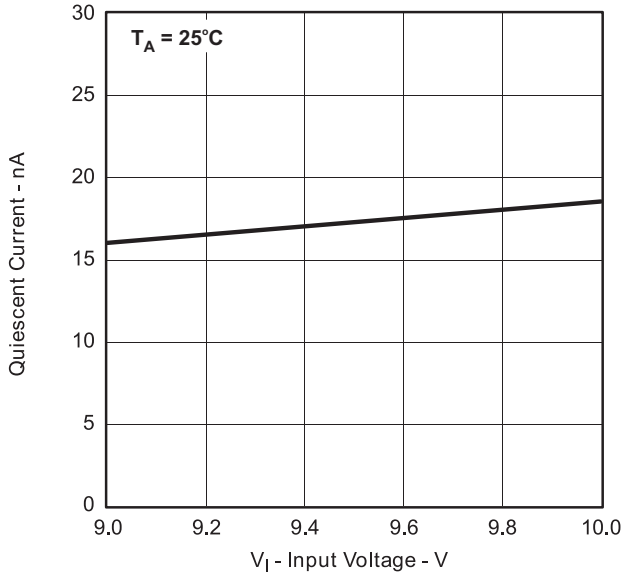


Figure 7.

DROPOUT VOLTAGE vs INPUT VOLTAGE

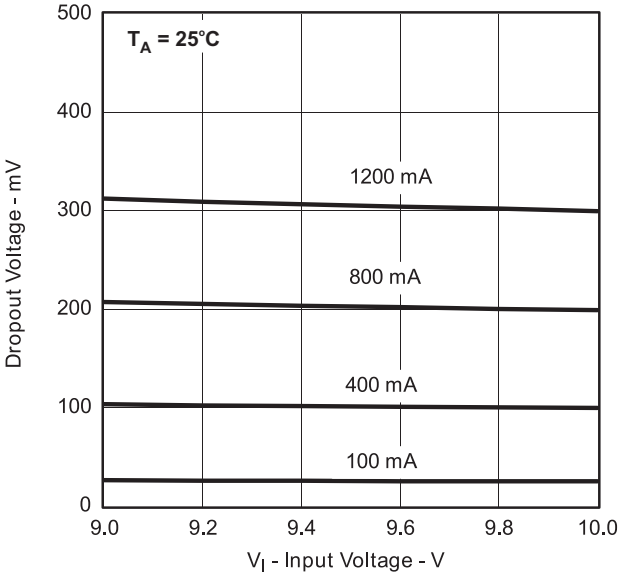


Figure 8.

TYPICAL CHARACTERISTICS (continued)

DROPOUT VOLTAGE vs OUTPUT CURRENT

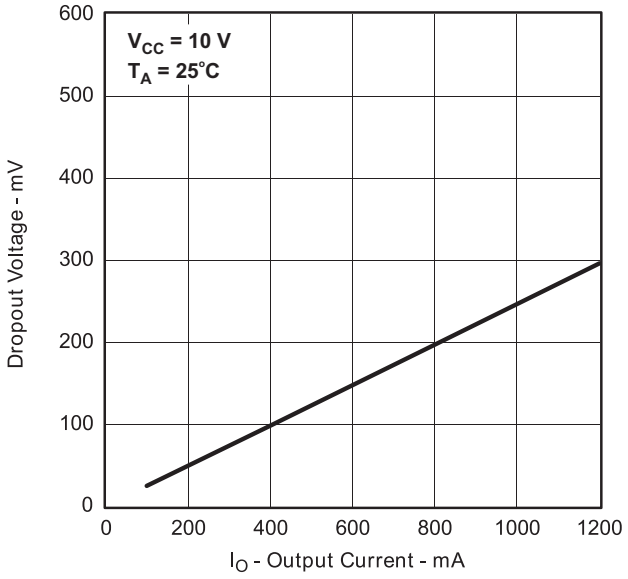


Figure 9.

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

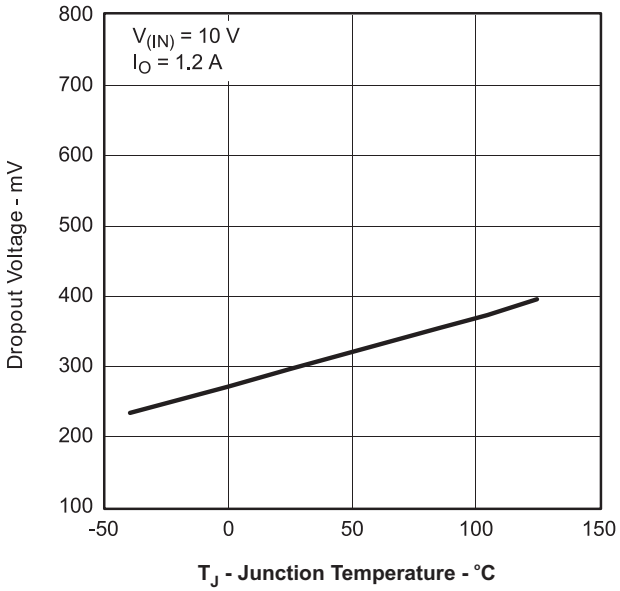


Figure 10.

REVERSE CURRENT vs JUNCTION TEMPERATURE

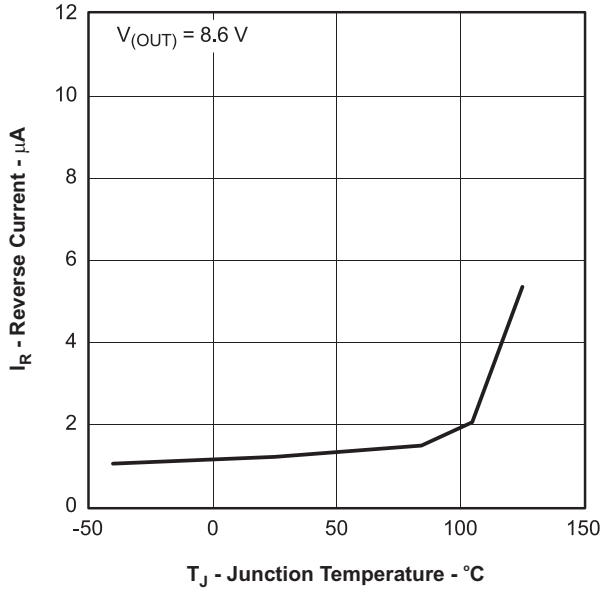


Figure 11.

REVERSE CURRENT LEAKAGE vs VOLTAGE ON OUT PIN

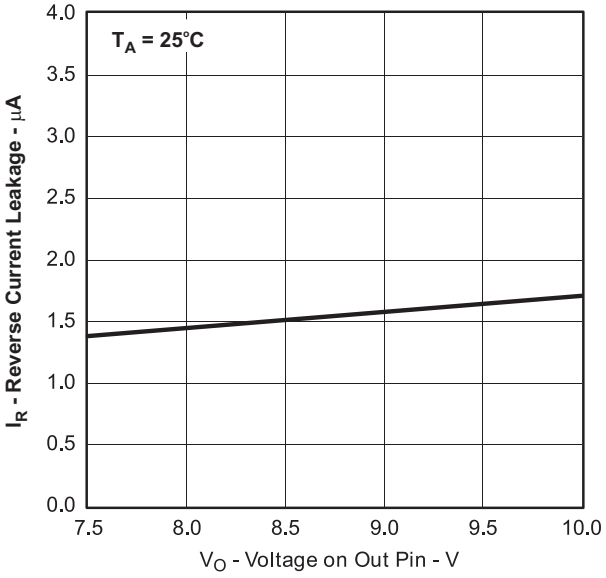


Figure 12.

APPLICATION INFORMATION

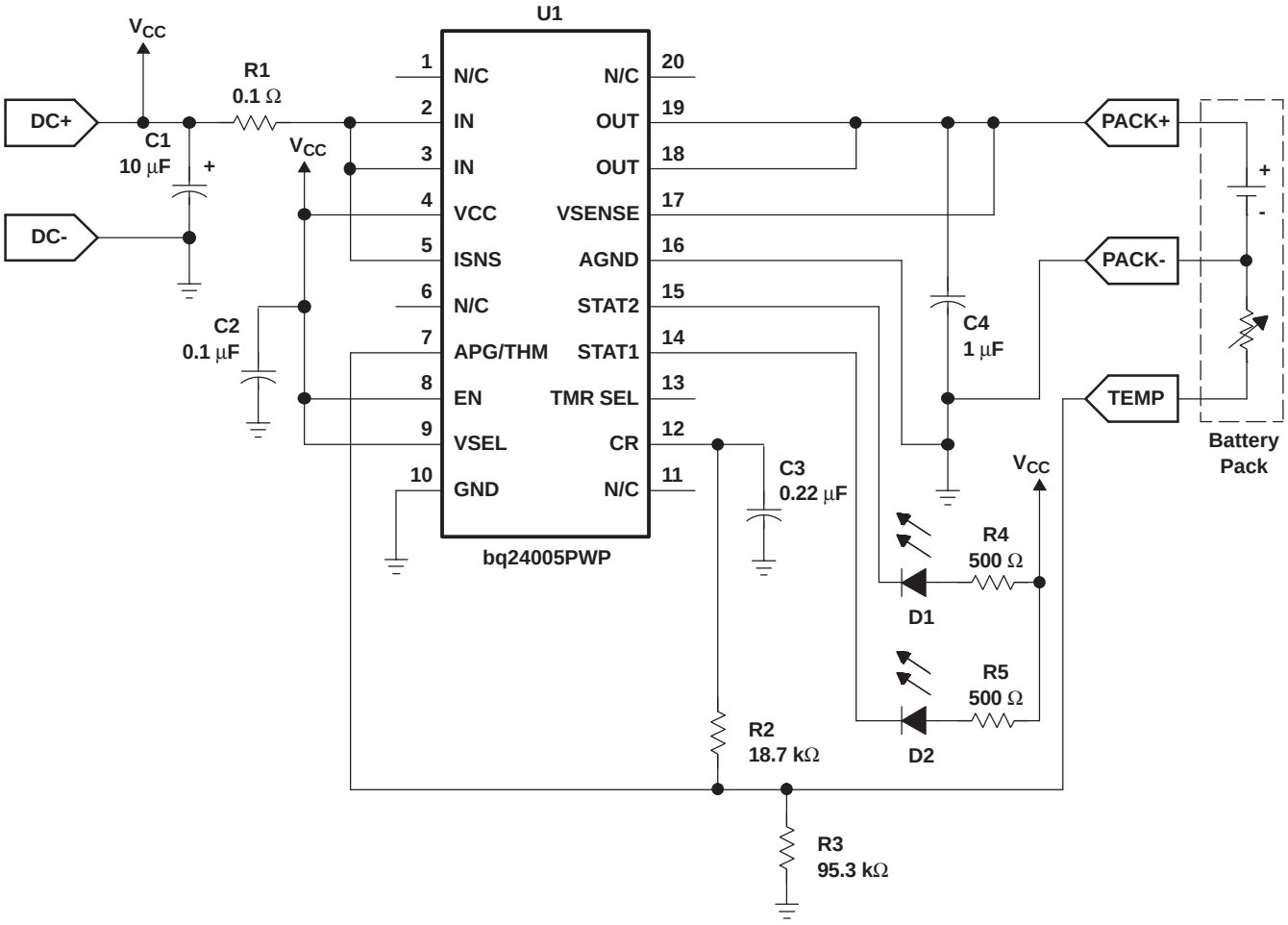


Figure 13. Li-ION/Li-POL Charger

- If the TMR SEL pin is left floating (3 HR time), a 10-pF capacitor should be installed between TMR SEL and CR.
- If a micro process is monitoring the STAT pins, it may be necessary to add some hysteresis into the feedback to prevent the STAT pins from cycling while crossing the taper detect threshold (usually less than one half second). See SLUU083 EVM or SLUU113 EVM for additional resistors used for the STAT pins.

FUNCTIONAL DESCRIPTION

The bq2400x supports a precision current- and voltage-regulated Li-Ion charging system suitable for cells with either coke or graphite anodes. See Figure 14 for a typical charge profile and Figure 15 for an operational flowchart.

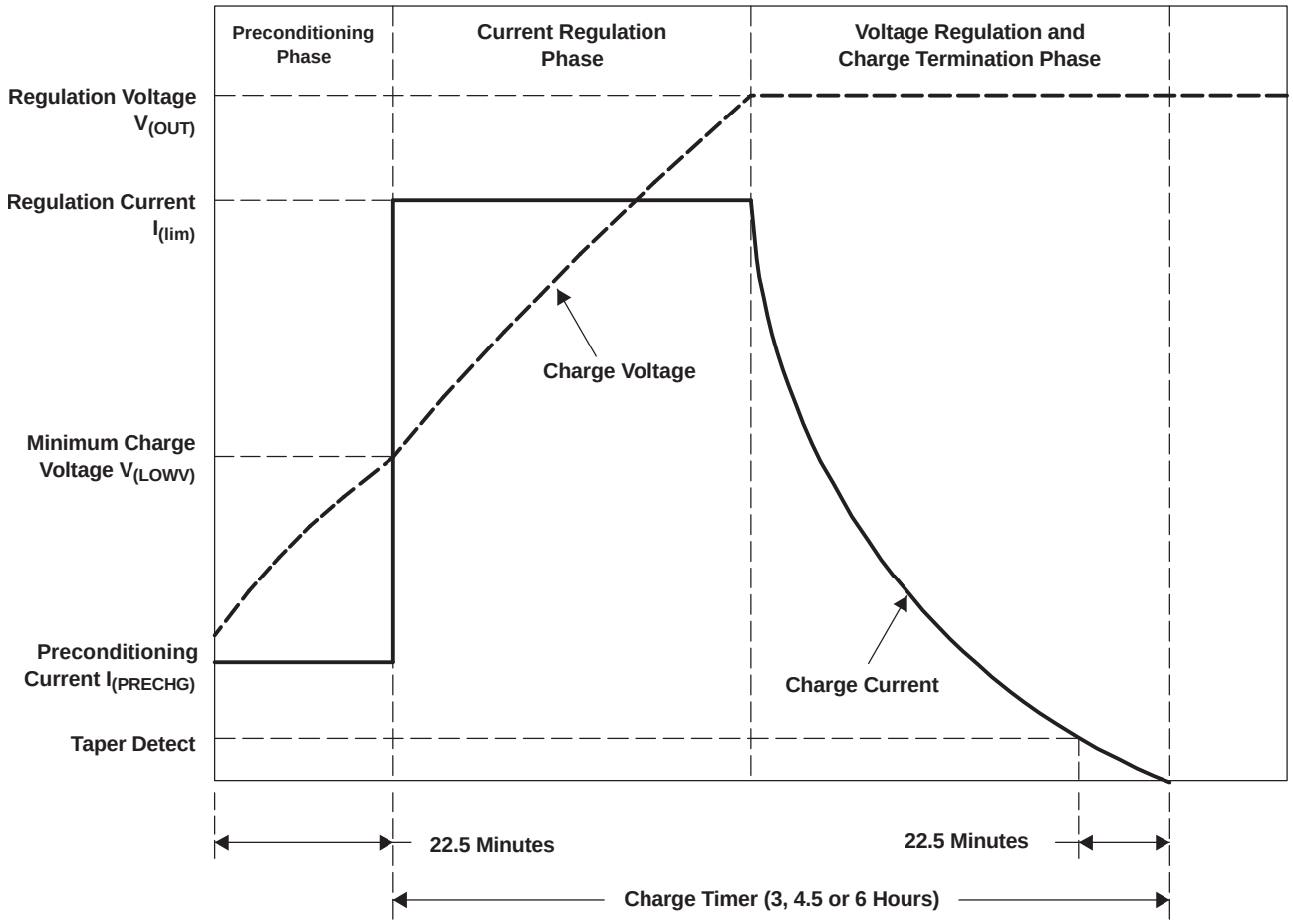


Figure 14. Typical Charge Profile

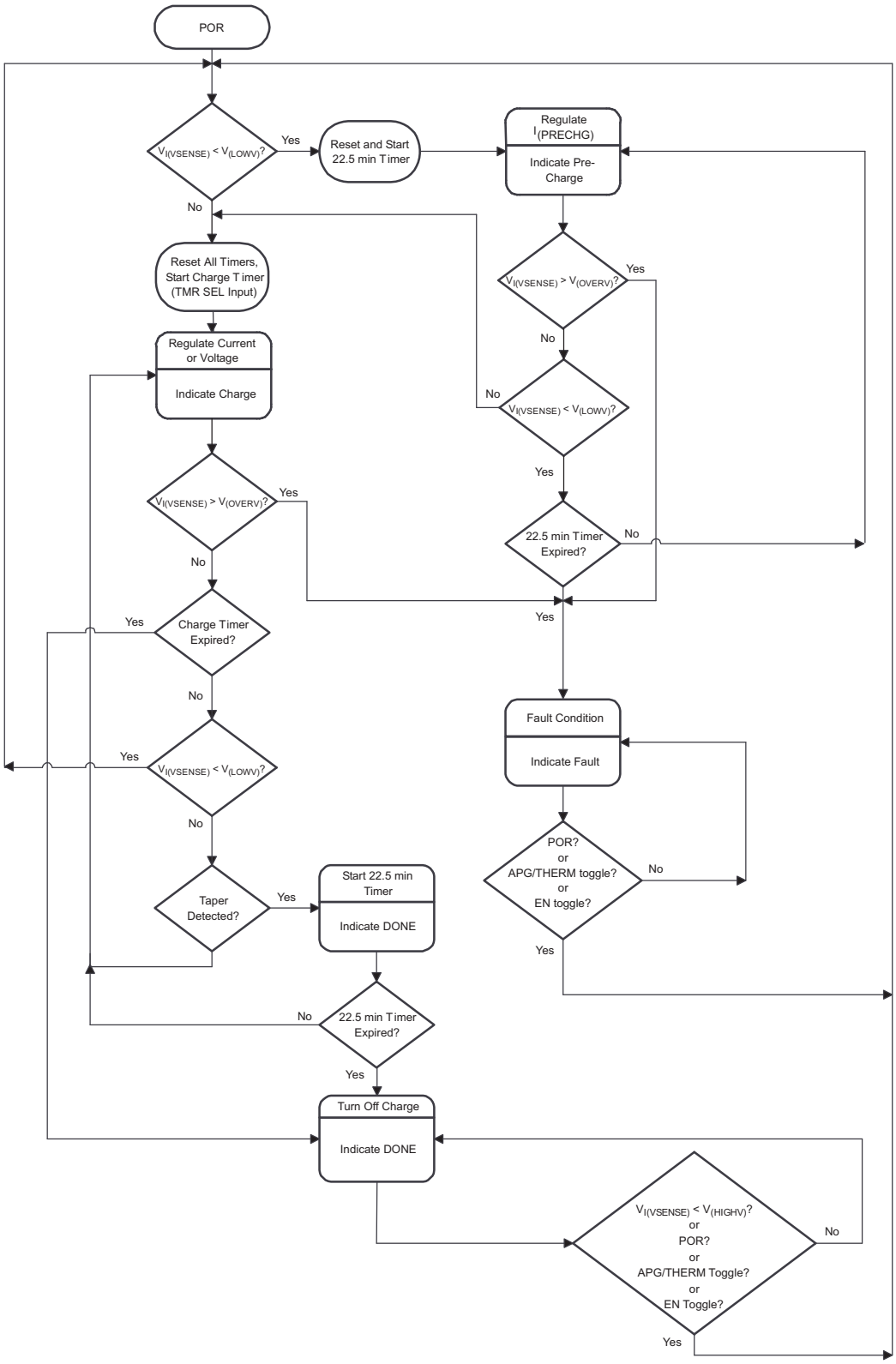


Figure 15. Operational Flow Chart

Charge Qualification and Preconditioning

The bq2400x starts a charge cycle when power is applied while a battery is present. Charge qualification is based on battery voltage and the APG/THERM input.

As shown in the block diagram, the internal LowV comparator output prevents fast-charging a deeply depleted battery. When set, charging current is provided by a dedicated precharge current source. The precharge timer limits the precharge duration. The precharge current also minimizes heat dissipation in the pass element during the initial stage of charge.

The APG/THERM input can also be configured to monitor either the adapter power or the battery temperature using a thermistor. The bq2400x suspends charge if this input is outside the limits set by the user. Refer to the APG/THERM input section for additional details.

APG/THERM Input

The bq2400x continuously monitors temperature or system input voltage by measuring the voltage between the APG/THERM (adapter power good/thermistor) and GND. For temperature, a negative- or a positive-temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage (see Figure 16). The bq2400x compares this voltage against its internal $V_{(TP1)}$ and $V_{(TP2)}$ thresholds to determine if charging is allowed. (See Figure 17.)

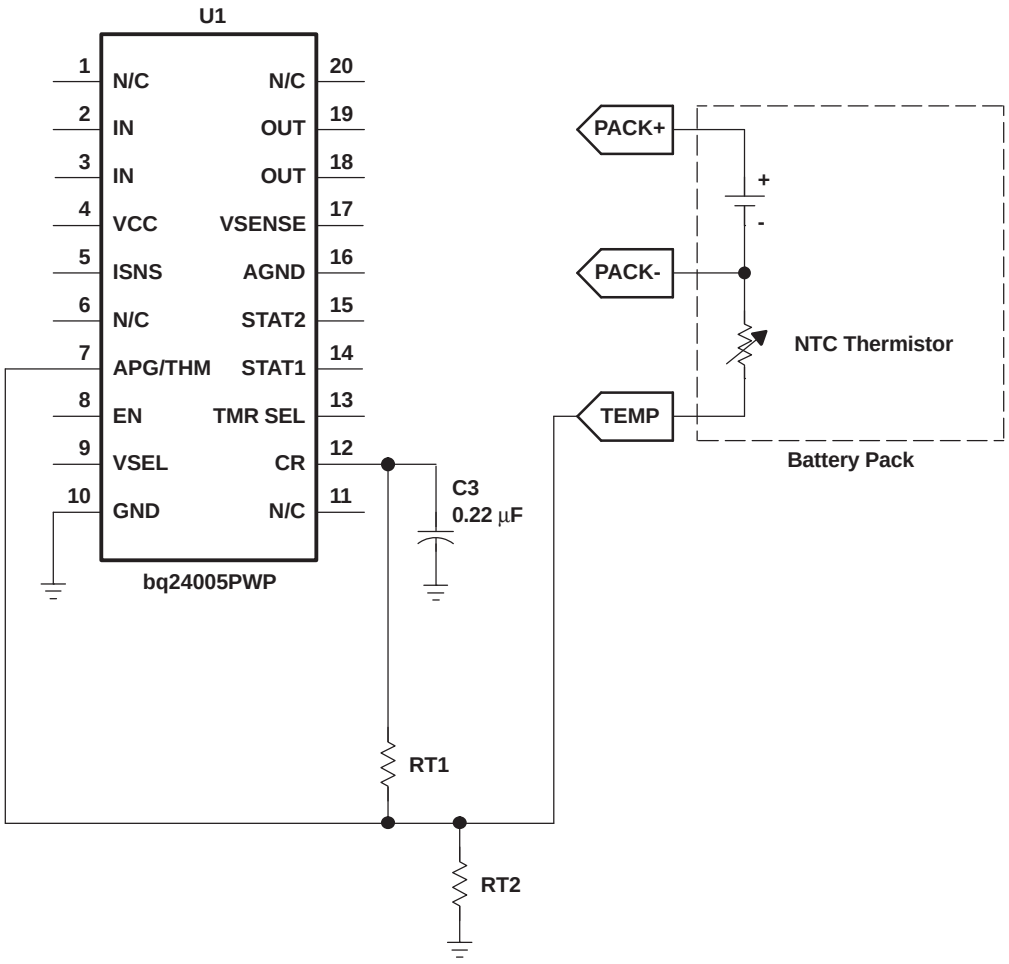


Figure 16. Temperature Sensing Circuit

If the charger designs incorporate a thermistor, the resistor divider RT1 and RT2 is calculated by using the following two equations.

First, calculate RT2.

$$RT2 = \frac{V_B R_H R_C \left[\frac{1}{V_C} - \frac{1}{V_H}\right]}{R_H \left(\frac{V_B}{V_H} - 1\right) - R_C \left(\frac{V_B}{V_C} - 1\right)}$$

then use the resistor value to find RT1.

$$RT1 = \frac{\frac{V_B}{V_C} - 1}{\frac{1}{RT2} + \frac{1}{R_C}}$$

Where:

$V_B = V_{CR}$ (bias voltage)

R_H = Resistance of the thermistor at the desired hot trip threshold

R_C = Resistance of the thermistor at the desired cold trip threshold

V_H = VP2 or the lower APG trip threshold

V_C = VP2 or the upper APG trip threshold

RT1 = Top resistor in the divider string

RT2 = Bottom resistor in the divider string

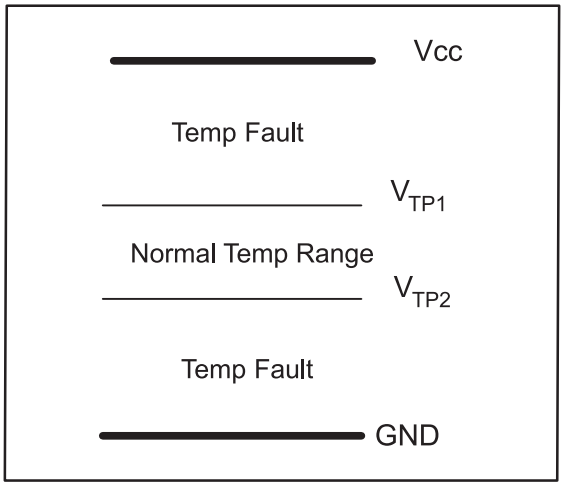


Figure 17. Temperature Threshold

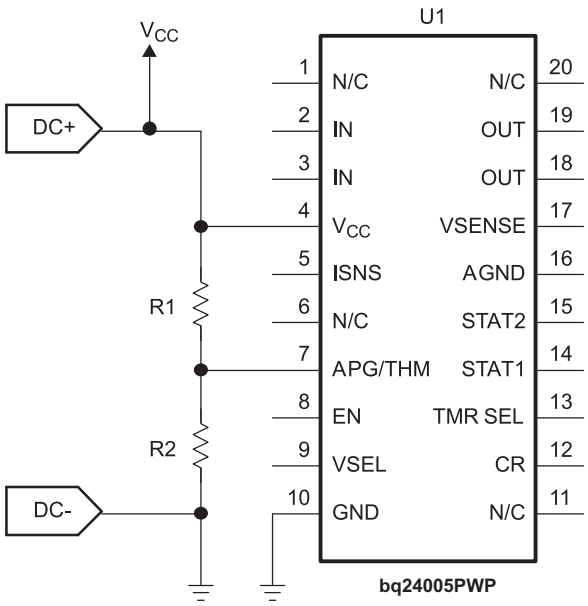


Figure 18. APG Sensing Circuit

Values of resistors R1 and R2 can be calculated using the following equation:

$$V_{(APG)} = V_{CC} \frac{R2}{(R1 + R2)}$$

where $V_{(APG)}$ is the voltage at the APG/THM pin.

Current Regulation

The bq2400x provides current regulation while the battery-pack voltage is less than the regulation voltage. The current regulation loop effectively amplifies the error between a reference signal, Vilim, and the drop across the external sense resistor, R_{SNS}.

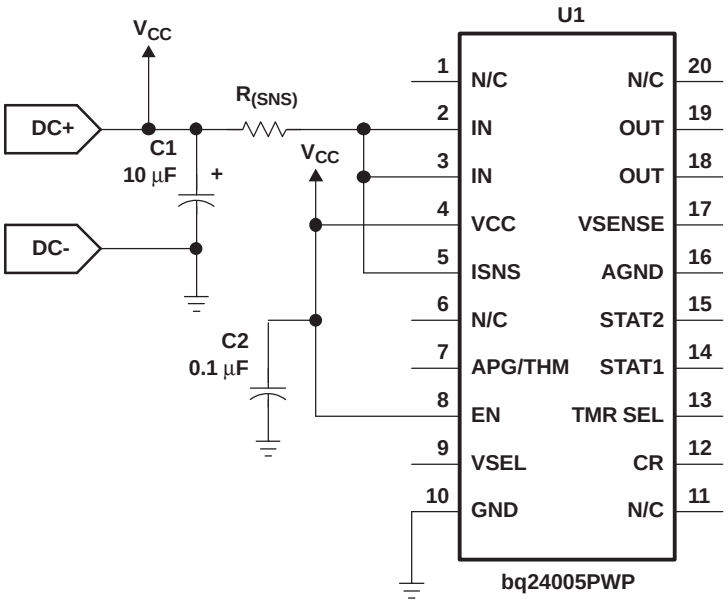


Figure 19. Current Sensing Circuit

Charge current feedback, applied through pin ISNS, maintains regulation around a threshold of Vilim. The following formula calculates the value of the sense resistor:

$$R_{(SNS)} = \frac{V_{(ilim)}}{I_{(REG)}}$$

where $I_{(REG)}$ is the desired charging current.

Voltage Monitoring and Regulation

Voltage regulation feedback is through pin VSENSE. This input is tied directly to the positive side of the battery pack. The bq2400x supports cells with either coke (8.2 V) or graphite (8.4 V) anode. Pin VSEL selects the charge regulation voltage.

VSEL STATE (see Note)	CHARGE REGULATION VOLTAGE
Low	8.2 V
High	8.4 V
NOTE: VSEL should not be left floating.	

Charge Termination

The bq2400x continues with the charge cycle until termination by one of the two possible termination conditions:

Maximum Charge Time: The bq2400x sets the maximum charge time through pin TMRSEL. The TMR SEL pin allows the user to select between three different total charge-time timers (3, 4, 5, or 6 hours). The charge timer is initiated after the preconditioning phase of the charge and is reset at the beginning of a new charge cycle. Note that in the case of a fault condition, such as an out-of-range signal on the APG/THERM input or a thermal shutdown, the bq2400x suspends the timer.

TMRSEL STATE	CHARGE TIME
Floating(1)	3 hours
Low	6 hours
High	4.5 hours
(1)To improve noise immunity, it is recommended that a minimum of 10 pF capacitor be tied to Vss on a floating pin.	

Minimum Current: The bq2400x monitors the charging current during the voltage regulation phase. The bq2400x initiates a 22-minute timer once the current falls below the taperdet trip threshold. Fast charge is terminated once the 22-minute timer expires.

Charge Status Display

The three available options allow the user to configure the charge status display for single LED (bq24004), two individual LEDs (bq24005) or a bicolor LED (bq24006). The output stage is totem pole for the bq24004 and bq24006 and open-drain for the bq24005. The following tables summarize the operation of the three options:

Table 1. bq24004 (Single LED)

CHARGE STATE	STAT1
Precharge	ON (LOW)
Fast charge	ON (LOW)
FAULT	Flashing (1 Hz, 50% duty cycle)

Table 1. bq24004 (Single LED) (continued)

CHARGE STATE	STAT1
Done (>90%)	OFF (HIGH)
Sleep-mode	OFF (HIGH)
APG/Therm invalid	OFF (HIGH)
Thermal shutdown	OFF (HIGH)
Battery absent	OFF (HIGH)

Table 2. bq24005 (2 Individual LEDs)

CHARGE STATE	STAT1 (RED)	STAT2 (GREEN)
Precharge	ON (LOW)	OFF
Fast charge	ON (LOW)	OFF
FAULT	Flashing (1 Hz,50% duty cycle)	OFF
Done (>90%)	OFF	ON (LOW)
Sleep-mode	OFF	OFF
APG/Therm invalid	OFF	OFF
Thermal shutdown	OFF	OFF

Table 2. bq24005 (2 Individual LEDs) (continued)

CHARGE STATE	STAT1 (RED)	STAT2 (GREEN)
Battery absent	OFF	OFF(1)

(1) If thermistor is used, then the Green LED is off.

Table 3. bq24006 (Single Bicolor LED)

CHARGE STATE	LED1 (RED)	LED2 (GREEN)	APPARENT COLOR
Precharge	ON (LOW)	OFF (HIGH)	RED
Fast charge	ON (LOW)	OFF (HIGH)	RED
FAULT	ON (LOW)	ON (LOW)	YELLOW
Done (>90%)	OFF (HIGH)	ON (LOW)	GREEN
Sleep-mode	OFF (HIGH)	OFF (HIGH)	OFF
APG/Therminvalid	OFF (HIGH)	OFF (HIGH)	OFF
Thermal shutdown	OFF (HIGH)	OFF (HIGH)	OFF
Battery absent	OFF (HIGH)	OFF (HIGH)(1)	OFF(1)

(1) If thermistor is used, then the Green LED is off.

Thermal Shutdown

The bq2400x monitors the junction temperature T_J of the DIE and suspends charging if T_J exceeds 165°C. Charging resumes when T_J falls below 155°C.

DETAILED DESCRIPTION

POWER FET

The integrated transistor is a P-channel MOSFET. The power FET features a reverse-blocking Schottky diode, which prevents current flow from OUT to IN.

An internal thermal-sense circuit shuts off the power FET when the junction temperature rises to approximately 165°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 10°C, the power FET turns back on. The power FET continues to cycle off and on until the fault is removed.

CURRENT SENSE

The bq2400x regulates current by sensing, on the ISNS pin, the voltage drop developed across an external sense resistor. The sense resistor must be placed between the supply voltage (Vcc) and the input of the IC (IN pins).

VOLTAGE SENSE

To achieve maximum voltage regulation accuracy, the bq2400x uses the feedback on the VSENSE pin. Externally, this pin should be connected as close to the battery cell terminals as possible. For additional safety, a 10-kΩ internal pullup resistor is connected between the VSENSE and OUT pins.

ENABLE (EN)

The logic EN input is used to enable or disable the IC. A high-level signal on this pin enables the bq2400x. A low-level signal disables the IC and places the device in a low-power standby mode.

THERMAL INFORMATION

THERMALLY ENHANCED TSSOP-20

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad (seeFigure 20) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

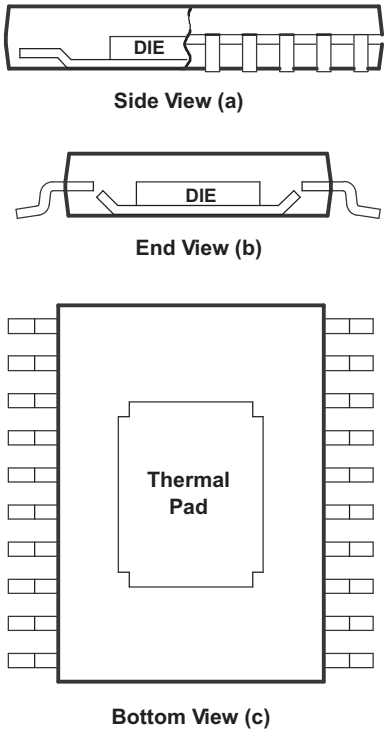


Figure 20. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air. (Reference Figure 22(a),8 cm^2 of copper heat sink and natural convection.) Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly. (See Figure 22(b) and Figure 22(c).) The line drawn at 0.3 cm^2 in Figure 21 and Figure 22 indicates performance at the minimum recommended heat-sink size.

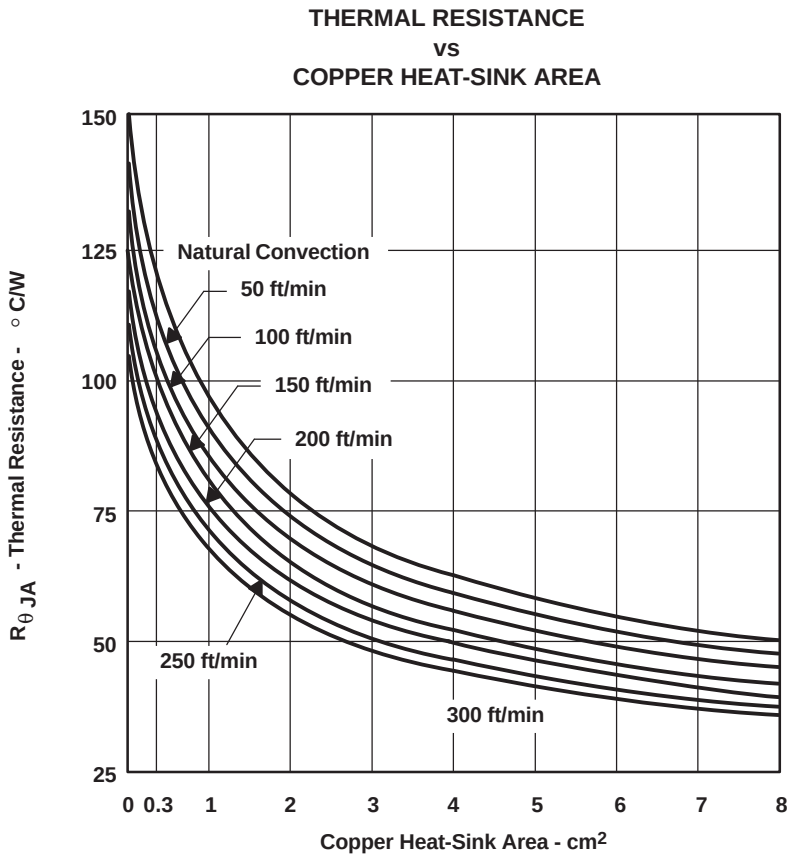


Figure 21.

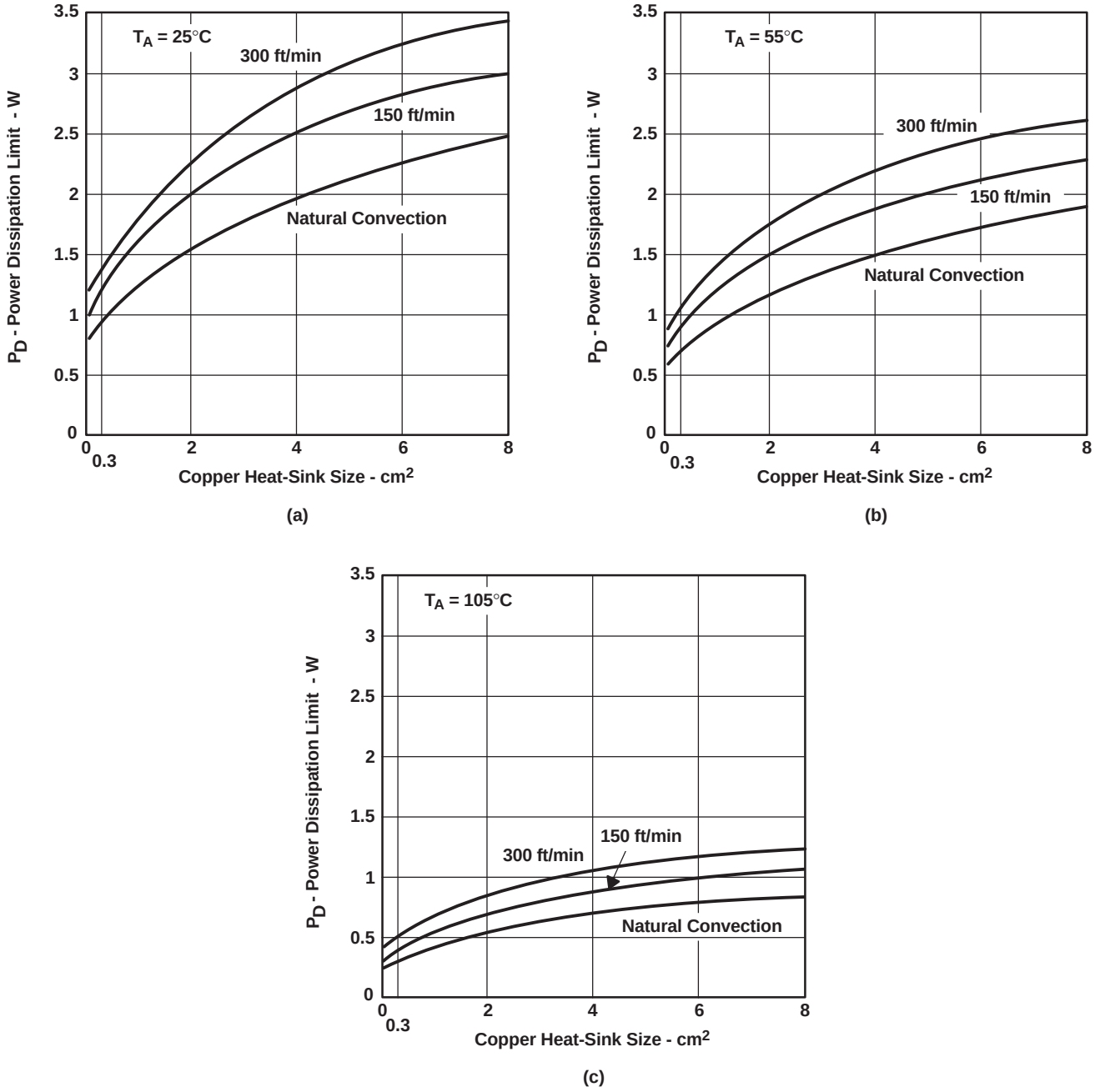


Figure 22. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24004PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	BQ24004
BQ24004PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	BQ24004
BQ24005PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24005
BQ24005PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24005
BQ24005PWPG4	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24005
BQ24005PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24005
BQ24005PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-20 to 70	BQ24005
BQ24006PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	BQ24006
BQ24006PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	BQ24006
BQ24006PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	BQ24006
BQ24006PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	BQ24006

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

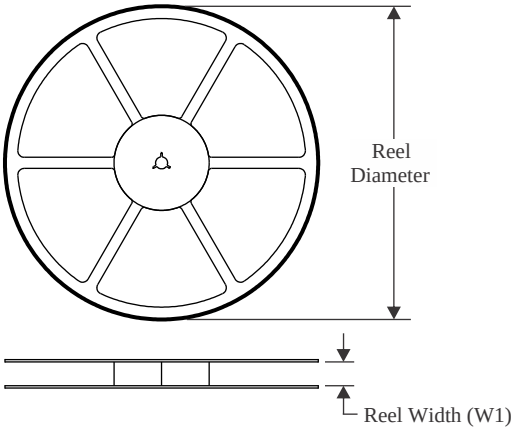
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

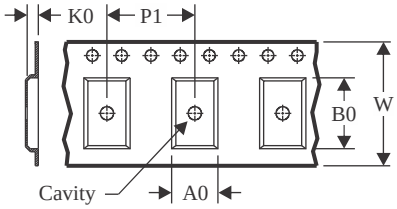
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

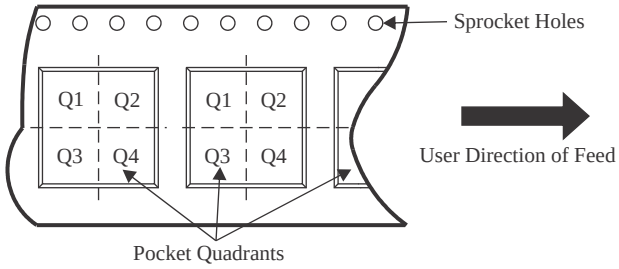


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

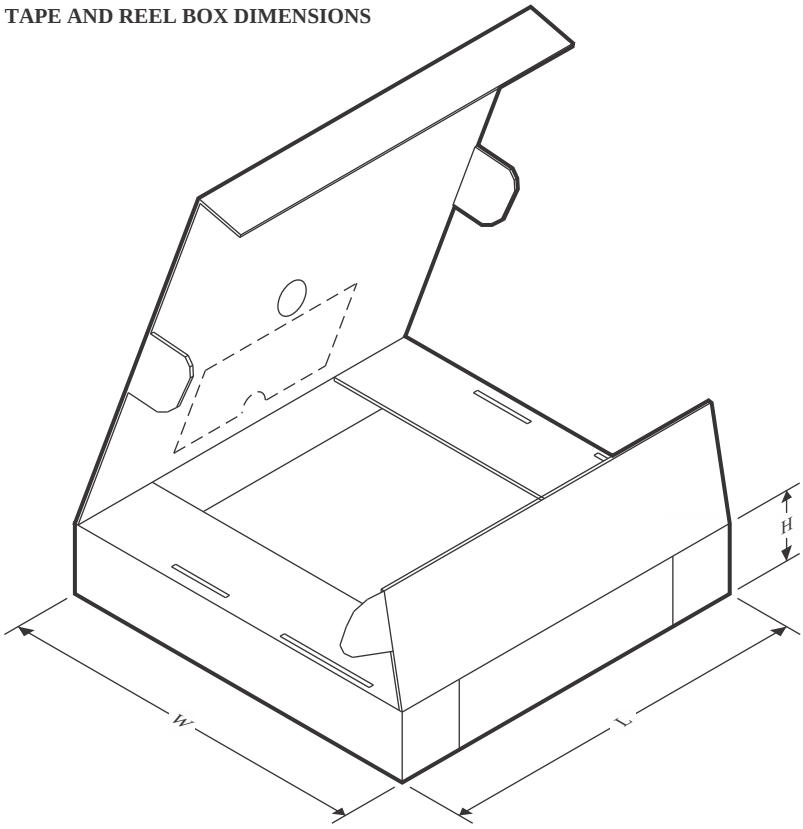
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24005PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
BQ24006PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

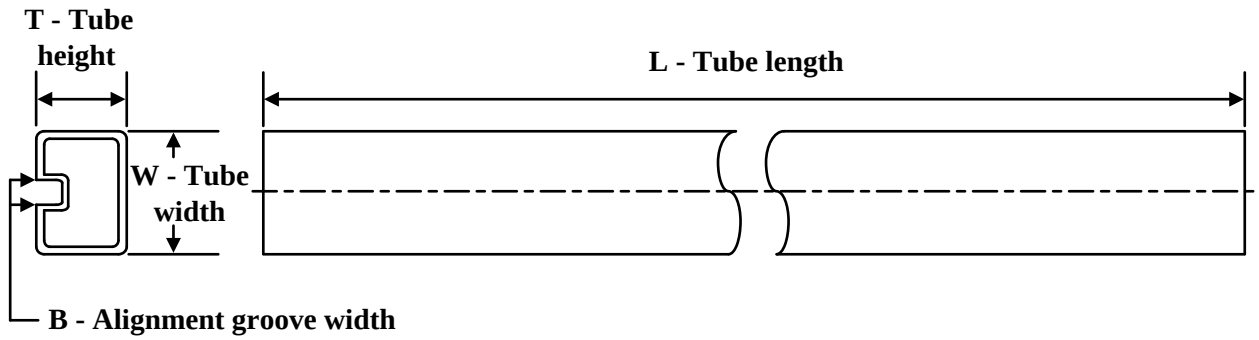
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24005PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
BQ24006PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ24004PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
BQ24004PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
BQ24005PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
BQ24005PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
BQ24005PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
BQ24006PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
BQ24006PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

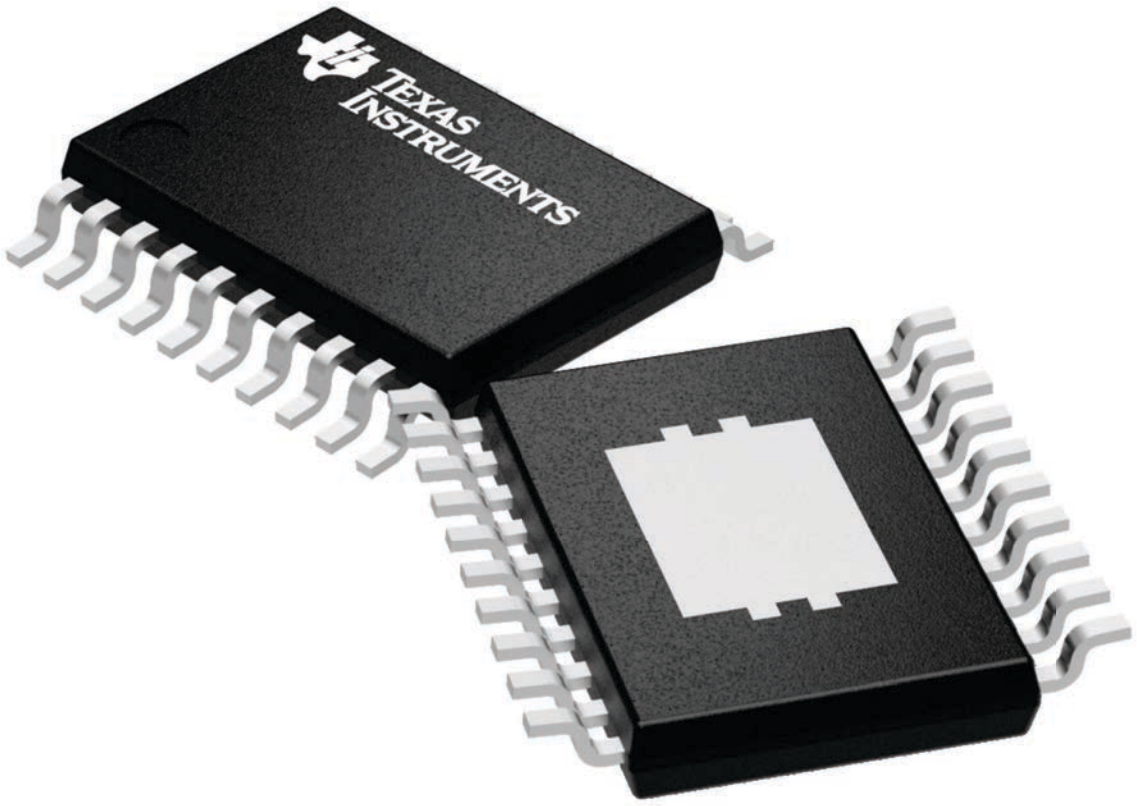
PWP 20

HTSSOP - 1.2 mm max height

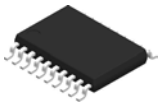
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

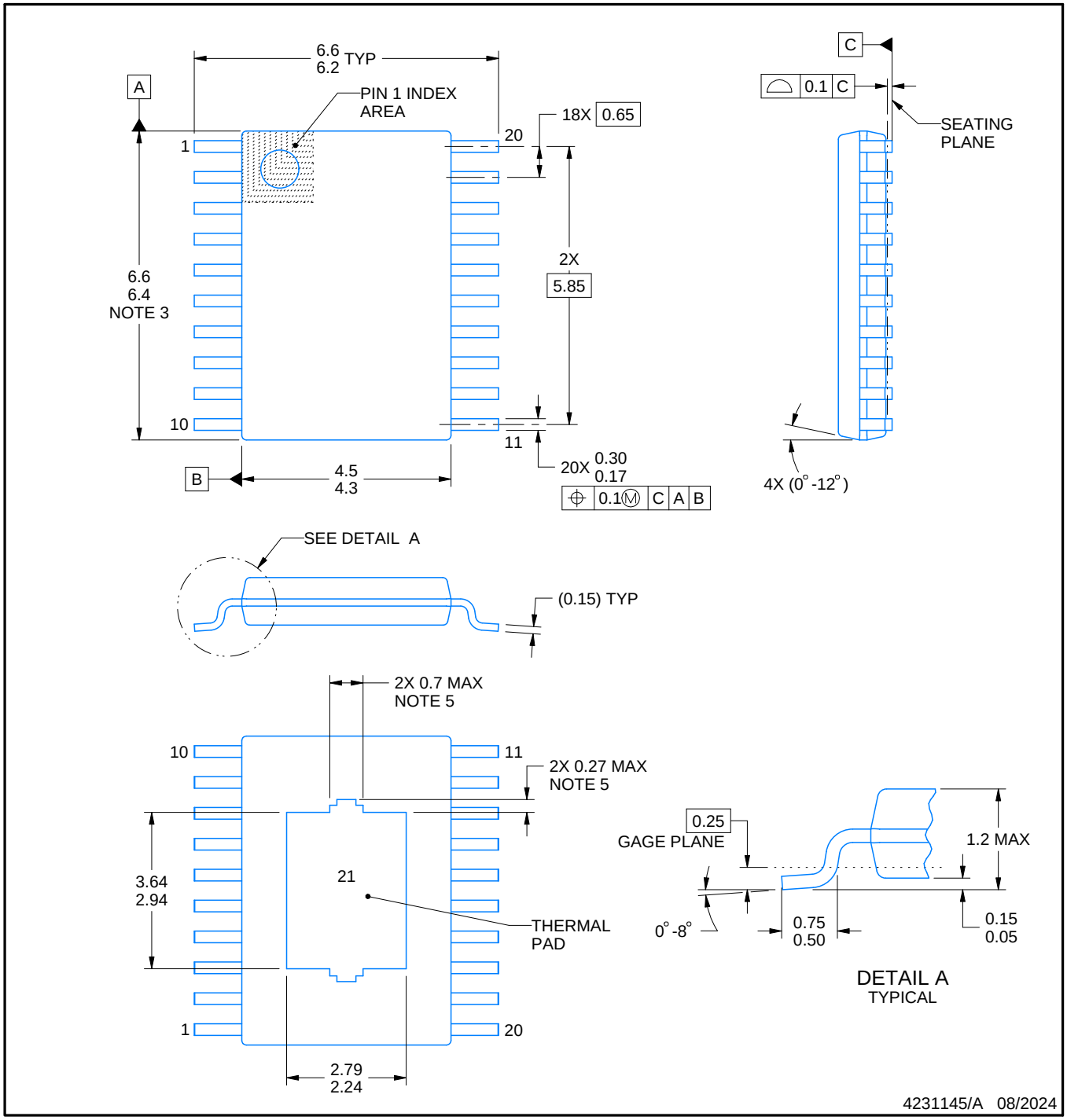


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

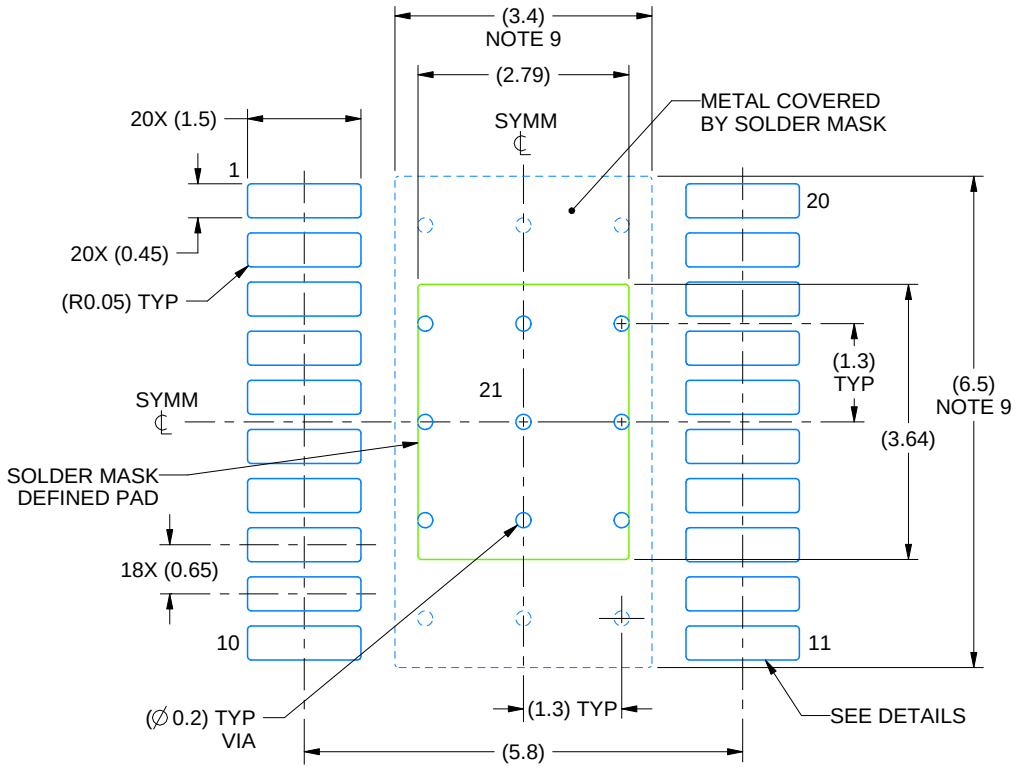
SMALL OUTLINE PACKAGE



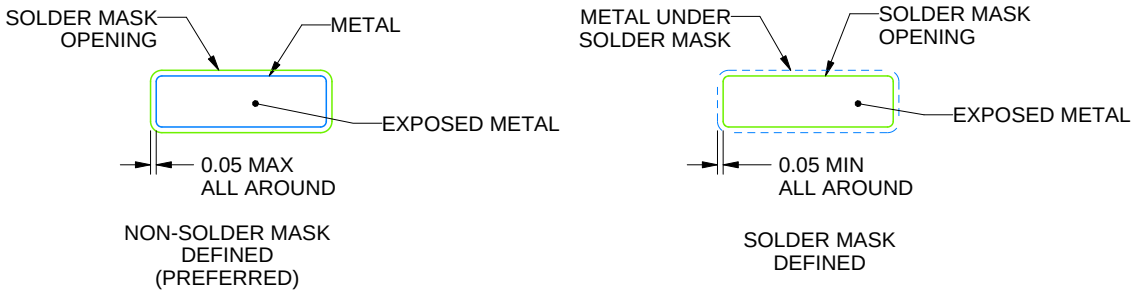
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

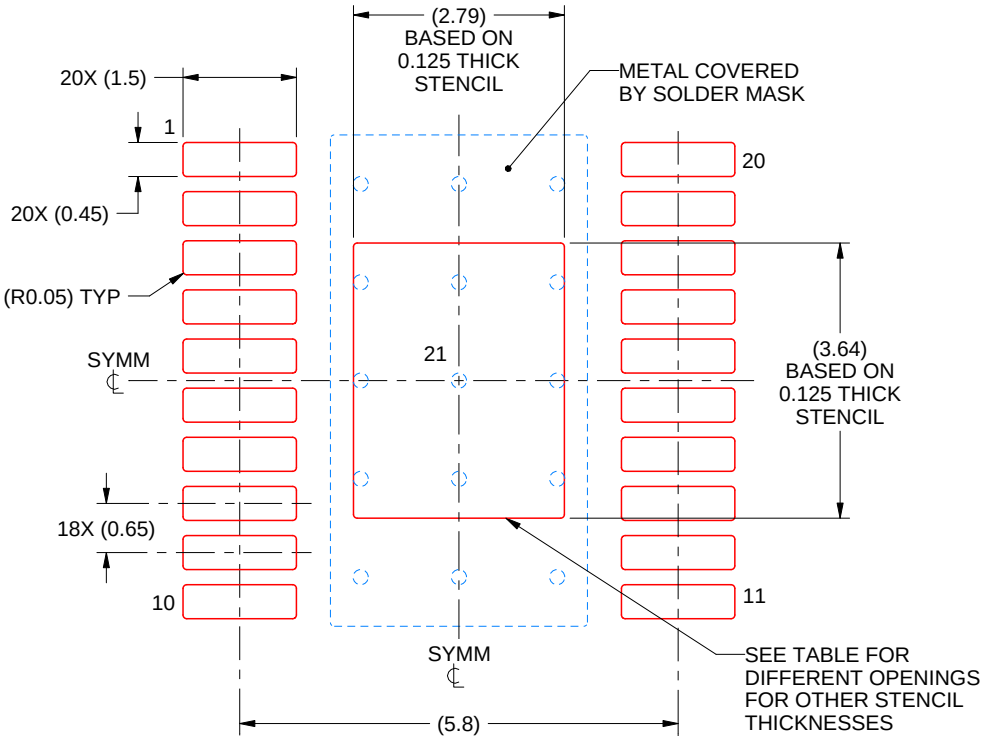


SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

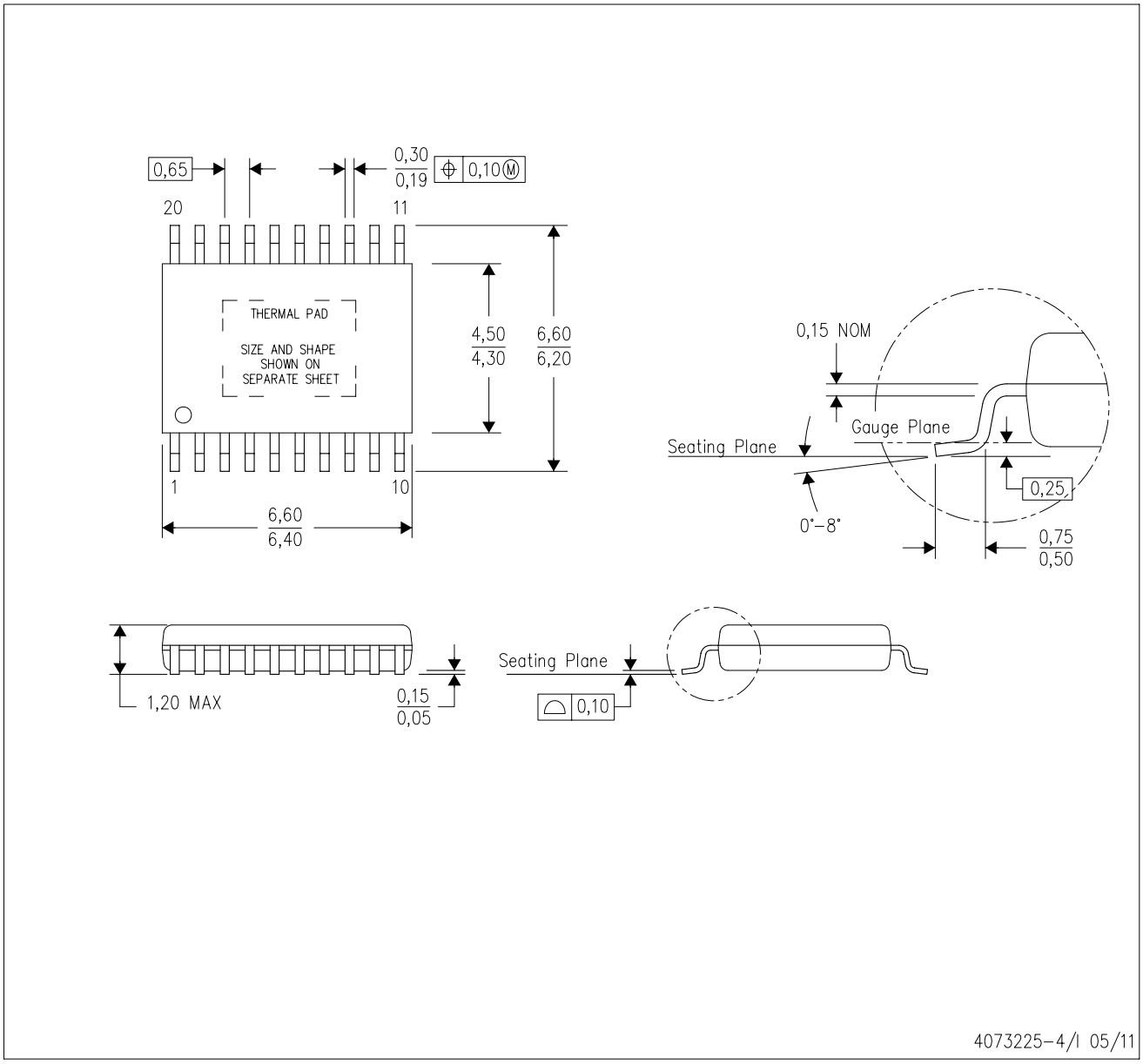
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

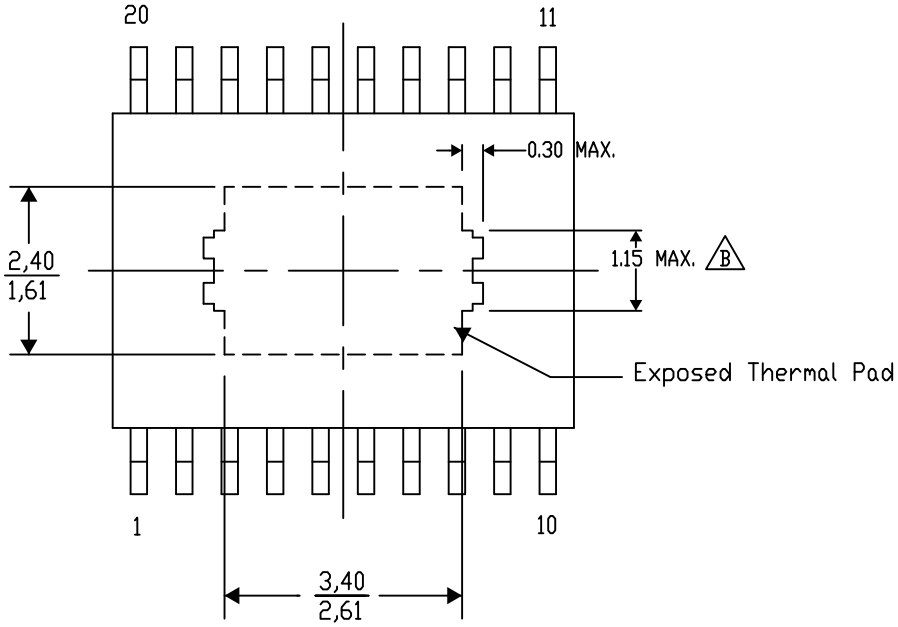
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

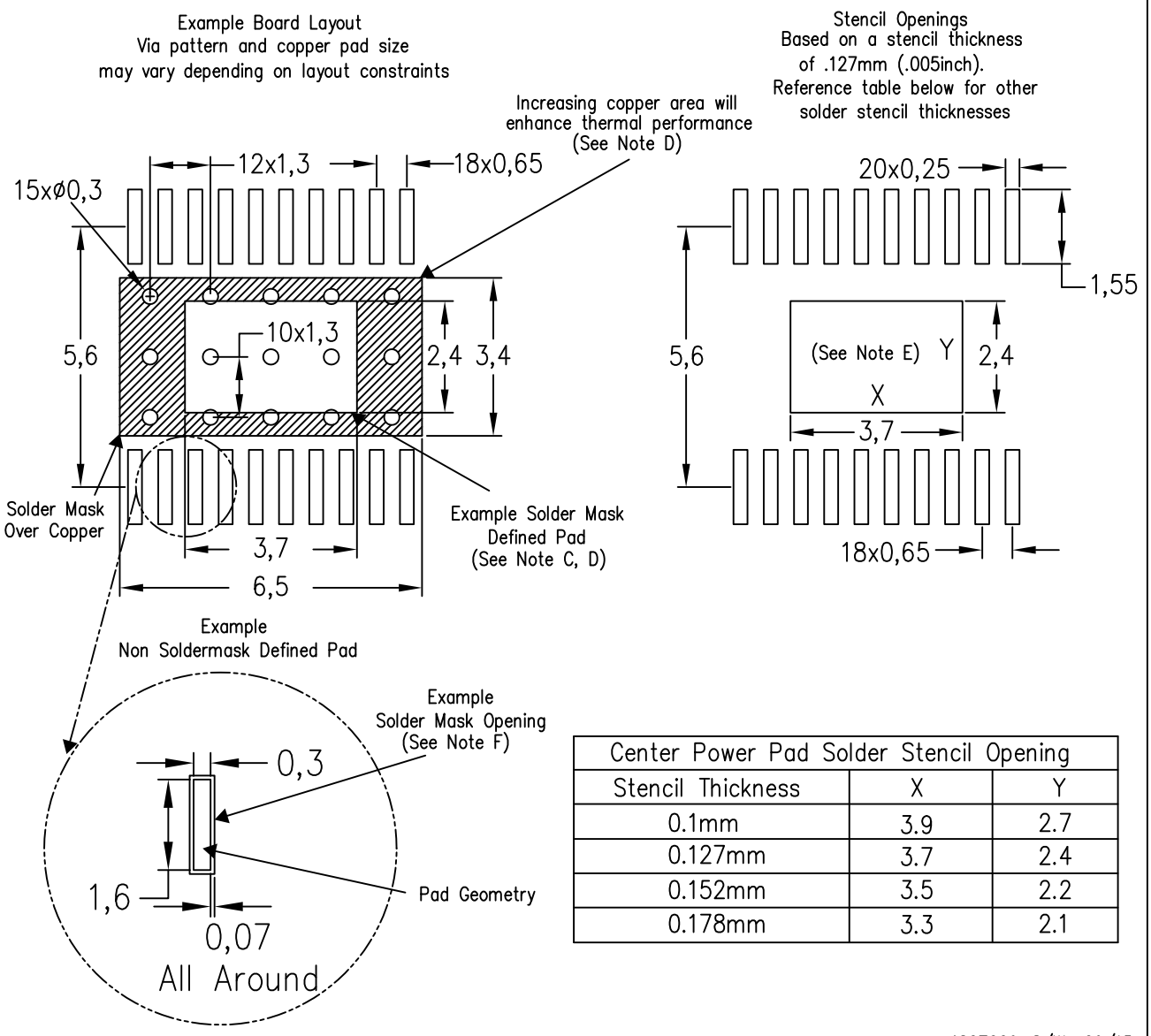
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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