



CYPRESS
SEMICONDUCTOR

T-46-23-12

PRELIMINARY

CY7C182

8,192 x 9 Static R/W RAM

Features

- Fast access time
 - Commercial: 25/35/45/55 ns (max.)
- Low power consumption
 - Active: 935 mW (max.)
- Wide temperature range
 - -55°C to +125°C
- 300-mil-width package
- TTL-compatible inputs and outputs
- Asynchronous
- Capable of withstanding greater than 2001V electrostatic discharge
- Single 5V supply

Functional Description

The CY7C182 is a high-speed CMOS static RAM organized as 8,192 by 9 bits and it is manufactured using Cypress's high-performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 935 mW.

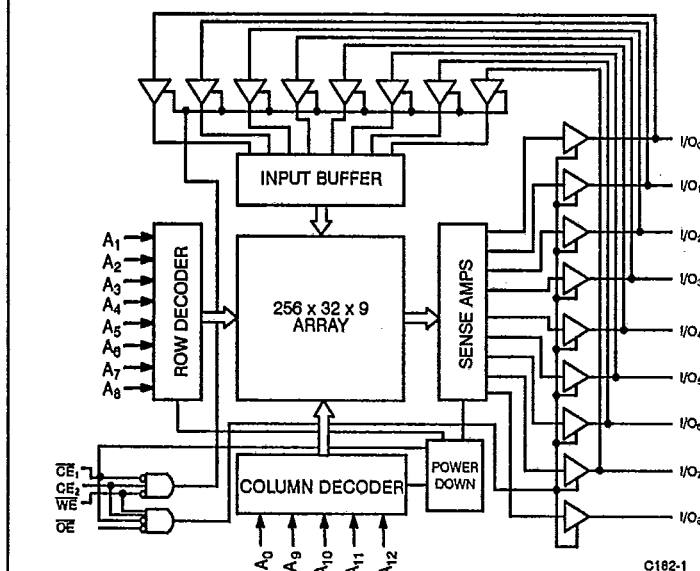
The CY7C182, which is oriented toward cache memory applications, features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85% when the circuit is deselected. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW, data on the nine data input/output pins (I/O_0 through I/O_8) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the nine data input/output pins.

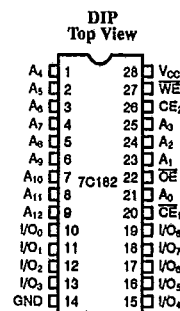
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration



C182-2

Selection Guide

	7C182-25	7C182-35	7C182-45	7C182-55
Maximum Access Time (ns)	25	35	45	55
Maximum Operating Current (mA)	170	170	170	170
Maximum Standby Current (mA)	25	25	25	25



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

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Storage Temperature - 65°C to + 150°C

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015.2)

Ambient Temperature with

Power Applied - 55°C to + 125°C

Latch-Up Current > 200 mA

Supply Voltage to Ground Potential - 0.5V to + 7.0V

DC Voltage Applied to Outputs

in High Z State - 0.5V to + 7.0V

DC Input Voltage - 3.0V to + 7.0V

Output Current into Outputs (Low) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%

2

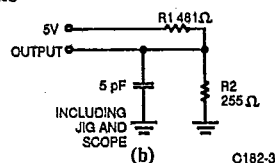
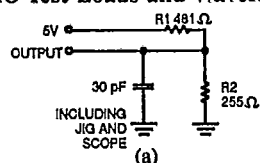
Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C182		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _{IN} ≤ V _{CC} , GND < V _{OUT} < V _{CC} , Output Disabled	-10	+ 10	μA
I _{OZ}	Output Leakage Current	V _{CC} = Max., V _{OUT} = GND	-10	+ 10	μA
I _{OS}	Output Short Circuit Current ^[1]	V _{CC} = Max., V _{OUT} = GND		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} Max., Output Current = 0 mA, f = Max., V _{IN} = V _{CC} or GND		170	mA
I _{SB}	Automatic Power-Down Current	$\overline{CE}_1 \geq V_{IH}$, $CE_2 \leq V_{IL}$		25	mA

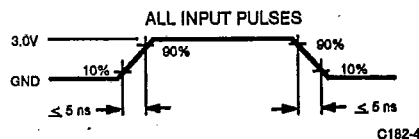
Capacitance^[2]

Parameters	Description	Test Conditions	Max.	Units
C _{OUT}	Output Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	7	pF
C _{IN}	Input Capacitance		5	pF

- Note:
1. Duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
 2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

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C182-4

Equivalent to: THEVENIN EQUIVALENT





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Switching Characteristics Over the Operating Range

Parameters	Description	7C182-25		7C182-35		7C182-45		7C182-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	25		35		45		55		ns
t _{AA}	Address to Data Valid		25		35		45		55	ns
t _{OHA}	Address Valid to Low Z	3		3		3		3		ns
t _{ACE1}	$\overline{CE}_1$ Access Time		25		35		45		55	ns
t _{ACE2}	CE ₂ Access Time		25		25		45		55	ns
t _{LZCE1}	$\overline{CE}_1$ LOW to Low Z	5		5		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	5		5		5		5		ns
t _{HZCE1} ^[3]	$\overline{CE}_1$ HIGH to High Z		20		20		25		25	ns
t _{HZCE2} ^[3]	CE ₂ LOW to High Z		20		20		25		25	
t _{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		25		25	ns
t _{DOE}	$\overline{OE}$ Access Time		20		20		20		25	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		25		30	ns
WRITE CYCLE ^[4]										
t _{WC}	Write Cycle Time	25		35		45		50		ns
t _{SA}	Address Set-Up Time	0		0		0		0		ns
t _{AW}	Address Valid to End of Write	20		30		40		50		ns
t _{SD}	Data Set-Up Time	18		20		25		30		ns
t _{SCB1}	$\overline{CE}_1$ LOW to Write End	20		30		40		50		ns
t _{SCB2}	CE ₂ HIGH to Write End	20		30		40		50		ns
t _{HZWE} ^[5]	Write LOW to High Z ^[7]		13		15		20		25	ns
t _{PWE}	$\overline{WE}$ Pulse Width	20		25		30		35		ns
t _{HA}	Address Hold from End of Write	5		5		5		5		ns
t _{HD}	Data Hold Time	0		0		0		0		ns
t _{LZWE}	Write HIGH to Low Z	3		3		3		3		ns

Notes:

- t_{HZCE} and t_{HZWB} are specified with $C_L = 5$ pF. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- At any given temperature and voltage condition, t_{LZWB} is less than t_{HZWB} for any given device. These parameters are sampled and not 100% tested.
- $\overline{WE}$ is HIGH for read cycle.
- Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- Address valid prior to or coincident with $\overline{CE}$ transition LOW and CE_2 transition HIGH.
- If $\overline{CE}_1$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

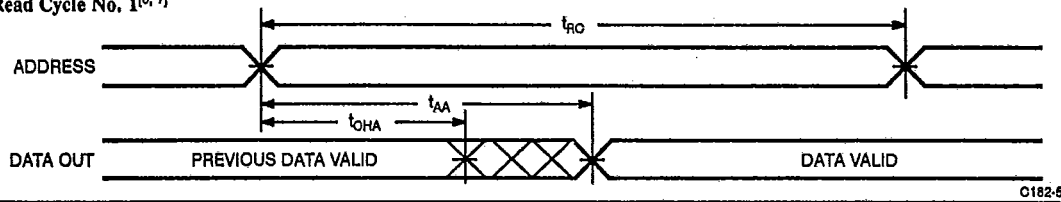


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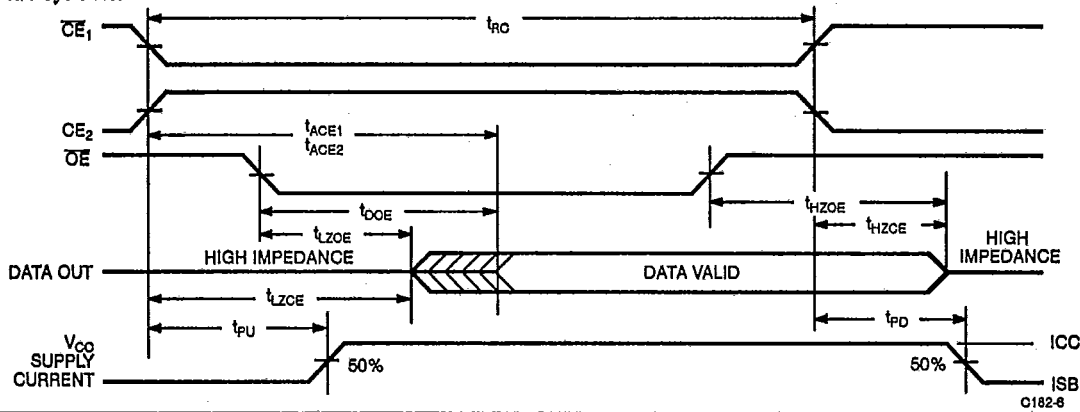
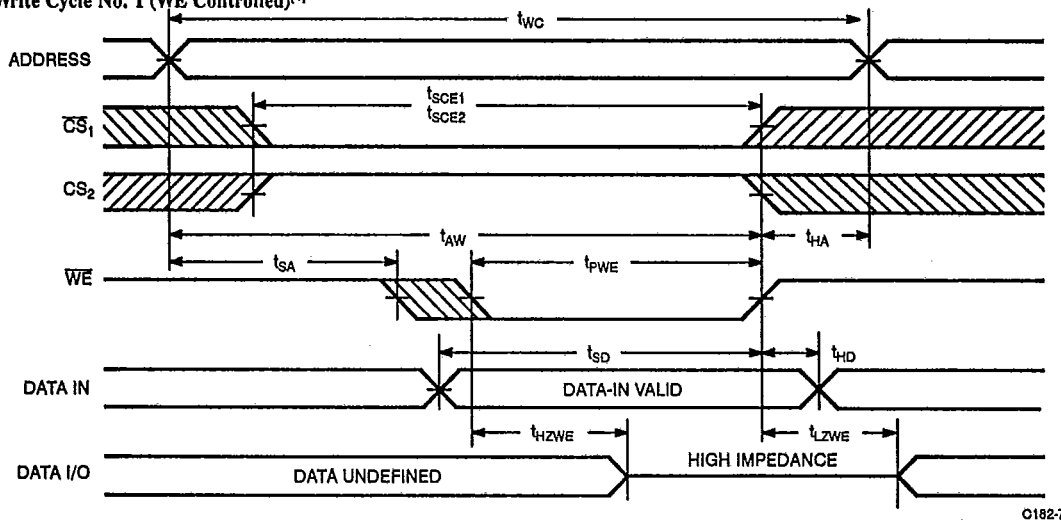
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Switching Waveforms

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Read Cycle No. 1^[6, 7]

2

Read Cycle No. 2^[6, 8]Write Cycle No. 1 ($\overline{WE}$ Controlled)^[4]

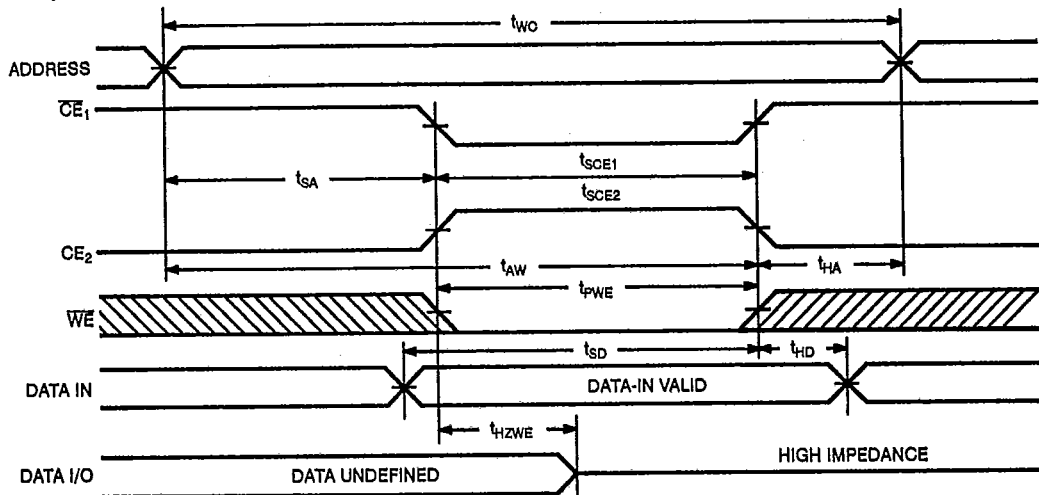


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Switching Waveforms (continued)

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Write Cycle No. 2 ($\overline{CE}$ Controlled)^(4,9)

0182-8

Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	Data-In	Data-Out	Mode
H	X	X	X	Z	Z	Deselect/Power-Down
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output Disable
X	L	X	X	Z	Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C182-25PC	P21	Commercial
	CY7C182-25VC	V21	
	CY7C182-25DC	D22	
35	CY7C182-35PC	P21	Commercial
	CY7C182-35VC	V21	
	CY7C182-35DC	D22	
45	CY7C182-45PC	P21	Commercial
	CY7C182-45VC	V21	
	CY7C182-45DC	D22	
55	CY7C182-55PC	P21	Commercial
	CY7C182-55VC	V21	
	CY7C182-55DC	D22	

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