



74ALVCH16821

20-bit bus-interface D-type flip-flop; positive-edge trigger;
3-state

Rev. 4 — 9 July 2024

Product data sheet

1. General description

The 74ALVCH16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-state output buffer. The two sections of each register are controlled independently by the clock (nCP) and output enable nOE control gates.

Each register is fully edge triggered. The state of each nDn input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's nQn output.

When nOE is LOW, the data in the register appears at the outputs. When nOE is HIGH, the outputs are in high impedance OFF state. Operation of the nOE input does not affect the state of the flip-flops.

The 74ALVCH16821 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50 Ω transmission lines at 85°C
- All data inputs have bushold
- Complies with JEDEC standard no. 8-1A
- Complies with JEDEC standards:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVCH16821DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram

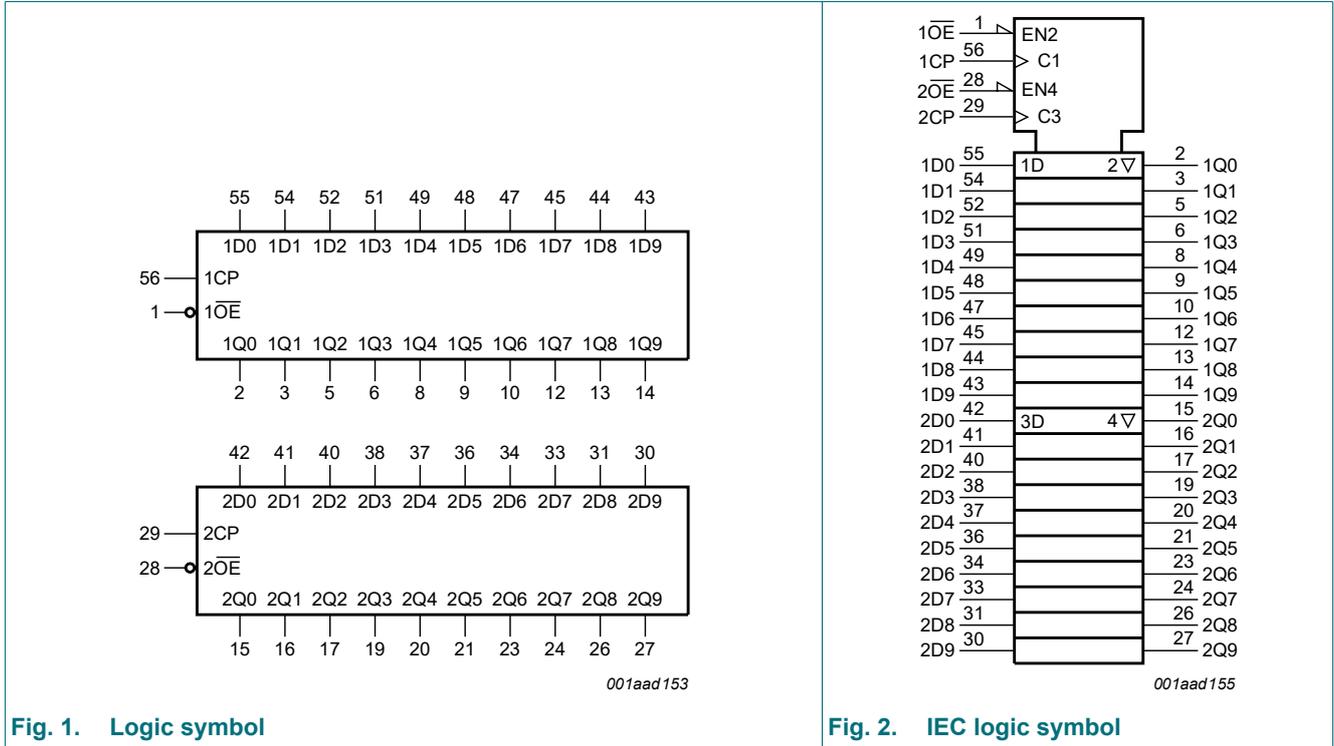


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

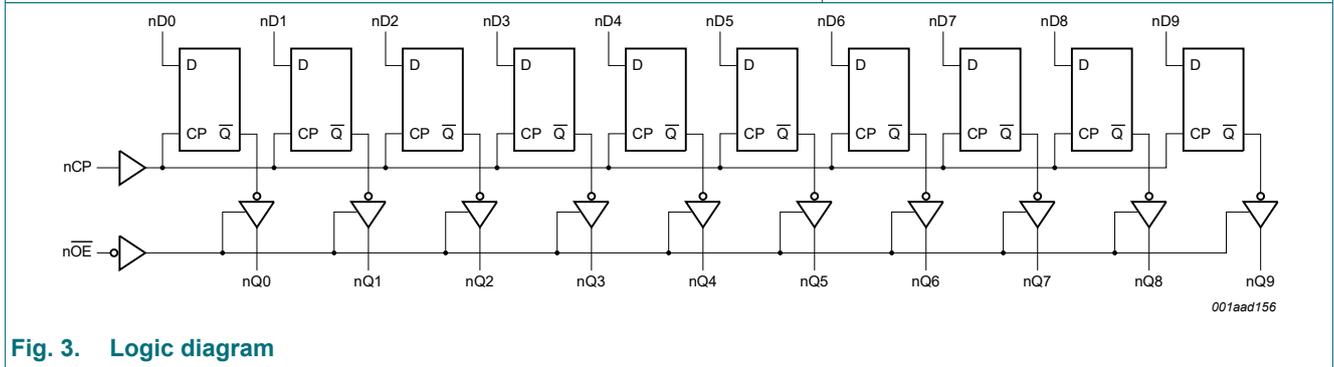
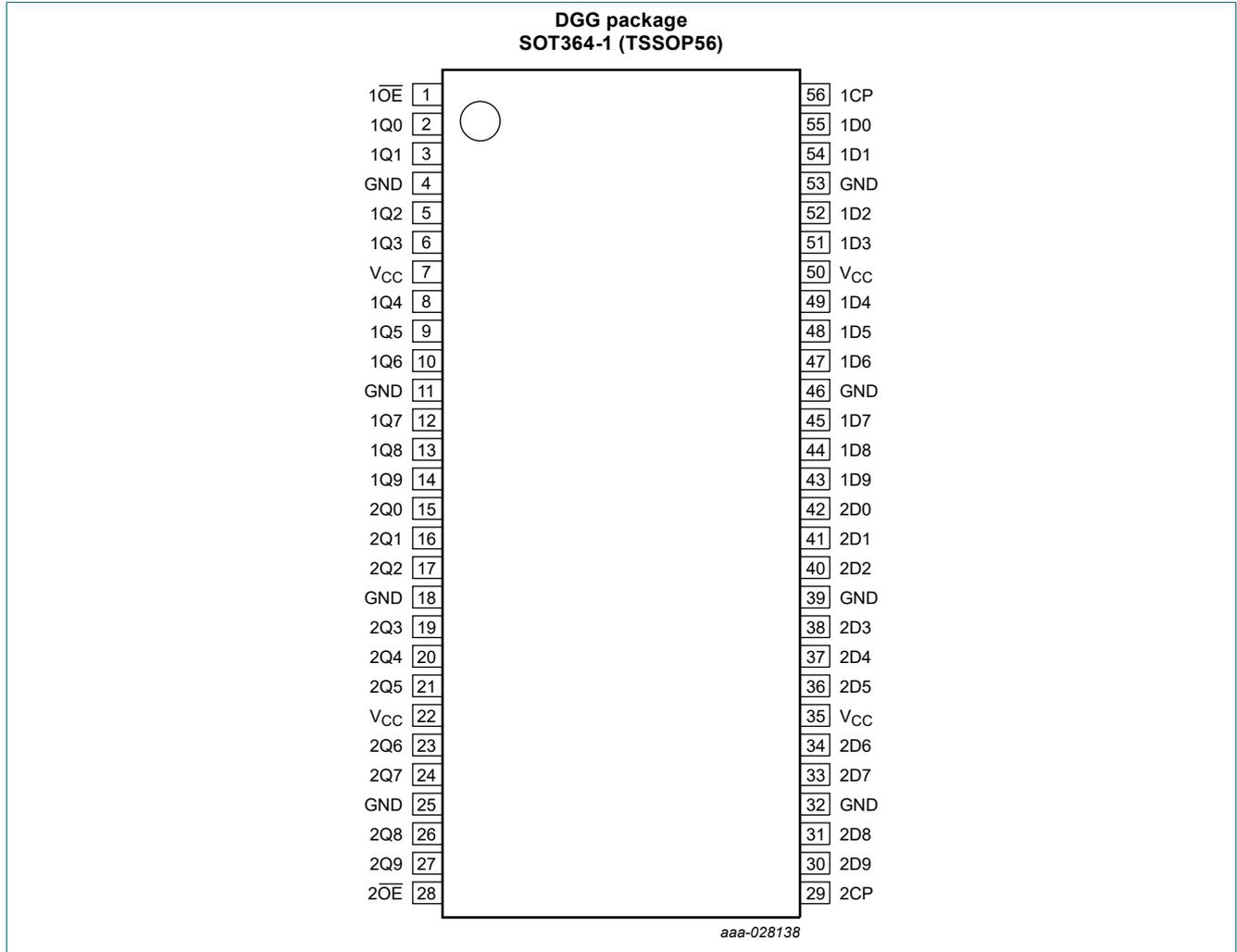


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8, 1D9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8, 2D9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8, 1Q9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8, 2Q9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data outputs
1OE, 2OE	1, 28	output enable inputs (active LOW)
1CP, 2CP	56, 29	clock pulse inputs (active rising edge)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V _{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

NC = no change; X = don't care; Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

Operating mode	Input			Internal register	Output nQn
	nOE	nCP	nDn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	nDn	nDn	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	For control pins [1]	-0.5	+4.6	V
		For data inputs [1]	-0.5	$V_{CC} + 0.5$	V
V_O	output voltage	[1]	-0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
$I_{O(sink/source)}$	output sink or source current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	2.5 V range for maximum speed performance at 30 pF output load	2.3	2.7	V
		3.3 V range for maximum speed performance at 50 pF output load	3.0	3.6	V
V_I	input voltage		0	V_{CC}	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.3	V _{CC} - 0.08	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.26	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.14	-	V
		I _O = -12 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	V _{CC} - 0.09	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.28	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.07	0.40	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.15	0.70	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.14	0.40	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.27	0.55	V
I _I	input leakage current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND	-	0.1	5	µA
I _{OZ}	OFF-state output current	V _{CC} = 2.7 V to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	0.1	10	µA
I _{CC}	supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	40	µA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	150	750	µA
I _{BHL}	bus hold LOW current	V _{CC} = 2.3 V; V _I = 0.7 V	45	-	-	µA
		V _{CC} = 3.0 V; V _I = 0.8 V	75	150	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 2.3 V; V _I = 1.7 V	-45	-	-	µA
		V _{CC} = 3.0 V; V _I = 2.0 V	-75	-175	-	µA
I _{BHLO}	bus hold LOW overdrive current	per data input; V _{CC} = 3.6 V	500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	per data input; V _{CC} = 3.6 V	-500	-	-	µA
C _I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t _{pd}	propagation delay	nCP to nQn; see Fig. 4 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	5.8	ns
		V _{CC} = 2.7 V	1.0	2.8	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	4.5	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nQn; see Fig. 6 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.8	6.6	ns
		V _{CC} = 2.7 V	1.0	3.2	6.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	5.1	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nQn; see Fig. 6 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.2	5.7	ns
		V _{CC} = 2.7 V	1.0	3.1	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.8	4.6	ns
t _{su}	set-up time	nDn to nCP; see Fig. 5				
		V _{CC} = 2.3 V to 2.7 V	1.4	0.3	-	ns
		V _{CC} = 2.7 V	1.2	0.3	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	0.2	-	ns
t _h	hold time	nDn to nCP; see Fig. 5				
		V _{CC} = 2.3 V to 2.7 V	0.4	0.0	-	ns
		V _{CC} = 2.7 V	0.6	-0.3	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	0.4	-	ns
t _w	pulse width	nCP HIGH or LOW; see Fig. 4				
		V _{CC} = 2.3 V to 2.7 V	3.0	1.8	-	ns
		V _{CC} = 2.7 V	3.3	1.7	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.3	0.2	-	ns
f _{max}	maximum frequency	nCP; see Fig. 4				-
		V _{CC} = 2.3 V to 2.7 V	150	250	-	MHz
		V _{CC} = 2.7 V	150	300	-	MHz
		V _{CC} = 3.0 V to 3.6 V	150	350	-	MHz
C _{PD}	power dissipation capacitance	per latch; V _i = GND to V _{CC} [3]				
		outputs enabled	-	33	-	pF
		outputs disabled	-	17	-	pF

[1] Typical values are measured at T_{amb} = 25 °C

Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.

Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

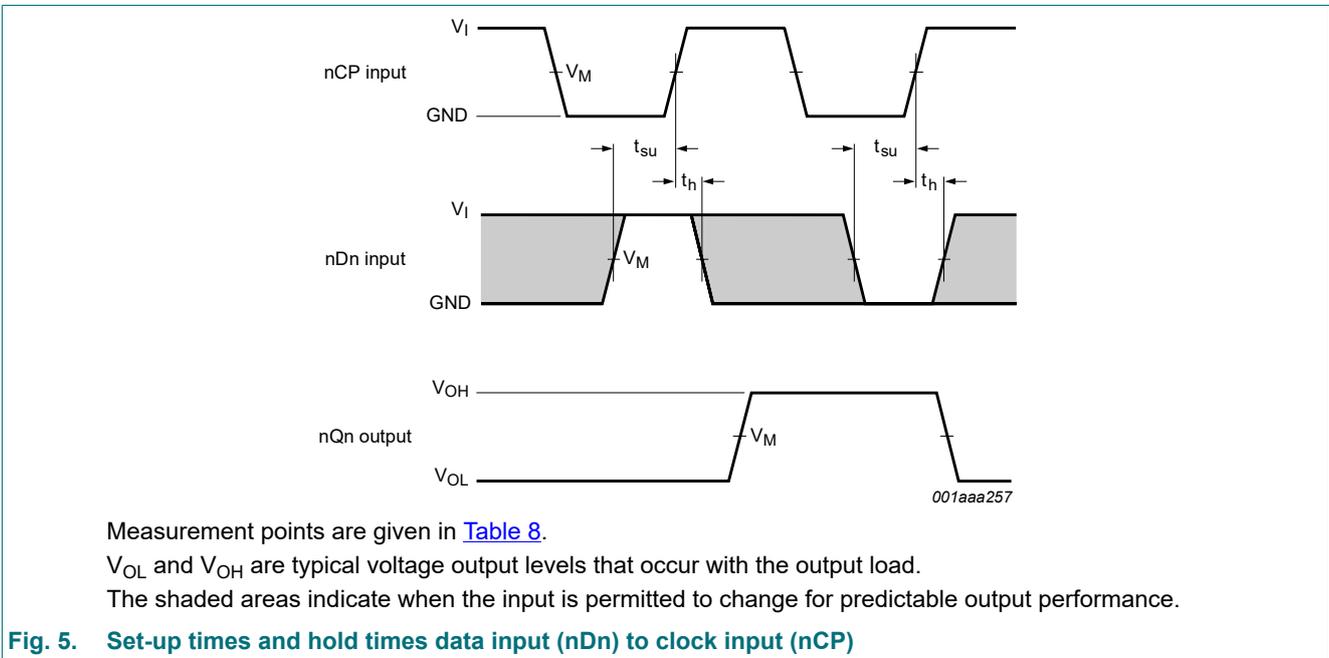
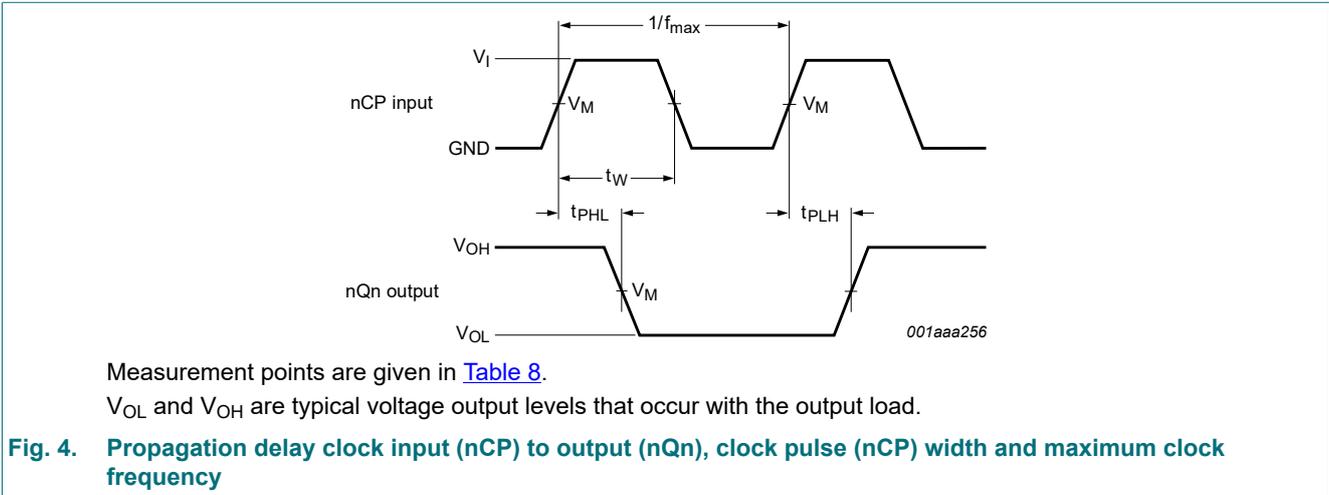
[2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). P_D = C_{PD} × V_{CC}² × f_i × N + ∑ (C_L × V_{CC}² × f_o) where:

f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts; N = total load switching outputs; ∑ (C_L × V_{CC}² × f_o) = sum of outputs.

10.1. Waveforms and test circuit



20-bit bus-interface D-type flip-flop; positive-edge trigger; 3-state

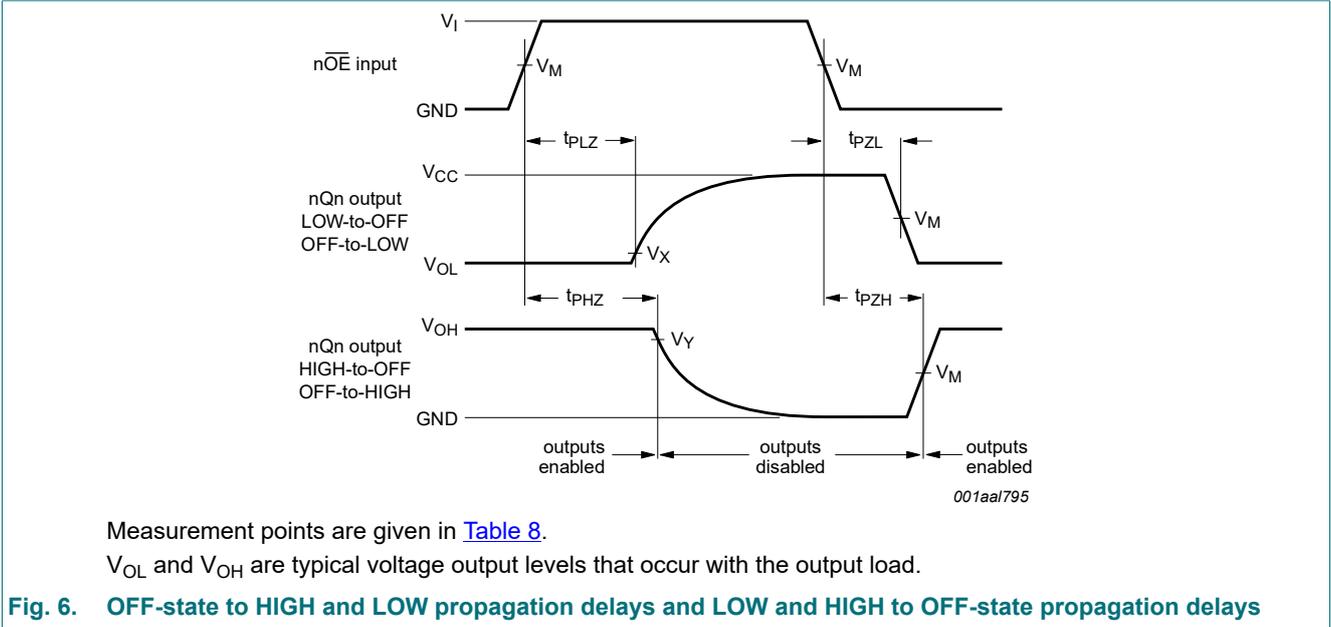


Table 8. Measurement points

V_{CC}	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
< 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
$\geq 2.7 \text{ V}$	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

20-bit bus-interface D-type flip-flop; positive-edge trigger; 3-state

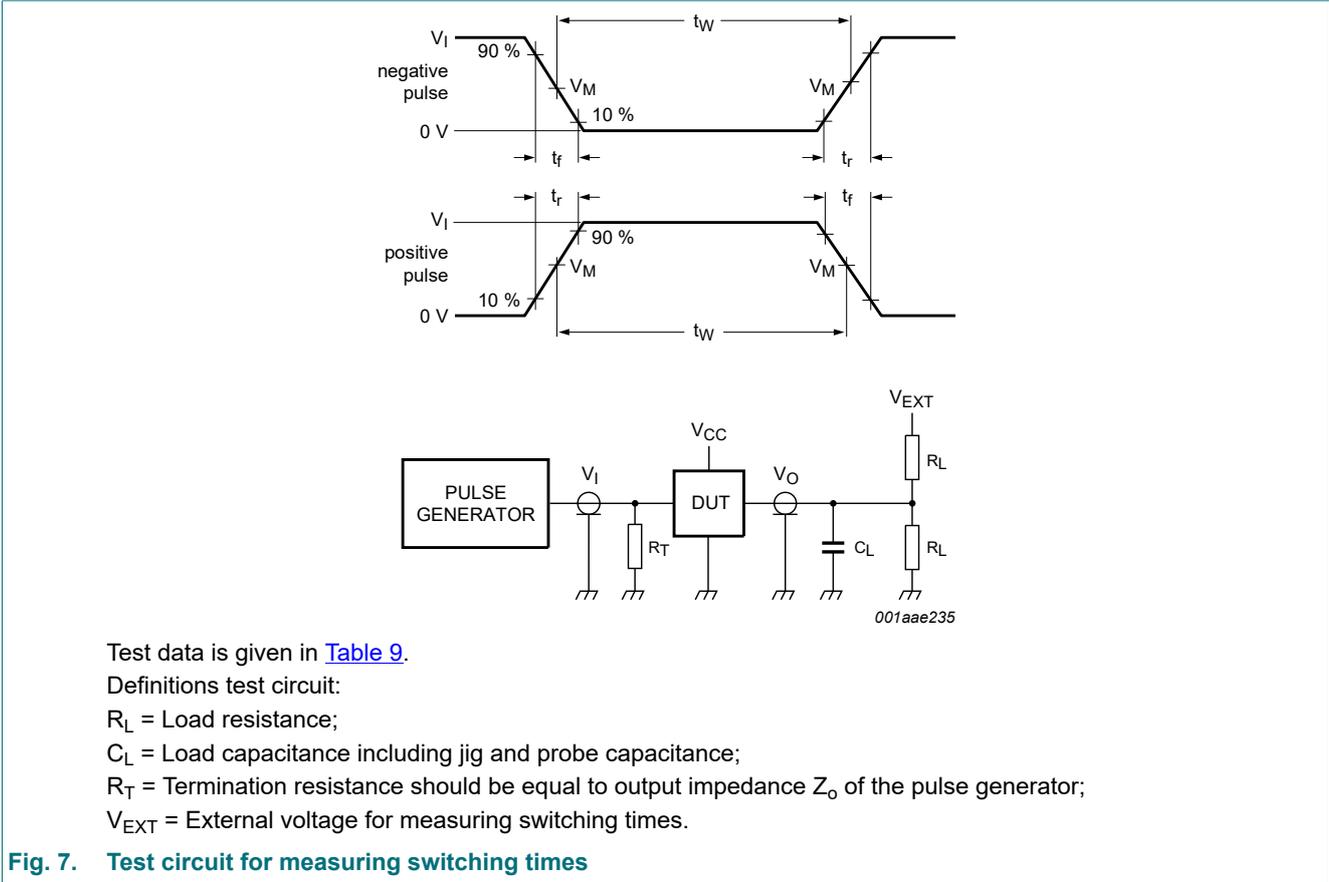


Table 9. Test data

Input			Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
< 2.7 V	V_{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	$2 \times V_{CC}$	open
≥ 2.7 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	$2 \times V_{CC}$	open

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

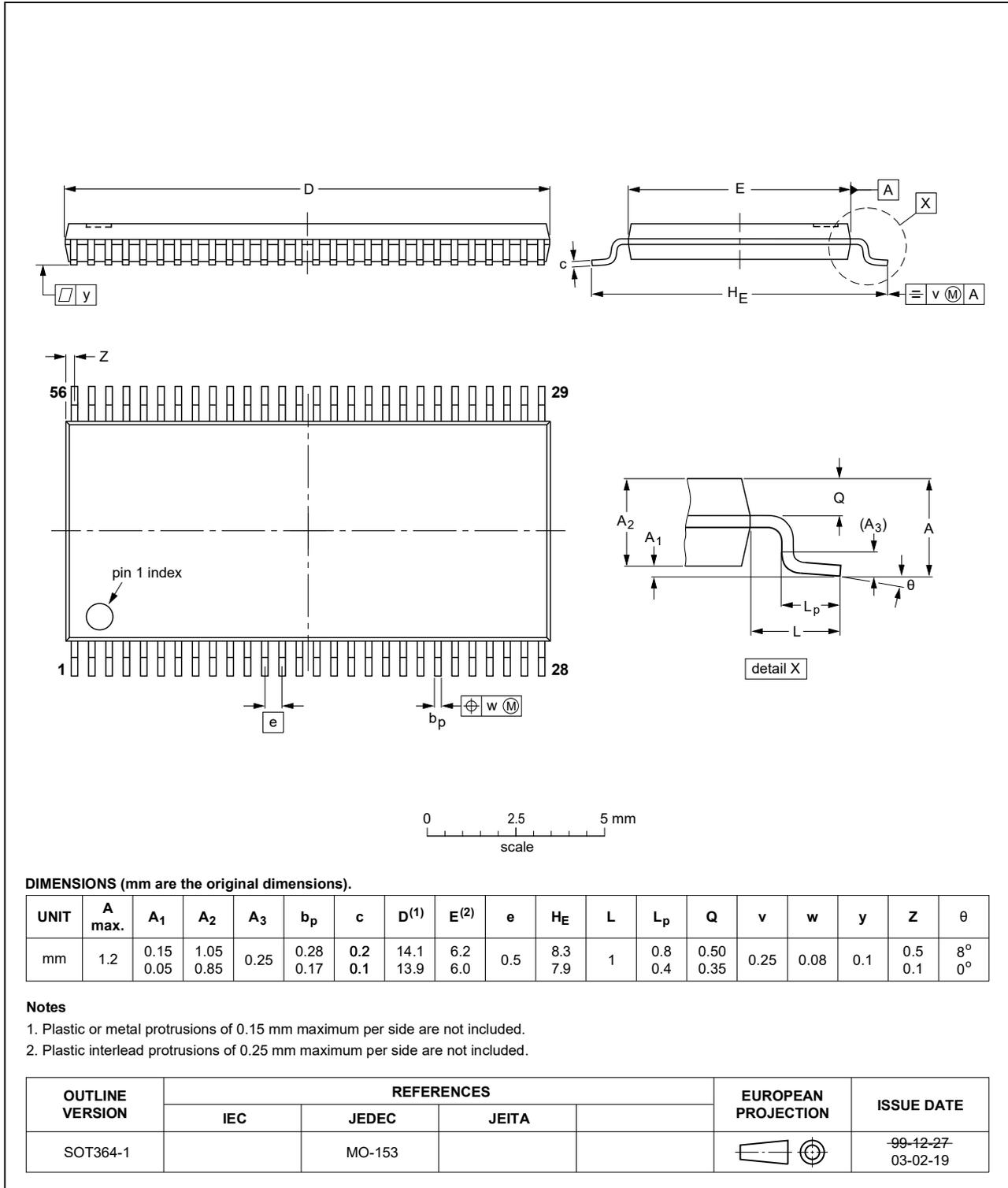


Fig. 8. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16821 v.4	20240709	Product data sheet	-	74ALVCH16821 v.3
Modifications:	<ul style="list-style-type: none"> Table 4: P_{tot} total power dissipation updated. Section 2: ESD specification updated according to the latest JEDEC standard. 			
74ALVCH16821 v.3	20180202	Product data sheet	-	74ALVCH16821 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74ALVCH16821DL (SOT371-1 / SSOP56) removed 			
74ALVCH16821 v.2	19980529	Product specification	-	74ALVCH16821 v.1
74ALVCH16821 v.1	19980529	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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