

FDS4435

Single P-Channel, Logic Level, PowerTrench™ MOSFET

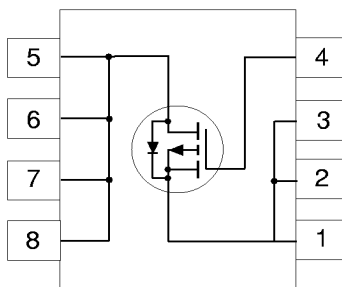
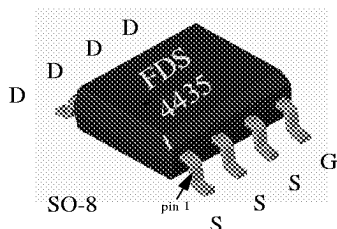
General Description

This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- -9 A, -30 V. $R_{DS(ON)} = 0.0185 \Omega$ @ $V_{GS} = -10$ V,
 $R_{DS(ON)} = 0.0300 \Omega$ @ $V_{GS} = -4.5$ V.
- Low gate charge (21nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.



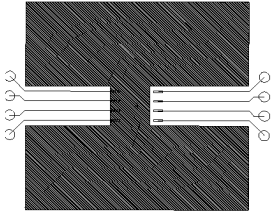
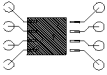
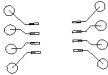
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDS4435	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	-9	A
	- Pulsed	-50	
P_D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Electrical Characteristics (T _A = 25 °C unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-30			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25 °C		-26		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μA
		T _J = 55°C			-10	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-1	-1.7	-3	V
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		4.2		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -9 A		0.015	0.0185	Ω
		T _J = 125°C		0.021	0.03	
		V _{GS} = -4.5 V, I _D = -7 A		0.023	0.03	
I _{D(on)}	On-State Drain Current	V _{GS} = -10 V, V _{DS} = -5 V	-40			A
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -9 A		25		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz		2010		pF
C _{oss}	Output Capacitance			590		pF
C _{rss}	Reverse Transfer Capacitance			260		pF
SWITCHING CHARACTERISTICS (Note 2)						
t _{D(on)}	Turn - On Delay Time	V _{DS} = -15 V, I _D = -1 A		12	22	ns
t _r	Turn - On Rise Time	V _{GEN} = -10 V, R _{GEN} = 6 Ω		15	27	ns
t _{D(off)}	Turn - Off Delay Time			100	140	ns
t _f	Turn - Off Fall Time			55	80	ns
Q _g	Total Gate Charge	V _{DS} = -15 V, I _D = -9 A,		21	30	nC
Q _{gs}	Gate-Source Charge	V _{GS} = -5 V		6		nC
Q _{gd}	Gate-Drain Charge			8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -2.1 A (Note 2)		-0.75	-1.2	V
t _{rr}	Source-Drain Reverse Recovery Time	I _F = -10 A, dI _F /dt = 100 A/μS		36	80	ns
Notes:						
1. R _{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R _{θJA} is guaranteed by design while R _{θCA} is determined by the user's board design.						
   a. 50°C/W on a 1 in² pad of 2oz copper. b. 105°C/W on a 0.04 in² pad of 2oz copper. c. 125°C/W on a 0.006 in² pad of 2oz copper. Scale 1 : 1 on letter size paper						
2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.						

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Typical Electrical Characteristics

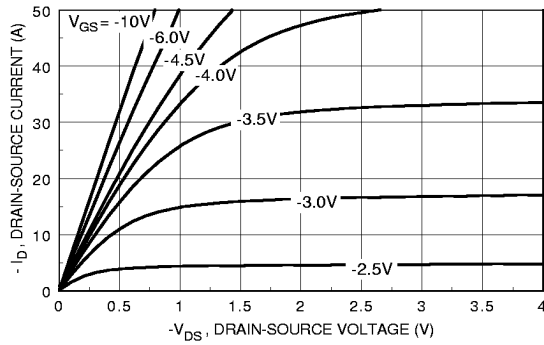


Figure 1. On-Region Characteristics.

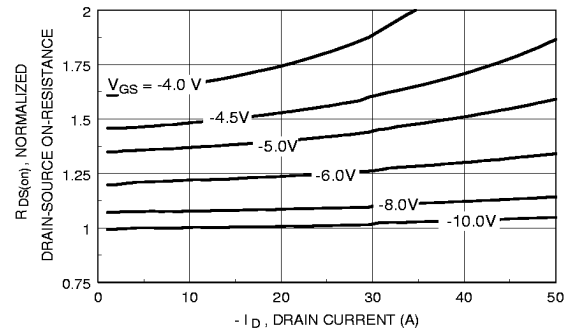


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

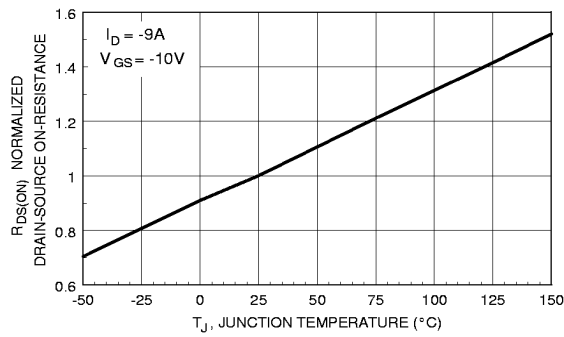


Figure 3. On-Resistance Variation with Temperature.

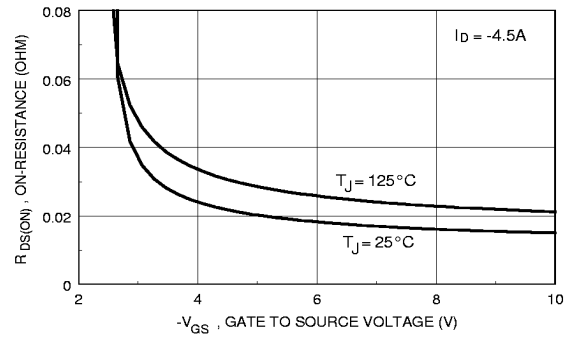


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

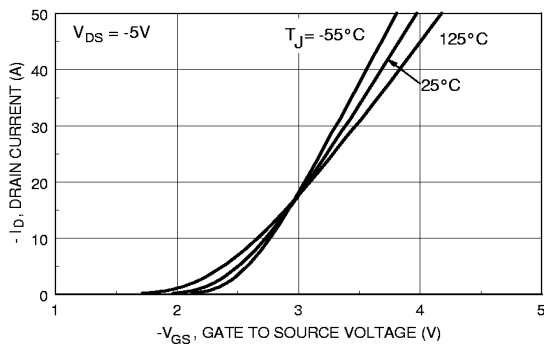


Figure 5. Transfer Characteristics.

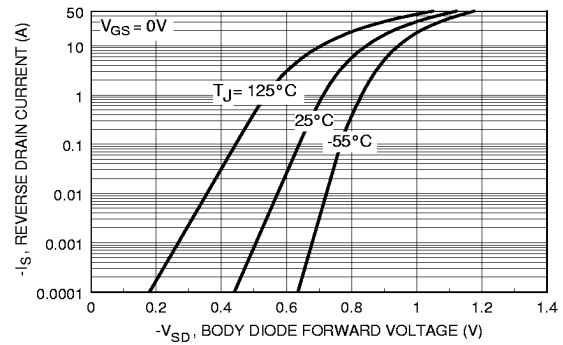


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

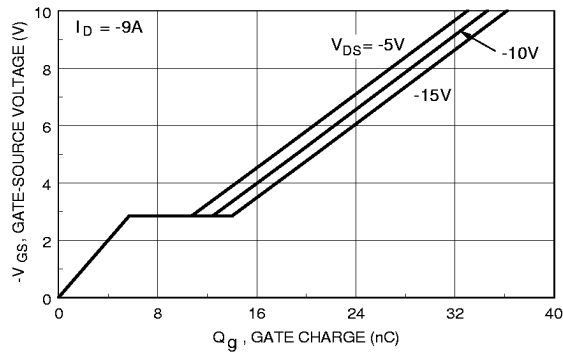


Figure 7. Gate Charge Characteristics.

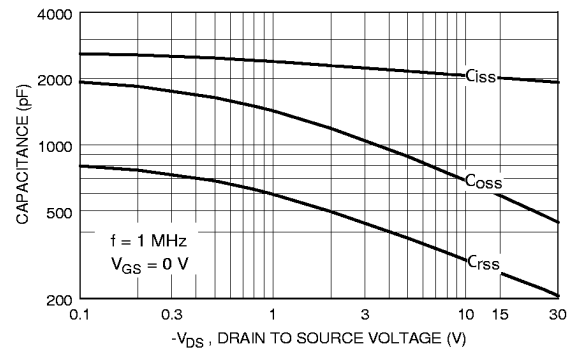


Figure 8. Capacitance Characteristics.

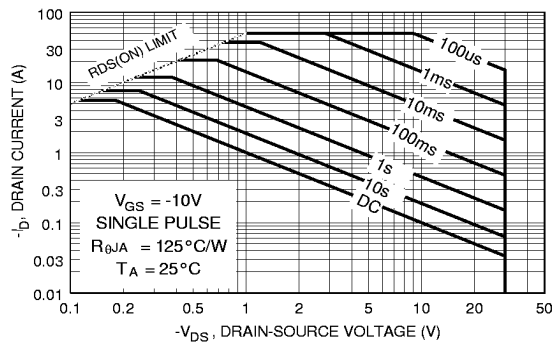


Figure 9. Maximum Safe Operating Area.

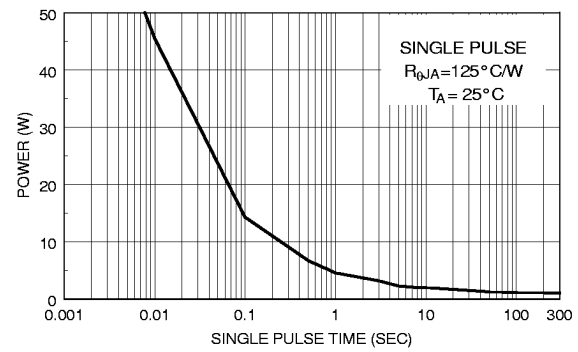


Figure 10. Single Pulse Maximum Power Dissipation.

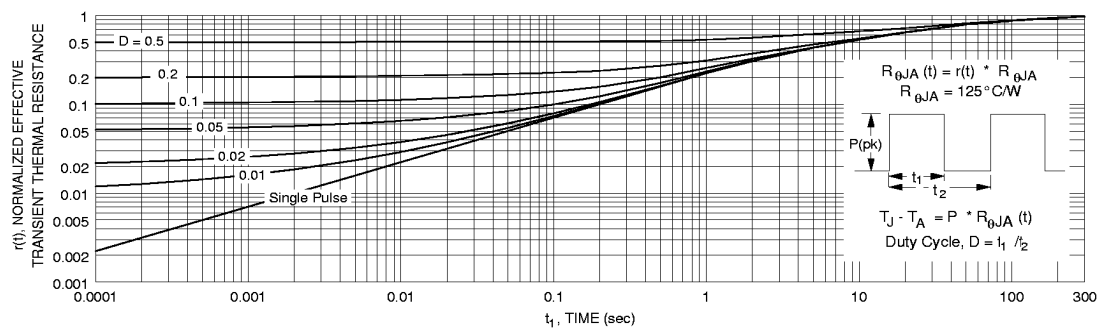


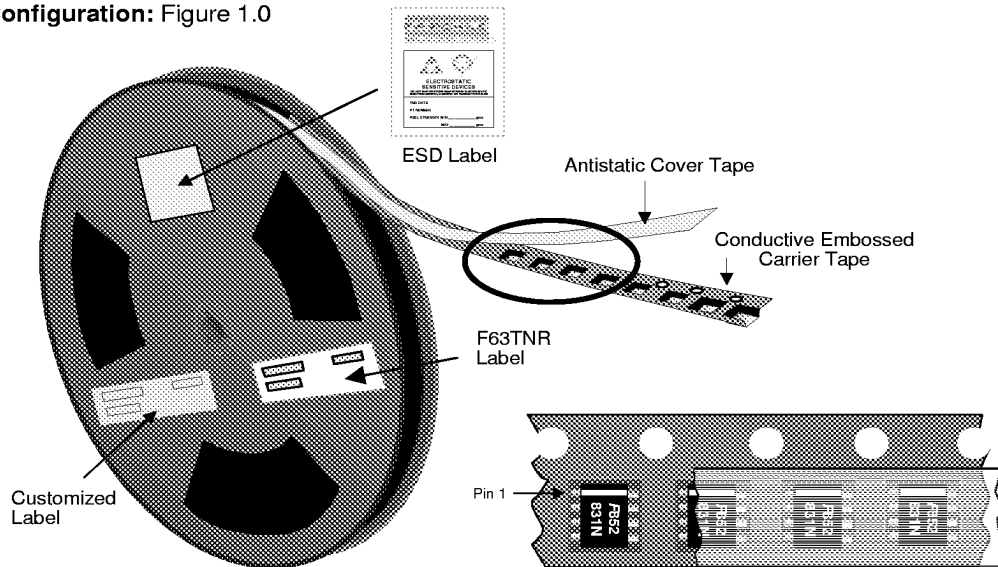
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions



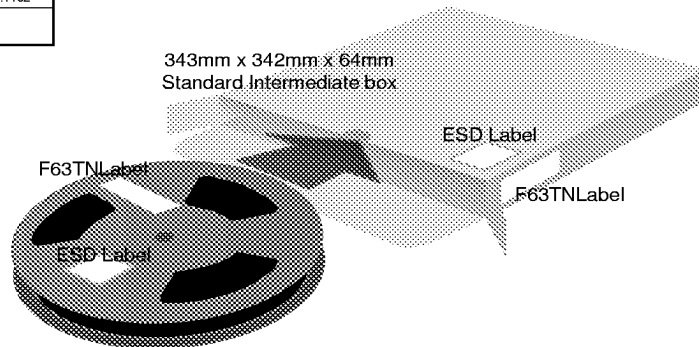
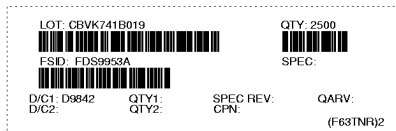
SOIC(8lds) Packaging Configuration: Figure 1.0



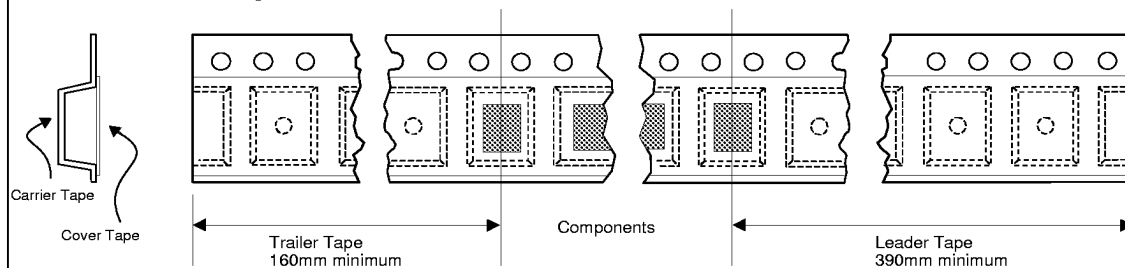
SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	S62Z	D84Z
Packaging type	TNR	Rail/Tube	Bag	TNR
Qty per Reel/Tube/Bag	2,500	95	200	500
Reel Size	13" Dia	-	-	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	76x102x127	184x187x47
Max qty per Box	5,000	30,000	1,000	2,500
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	-	0.1182
Note/Comments			Bulk	

F63TNR Label sample



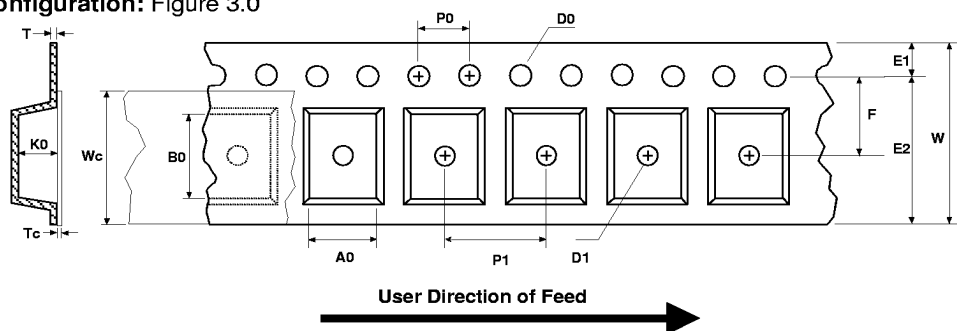
SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



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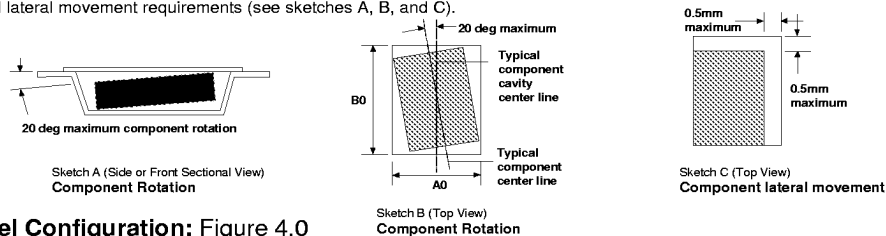
SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0

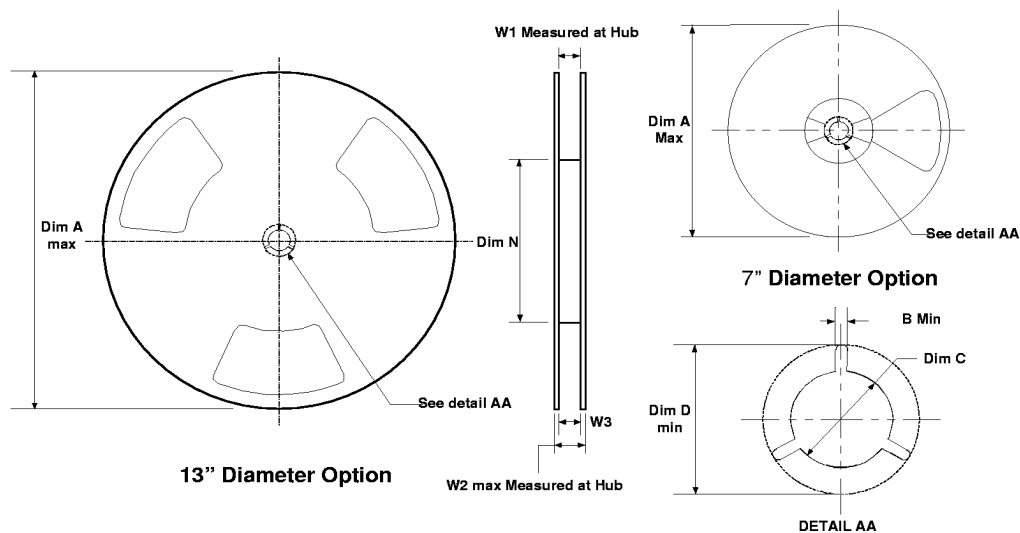


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



SOIC(8lds) Reel Configuration: Figure 4.0

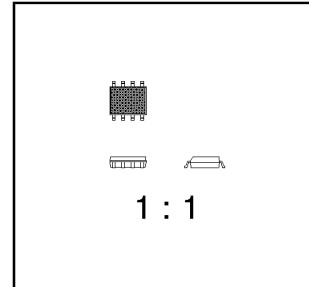
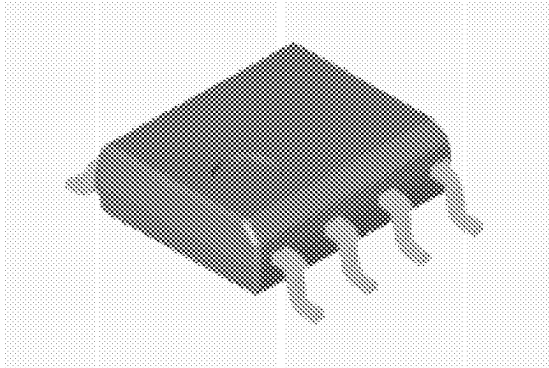


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

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SO-8 Tape and Reel Data and Package Dimensions, continued

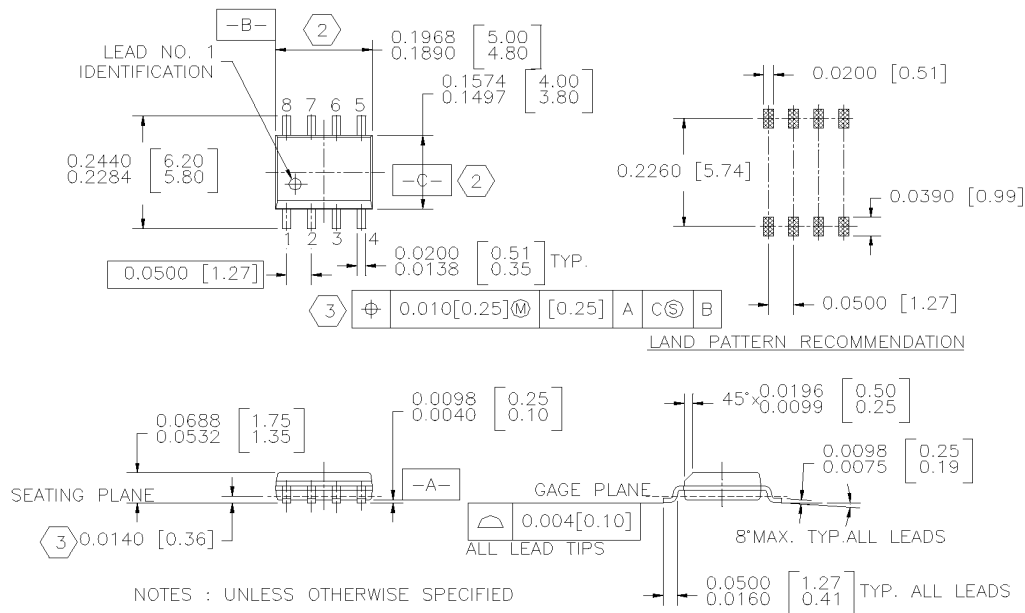
SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
200 MICRINCHES / 5.08 MICRONS MINIMUM
LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

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