

114 dB, 192 kHz 6-Ch Codec with PLL

Features

- Six 24-bit D/A, two 24-bit A/D converters
- 114 dB DAC / 114 dB ADC dynamic range
- -100 dB THD+N
- System sampling rates up to 192 kHz
- Integrated low-jitter PLL for increased system jitter tolerance
- PLL clock or OMCK system clock selection
- 7 configurable general purpose outputs
- ADC high pass filter for DC offset calibration
- Expandable ADC channels and one-line mode support
- Digital output volume control with soft ramp
- Digital +/-15 dB input gain adjust for ADC
- Differential analog architecture
- Supports logic levels between 5 V and 1.8 V

General Description

The CS42426 CODEC provides two analog-to-digital and six digital-to-analog Delta-Sigma converters, as well as an integrated PLL, in a 64-pin LQFP package.

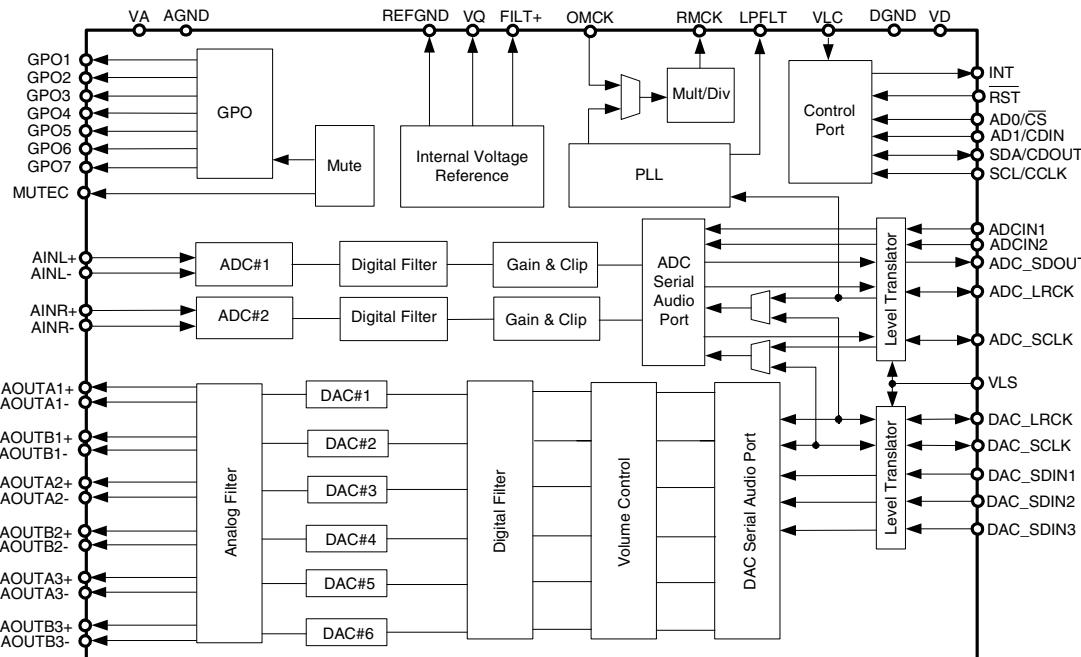
The CS42426 integrated PLL provides a low-jitter system clock. The internal stereo ADC is capable of independent channel gain control for single-ended or differential analog inputs. All six channels of DAC provide digital volume control and differential analog outputs. The general purpose outputs may be driven high or low, or mapped to a variety of DAC mute controls or ADC overflow indicators.

The CS42426 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

ORDERING INFORMATION

| | | |
|-------------|------------------|-------------|
| CS42426-CQ* | -10° to 70° C | 64-pin LQFP |
| CS42426-DQ* | -40° to 85° C | 64-pin LQFP |
| CDB42428 | Evaluation Board | |

*Also available in Lead-Free package



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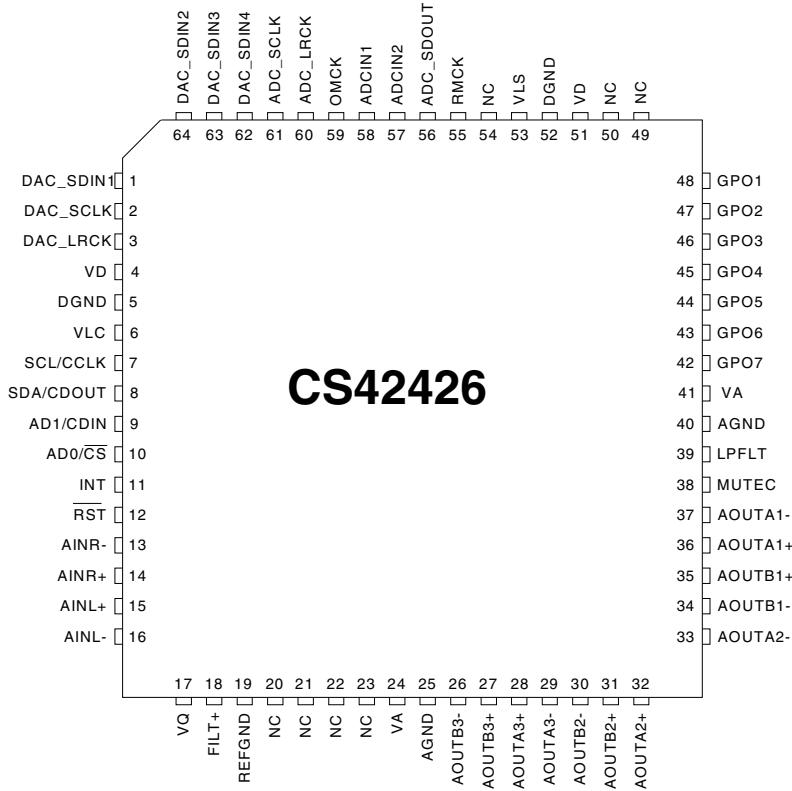
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1 PIN DESCRIPTIONS



| Pin Name | # | Pin Description |
|-------------------|----|--|
| DAC_SDIN1 | 1 | DAC Serial Audio Data Input (Input) - Input for two's complement serial audio data. |
| DAC_SDIN2 | 64 | |
| DAC_SDIN3 | 63 | |
| DAC_SCLK | 2 | DAC Serial Clock (Input/Output) - Serial clock for the DAC serial audio interface. |
| DAC_LRCK | 3 | DAC Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the DAC serial audio data line. |
| VD | 4 | Digital Power (Input) - Positive power supply for the digital section. |
| | 51 | |
| DGND | 5 | Digital Ground (Input) - Ground reference. Should be connected to digital ground. |
| | 52 | |
| VLC | 6 | Control Port Power (Input) - Determines the required signal level for the control port. |
| SCL/CCLK | 7 | Serial Control Port Clock (Input) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I ² C mode as shown in the Typical Connection Diagram. |
| SDA/CDDOUT | 8 | Serial Control Data (Input/Output) - SDA is a data I/O line in I ² C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDDOUT is the output data line for the control port interface in SPI mode. |
| AD1/CDIN | 9 | Address Bit 1 (I²C)/Serial Control Data (SPI) (Input) - AD1 is a chip address pin in I ² C mode; CDIN is the input data line for the control port interface in SPI mode. |
| AD0/CS | 10 | Address Bit 0 (I²C)/Control Port Chip Select (SPI) (Input) - AD0 is a chip address pin in I ² C mode; CS is the chip select signal in SPI mode. |

| | | |
|---|--|---|
| INT | 11 | Interrupt (Output) - The CS42426 will generate an interrupt condition as per the Interrupt Mask register. See "Interrupts" on page 28 for more details. |
| RST | 12 | Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when low. |
| AINR- AINR+ | 13 14 | Differential Right Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins. |
| AINL+ AINL- | 15 16 | Differential Left Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins. |
| VQ | 17 | Quiescent Voltage (Output) - Filter connection for internal quiescent reference voltage. |
| FILT+ | 18 | Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits. |
| REFGND | 19 | Reference Ground (Input) - Ground reference for the internal sampling circuits. |
| AOUTA1 +,- AOUTB1 +,- | 36,37 35,34 | Differential Analog Output (Output) - The full-scale differential analog output level is specified in the Analog Characteristics specification table. |
| AOUTA2 +,- | 32,33 | |
| AOUTB2 +,- | 31,30 | |
| AOUTA3 +,- | 28,29 | |
| AOUTB3 +,- | 27,26 | |
| VA | 24 41 | Analog Power (Input) - Positive power supply for the analog section. |
| AGND | 25 40 | Analog Ground (Input) - Ground reference. Should be connected to analog ground. |
| MUTEC | 38 | Mute Control (Output) - The Mute Control pin outputs high impedance following an initial power-on condition or whenever the PDN bit is set to a '1', forcing the codec into power-down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected "active" state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops. |
| LPFLT | 39 | PLL Loop Filter (Output) - An RC network should be connected between this pin and ground. |
| GPO7 GPO6 GPO5 GPO4 GPO3 GPO2 GPO1 | 42 43 44 45 46 47 48 | General Purpose Output (Output) - These pins can be configured as general purpose output pins, an ADC overflow interrupt or Mute Control outputs according to the General Purpose Pin Control registers. |
| VLS | 53 | Serial Port Interface Power (Input) - Determines the required signal level for the serial port interfaces. |
| RMCK | 55 | Recovered Master Clock (Output) - Recovered master clock output from the External Clock Reference (OMCK, pin 59) or the PLL which is locked to the incoming ADC_LRCK. |
| ADC_SDOUT | 56 | ADC Serial Data Output (Output) - Output for two's complement serial audio PCM data from the output of the internal and external ADCs. |
| ADCIN1 ADCIN2 | 58 57 | External ADC Serial Input (Input) - The CS42426 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42426 is placed in One Line mode. |
| OMCK | 59 | External Reference Clock (Input) - External clock reference that must be within the ranges specified in the register "OMCK Frequency (OMCK Freqx)" on page 38. |
| ADC_LRCK | 60 | ADC Left/Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the ADC serial audio data line. |
| ADC_SCLK | 61 | ADC Serial Clock (Input/Output) - Serial clock for the ADC serial audio interface. |

2 TYPICAL CONNECTION DIAGRAMS

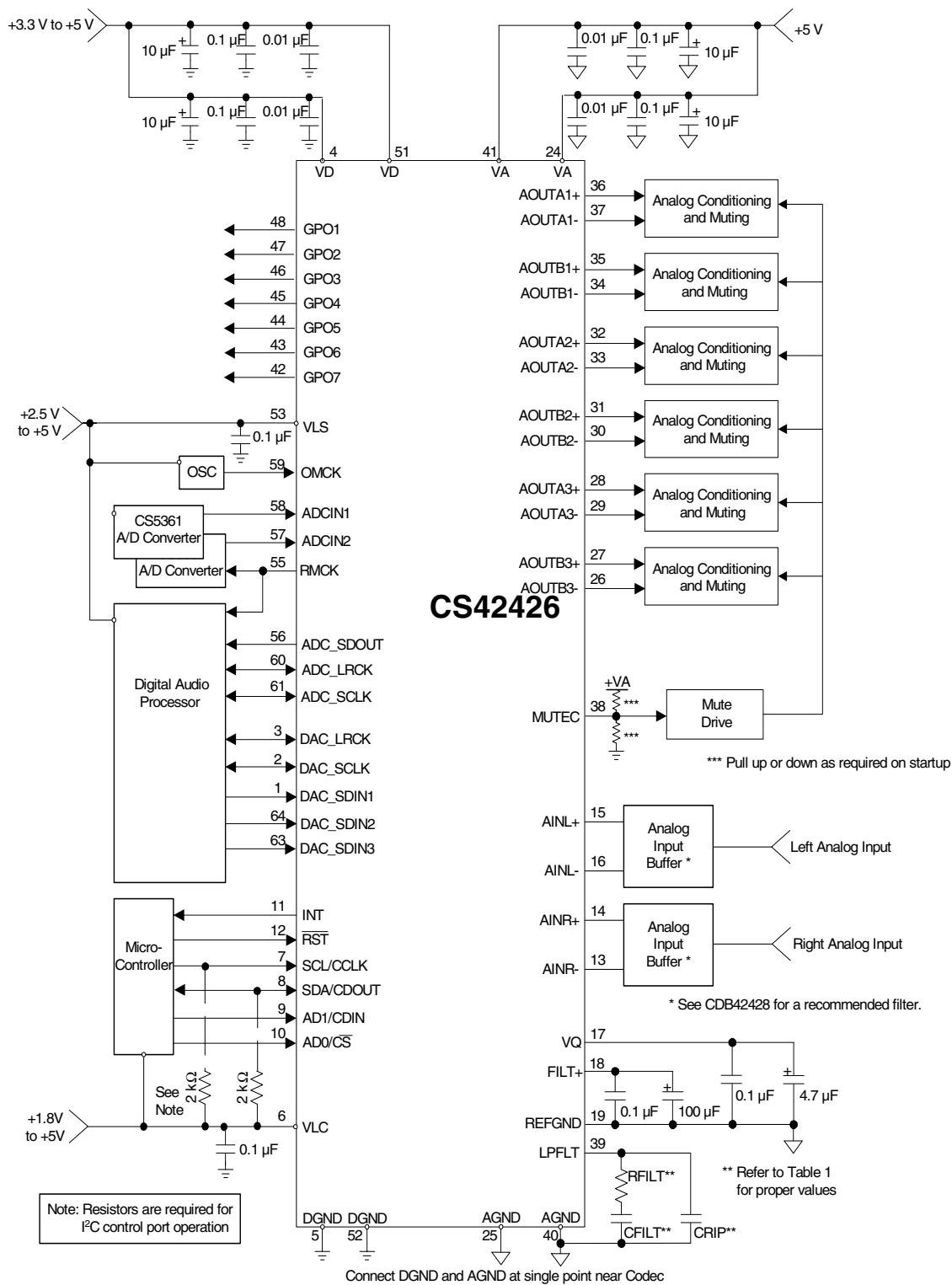


Figure 1. Typical Connection Diagram

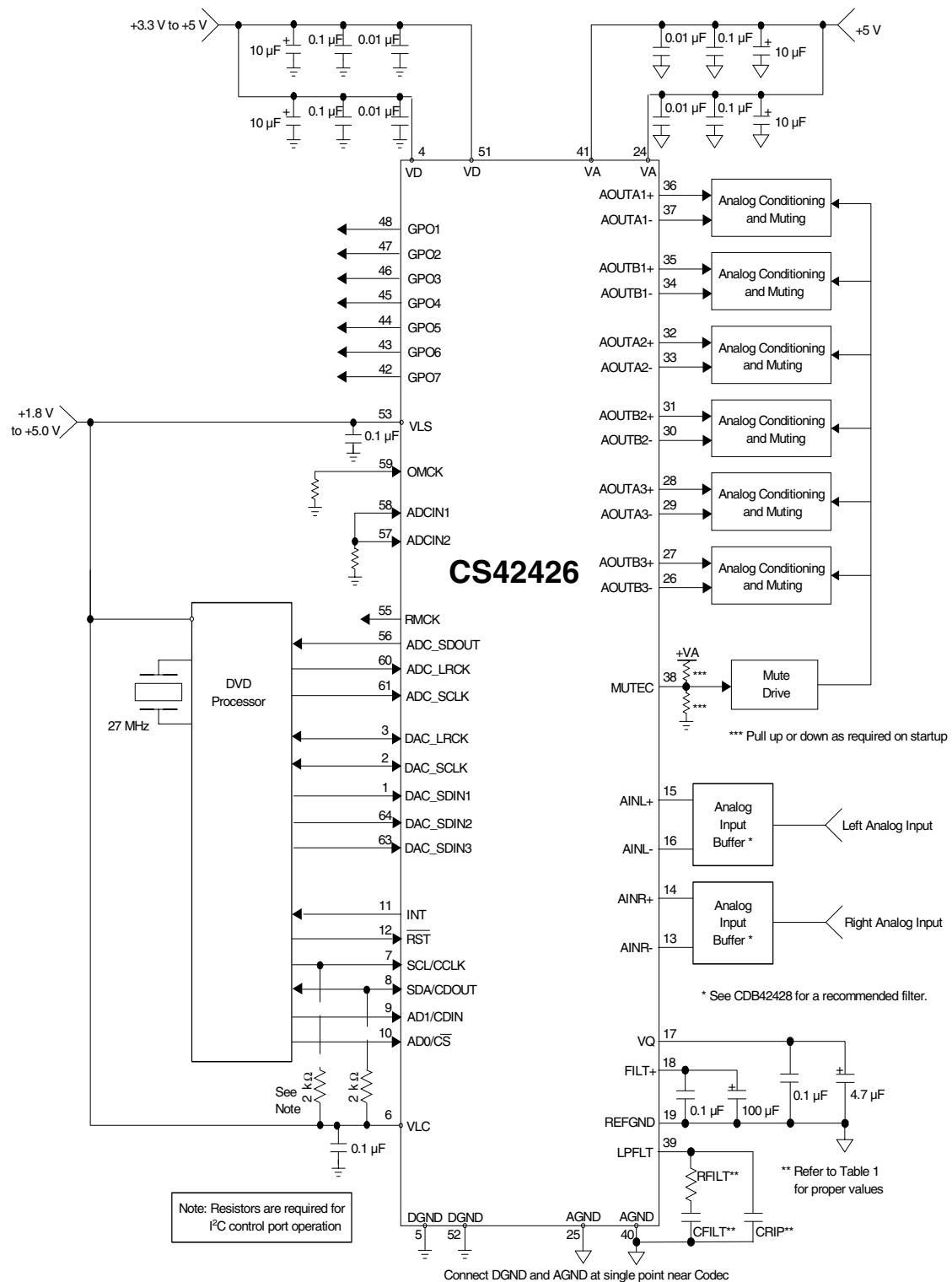


Figure 2. Typical Connection Diagram using the PLL

3 APPLICATIONS

3.1 Overview

The CS42426 is a highly integrated mixed signal 24-bit audio codec comprised of 2 analog-to-digital converters (ADC), implemented using multi-bit delta-sigma techniques, and 6 digital-to-analog converters (DAC). Other functions integrated within the codec include independent digital volume controls for each DAC, digital de-emphasis filters for DAC, digital gain control for ADC channels, ADC high-pass filters, and an on-chip voltage reference. All serial data is transmitted through one configurable serial audio interface for the ADC with enhanced one line modes of operation allowing up to 6 channels of serial audio data on one data line. All functions are configured through a serial control port operable in SPI mode or in I²C mode. Figure 1 shows the recommended connections for the CS42426.

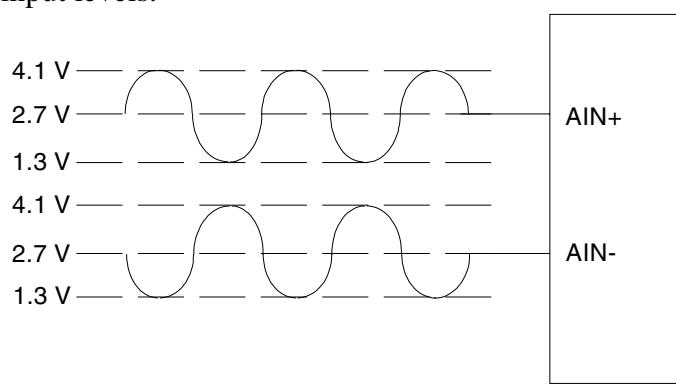
The CS42426 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the FM bits in register “Functional Mode (address 03h)” on page 33. Single-Speed mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed mode (QSM) supports input sample rates up to 192 kHz and uses an oversampling ratio of 32x.

Using the integrated PLL, a low jitter clock is recovered from the ADC LRCK input signal. The recovered clock or an externally supplied clock attached to the OMCK pin can be used as the System Clock.

3.2 Analog Inputs

3.2.1 Line Level Inputs

AINR+, AINR-, AINL+, and AINL- are the line level differential analog inputs. These pins are internally biased to the DC quiescent reference voltage, VQ, of approximately 2.7 V. The level of the signal can be adjusted for the left and right ADC independently through the ADC Left and Right Channel Gain Control Registers on page 45. The ADC output data is in 2's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFFH or 800000H, respectively and cause the ADC Overflow bit in the register “Interrupt Status (address 20h) (Read Only)” on page 46 to be set to a ‘1’. The GPO pins may also be configured to indicate an overflow condition has occurred in the ADC. See “General Purpose Pin Control (addresses 29h to 2Fh)” on page 48 for proper configuration. Figure 3 shows the full-scale analog input levels.



Full-Scale Input Level= (AIN+) - (AIN-)= 5.6 Vpp

Figure 3. Full-Scale Analog Input

3.2.2 *External Input Filter*

The analog modulator samples the input at 6.144 MHz (internal MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are $(n \times 6.144 \text{ MHz})$ the digital passband frequency, where $n=0,1,2,\dots$ Refer to the CDB42418 for a recommended analog input buffer that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

3.2.3 *High Pass Filter and DC Offset Calibration*

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. The high pass filter can be independently enabled and disabled. If the HPF_Freeze bit is set during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

- 1) Running the CS42426 with the high pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
- 2) Disabling the high pass filter and freezing the stored DC offset.

The high pass filters are controlled using the HPF_FREEZE bit in the register “Misc Control (address 05h)” on page 36.

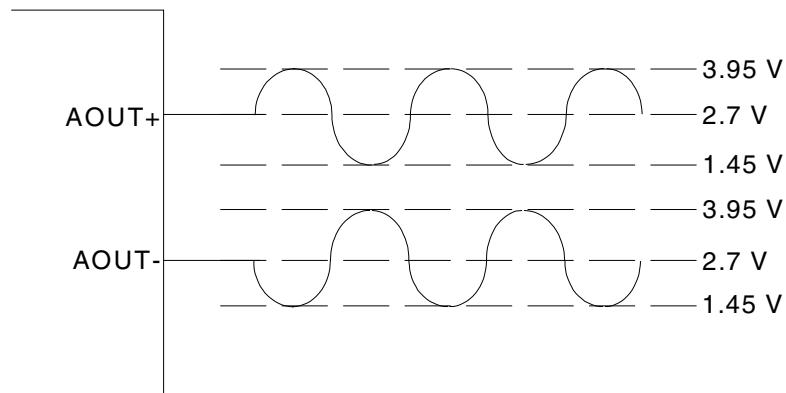
3.3 Analog Outputs

3.3.1 *Line Level Outputs and Filtering*

The CS42426 contains on-chip buffer amplifiers capable of producing line level differential outputs. These amplifiers are biased to a quiescent DC level of approximately VQ.

The delta-sigma conversion process produces high frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low pass filter. The recommended output filter configuration is shown in the CDB42418. This filter configuration accounts for the normally differing AC loads on the AOUT+ and AOUT- differential output pins. It also shows an AC coupling configuration which minimizes the number of required AC coupling capacitors.

The CS42426 is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry. Figure 4 shows the full-scale analog output levels.



Full-Scale Output Level= (AIN+) - (AIN-)= 5 Vpp

Figure 4. Full-Scale Output

3.3.2 *Interpolation Filter*

To accommodate the increasingly complex requirements of digital audio systems, the CS42426 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single, Double, and Quad Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit found in the register “Misc Control (address 05h)” on page 36 is used to select which filter is used. Filter response plots can be found in Figures 32 to 55.

3.3.3 *Digital Volume and Mute Control*

Each DAC’s output level is controlled via the Volume Control registers operating over the range of 0 to -127 dB attenuation with 0.5 dB resolution. See “Volume Control (addresses 0Fh, 10h, 11h, 12h, 13h, 14h)” on page 42. Volume control changes are programmable to ramp in increments of 0.125 dB at the rate controlled by the SZC[1:0] bits in the Digital Volume Control register. See “Volume Control (address 0Dh)” on page 40.

Each output can be independently muted via mute control bits in the register “Channel Mute (address 0Eh)” on page 41. When enabled, each XX_MUTE bit attenuates the corresponding DAC to its maximum value (-127 dB). When the XX_MUTE bit is disabled, the corresponding DAC returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZC[1:0] bits.

The Mute Control pin, MUTEC, is typically connected to an external mute control circuit. The Mute Control pin is tri-stated during power up or in power down mode by setting the PDN bit in the register “Power Control (address 02h)” on page 33 to a ‘1’. Once out of power-down mode the pin can be controlled by the user via the control port, or automatically asserted high when zero data is present on all DAC inputs, or when serial port clock errors are present. To prevent large transients on the output, it is desirable to mute the DAC outputs before the Mute Control pin is asserted. Please see the MUTEC pin in the Pin Descriptions section for more information.

Each of the GPO1-GPO7 can be programmed to provide a hardware MUTE signal to individual circuits. Each pin can be programmed as an output, with specific muting capabilities as defined by the function bits in the register “General Purpose Pin Control (addresses 29h to 2Fh)” on page 48.

3.3.4 ATAPI Specification

The CS42426 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 15 on page 44 and Figure 5 for additional information.

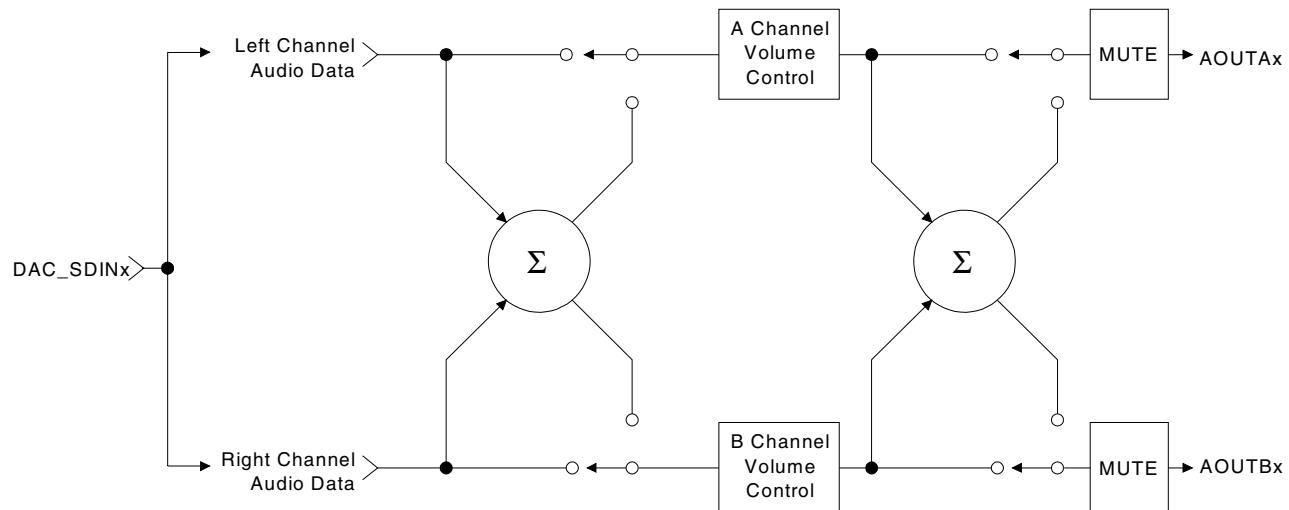


Figure 5. ATAPI Block Diagram (x = channel pair 1, 2, 3)

3.4 Clock Generation

The clock generation for the CS42426 is shown in the figure below. The internal MCLK is derived from the output of the PLL or a master clock source attached to OMCK. The mux selection is controlled by the SW_CTRLx bits and can be configured to manual switch mode only, or automatically switch on loss of PLL lock to the other source input.

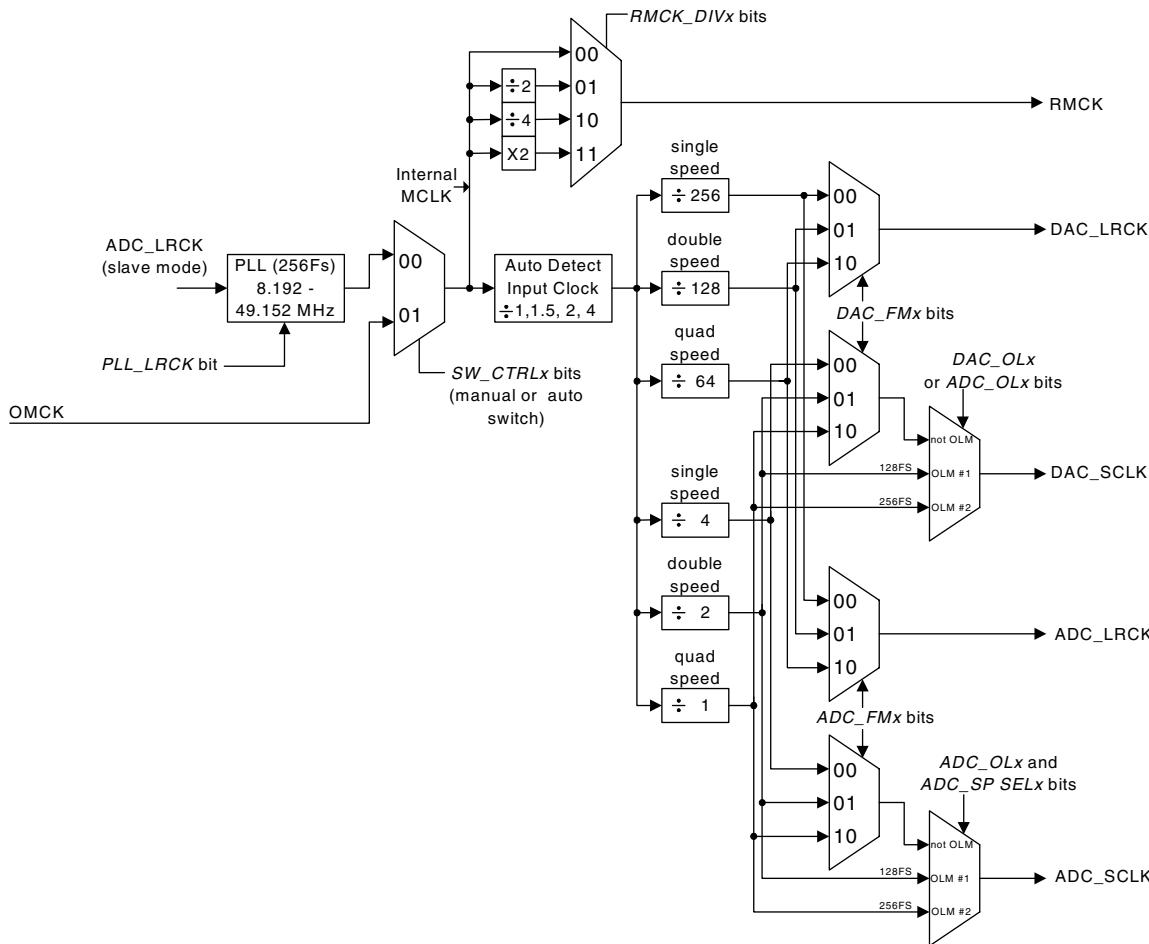


Figure 6. Clock Generation

3.4.1 PLL and Jitter Attenuation

The PLL can be configured to lock onto the incoming ADC_LRCK signal from the ADC Serial Port and generate the required internal master clock frequency. There are some applications where low jitter in the recovered clock, presented on the RMCK pin, is important. For this reason, the PLL has been designed to have good jitter attenuation characteristics. By setting the PLL_LRCK bit to a ‘1’ in the register “Clock Control (address 06h)” on page 37, the PLL will lock to the incoming ADC_LRCK and generate an output master clock (RMCK) of 256Fs. Table 3 below shows the output of the PLL with typical input Fs values for ADC_LRCK.

The PLL behavior is affected by the external filter component values. Figure 1 shows the required configuration of the external filter components. The set of component values required for 32 kHz to 192 kHz

sample rate applications are shown in Table 1. The lock time is the worst case for an F_s transition from unlocked state to locking to 192 kHz.

| Fs Range (kHz) | RFILT (kΩ) | CFILT (pF) | CRIP (pF) | Settling time |
|----------------|------------|------------|-----------|---------------|
| 32 to 192 | 10 | 2700 | 680 | 11 ms |

Table 1. PLL External Component Values

It is important to treat the LPFLT pin as a low level analog input. It is suggested that the ground end of the PLL filter be returned directly to the AGND pin independently of the digital ground plane.

3.4.2 OMCK System Clock Mode

A special clock switching mode is available that allows the clock that is input through the OMCK pin to be used as the internal master clock. This feature is controlled by the SW_CTRLx bits in register “Clock Control (address 06h)” on page 37. An advanced auto switching mode is also implemented to maintain master clock functionality. The clock auto switching mode allows the clock input through OMCK to be used as a clock in the system without any disruption when the PLL loses lock, for example, when the LRCK is removed from ADC_LRCK. This clock switching is done glitch free.

3.4.3 Master Mode

In master mode, the serial interface timings are derived from an external clock attached to OMCK or the output of the PLL with an input reference to the ADC_LRCK input from the ADC serial port. The DAC Serial Port and ADC Serial Port can both be masters only when OMCK is used as the clock source. When using the PLL output, the ADC Serial Port must be slave and the DAC Serial Port can operate in Master Mode. Master clock selection and operation is configured with the SW_CTRL1:0 and CLK_SEL bits in the Clock Control Register (See “Clock Control (address 06h)” on page 37).

The sample rate to OMCK ratios and OMCK frequency requirements for Master mode operation are shown in Table 2.

| Sample Rate (kHz) | OMCK (MHz) | | | | | | | | |
|-------------------|----------------------------|---------|---------|------------------------------|---------|---------|-----------------------------|---------|---------|
| | Single Speed (4 to 50 kHz) | | | Double Speed (50 to 100 kHz) | | | Quad Speed (100 to 192 kHz) | | |
| | 256x | 384x | 512x | 128x | 192x | 256x | 64x | 96x | 128x |
| 48 | 12.2880 | 18.4320 | 24.5760 | - | - | - | - | - | - |
| 96 | - | - | - | 12.2880 | 18.4320 | 24.5760 | - | - | - |
| 192 | - | - | - | - | - | - | 12.2880 | 18.4320 | 24.5760 |

Table 2. Common OMCK Clock Frequencies

3.4.4 Slave Mode

In Slave mode, DAC_LRCK, DAC_SCLK and/or ADC_LRCK and ADC_SCLK operate as inputs. The Left/Right clock signal must be equal to the sample rate, F_s and must be synchronously derived from the supplied master clock, OMCK or must be synchronous to the supplied ADC_LRCK used as the input to

the PLL. In this latter scenario the PLL output becomes the internal master clock. The supported PLL output frequencies are shown in Table 3 below.

| Sample Rate (kHz) | PLL Output (MHz) | | |
|-------------------|----------------------------|------------------------------|-----------------------------|
| | Single Speed (4 to 50 kHz) | Double Speed (50 to 100 kHz) | Quad Speed (100 to 192 kHz) |
| | 256x | 256x | 256x |
| 32 | 8.1920 | - | - |
| 44.1 | 11.2896 | - | - |
| 48 | 12.2880 | - | - |
| 64 | - | 16.3840 | - |
| 88.2 | - | 22.5792 | - |
| 96 | - | 24.5760 | - |
| 176.4 | - | - | 45.1584 |
| 192 | - | - | 49.1520 |

Table 3. Common PLL Output Clock Frequencies

The serial bit clock, DAC_SCLK and/or ADC_SCLK, must be synchronous to the corresponding DAC_LRCK/ADC_LRCK and be equal to 128x, 64x, 48x or 32x Fs depending on the interface format selected and desired speed mode. One Line Mode #1 is supported in Slave Mode. One Line Mode #2 is not supported. Refer to Table 4 for required clock ratios.

| | Single Speed | Double Speed | Quad Speed | One Line Mode #1 |
|-----------------|---------------------|--------------|------------|------------------|
| OMCK/LRCK Ratio | 256x, 512x | 128x, 256x | 128x | 256x |
| SCLK/LRCK Ratio | 32x, 48x, 64x, 128x | 32x, 64x | 32x, 64x | 128x |

Table 4. Slave Mode Clock Ratios

3.5 Digital Interfaces

3.5.1 Serial Audio Interface Signals

The CS42426 interfaces to an external Digital Audio Processor via two independent serial ports, the DAC serial port, DAC_SP and the ADC serial port, ADC_SP. The digital output of the internal ADCs use the ADC_SDOOUT pin and can be configured to use either the ADC or DAC serial port timings. These configuration bits and the selection of Single, Double or Quad Speed mode for DAC_SP and ADC_SP are found in register “Functional Mode (address 03h)” on page 33.

The serial interface clocks, ADC_SCLK for ADC_SP and DAC_SCLK for DAC_SP, are used for transmitting and receiving audio data. Either ADC_SCLK or DAC_SCLK can be generated by the CS42426 (master mode) or it can be input from an external source (slave mode). Master or Slave mode selection is made using bits DAC_SP M/S and ADC_SP M/S in register “Misc Control (address 05h)” on page 36.

The Left/Right clock (ADC_LRCK or DAC_LRCK) is used to indicate left and right data frames and the start of a new sample period. It may be an output of the CS42426 (master mode), or it may be generated by an external source (slave mode). As described in later sections, particular modes of operation do allow the sample rate, Fs, of the ADC_SP and the DAC_SP to be different, but must be multiples of each other.

The serial data interface format selection (left/right justified, I²S or one line mode) for the ADC serial port data out pin, ADC_SDOOUT, and the DAC input pins, DAC_SDIN1:3, is configured using the appropriate

bits in the register “Interface Formats (address 04h)” on page 34. The serial audio data is presented in 2’s complement binary form with the MSB first in all formats.

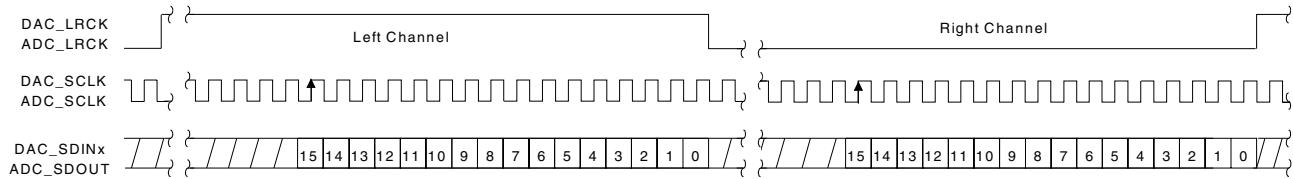
DAC_SDIN1, DAC_SDIN2, and DAC_SDIN3 are the serial data input pins supplying the internal DAC. ADC_SDOUT, the ADC data output pin, carries data from the two internal 24-bit ADCs and, when configured for one-line mode, up to four additional ADC channels attached externally to the signals ADCIN1 and ADCIN2 (typically two CS5361 stereo ADCs). When operated in One Line Data Mode, 6 channels of DAC data are input on DAC_SDIN1 and 6 channels of ADC data are output on ADC_SDOUT. Table 5 outlines the serial port channel allocations.

| Serial Inputs / Outputs | | |
|-------------------------|---------------|--------------------------|
| DAC_SDIN1 | left channel | DAC #1 |
| | right channel | DAC #2 |
| | one line mode | DAC channels 1,2,3,4,5,6 |
| DAC_SDIN2 | left channel | DAC #3 |
| | right channel | DAC #4 |
| | one line mode | not used |
| DAC_SDIN3 | left channel | DAC #5 |
| | right channel | DAC #6 |
| | one line mode | not used |
| ADC_SDOUT | left channel | ADC #1 |
| | right channel | ADC #2 |
| | one line mode | ADC channels 1,2,3,4,5,6 |
| ADCIN1 | left channel | External ADC #3 |
| | right channel | External ADC #4 |
| ADCIN2 | left channel | External ADC #5 |
| | right channel | External ADC #6 |

Table 5. Serial Audio Port Channel Allocations

3.5.2 Serial Audio Interface Formats

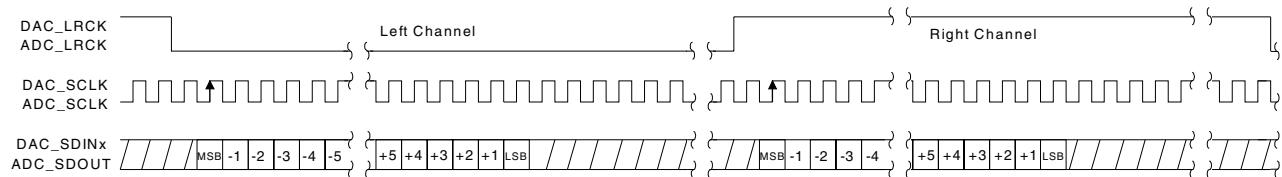
The DAC_SP and ADC_SP digital audio serial ports support 5 formats with varying bit depths from 16 to 24 as shown in Figure 7, Figure 8, Figure 9, Figure 10 and Figure 11. These formats are selected using the configuration bits in the registers, “Functional Mode (address 03h)” on page 33 and “Interface Formats (address 04h)” on page 34. For the diagrams below, single-speed mode is equivalent to $F_s = 32, 44.1, 48\text{kHz}$; double-speed mode is for $F_s = 64, 88.2, 96\text{ kHz}$; and quad-speed mode is for $F_s = 176.4, 196\text{ kHz}$.



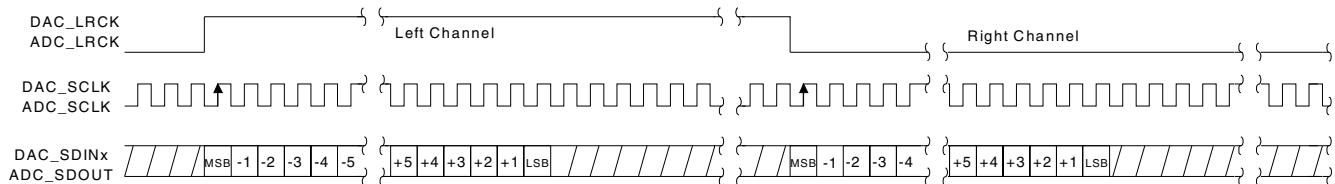
Right Justified Mode, Data Valid on Rising Edge of SCLK

| Bits/Sample | SCLK Rate(s) | | Notes |
|-------------|--------------------|-------------------|-------------------|
| | Master | Slave | |
| 16 | 64 F_s | 48, 64, 128 F_s | single-speed mode |
| | 64 F_s | 64 F_s | double-speed mode |
| | 64 F_s | 64 F_s | quad-speed mode |
| 24 | 64, 128, 256 F_s | 64, 128 F_s | single-speed mode |
| | 64 F_s | 64 F_s | double-speed mode |
| | 64 F_s | 64 F_s | quad-speed mode |

Figure 7. Right Justified Serial Audio Formats

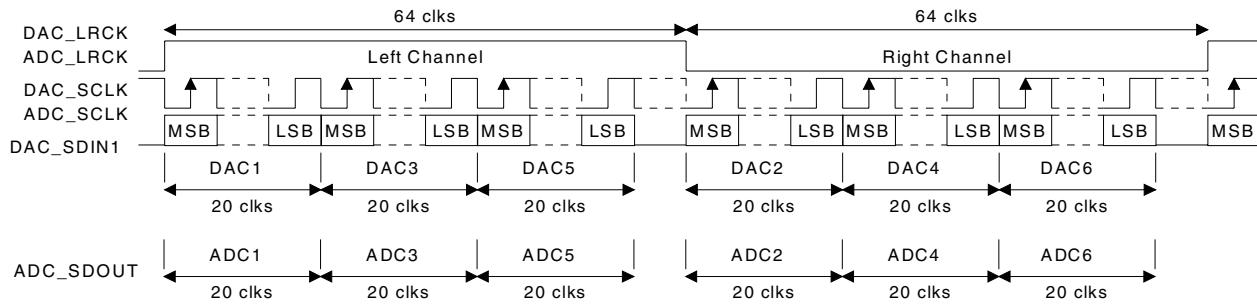

I2S Mode, Data Valid on Rising Edge of SCLK

| Bits/Sample | SCLK Rate(s) | | Notes |
|-------------|-----------------|----------------|-------------------|
| | Master | Slave | |
| 16 | 64 Fs | 48, 64, 128 Fs | single-speed mode |
| | 64 Fs | 64 Fs | double-speed mode |
| | 64 Fs | 64 Fs | quad-speed mode |
| 18 to 24 | 64, 128, 256 Fs | 48, 64, 128 Fs | single-speed mode |
| | 64 Fs | 64 Fs | double-speed mode |
| | 64 Fs | 64 Fs | quad-speed mode |

Figure 8. I²S Serial Audio Formats

Left Justified Mode, Data Valid on Rising Edge of SCLK

| Bits/Sample | SCLK Rate(s) | | Notes |
|-------------|-----------------|--------------------|-------------------|
| | Master | Slave | |
| 16 | 64 Fs | 32, 48, 64, 128 Fs | single-speed mode |
| | 64 Fs | 32, 64 Fs | double-speed mode |
| | 64 Fs | 32, 64 Fs | quad-speed mode |
| 18 to 24 | 64, 128, 256 Fs | 48, 64, 128 Fs | single-speed mode |
| | 64 Fs | 64 Fs | double-speed mode |
| | 64 Fs | 64 Fs | quad-speed mode |

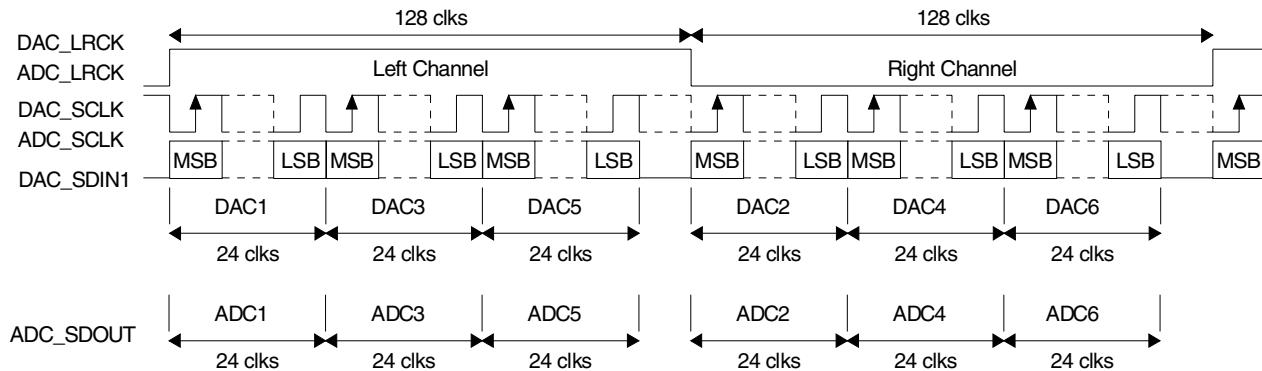
Figure 9. Left Justified Serial Audio Formats



One Line Data Mode #1, Data Valid on Rising Edge of SCLK

| Bits/Sample | SCLK Rate(s) | | Notes |
|-------------|--------------|--------|-------------------|
| | Master | Slave | |
| 20 | 128 Fs | 128 Fs | single-speed mode |
| | 128 Fs | 128Fs | double-speed mode |

Figure 10. One Line Mode #1 Serial Audio Format



One Line Data Mode #2, Data Valid on Rising Edge of SCLK

| Bits/Sample | SCLK Rate(s) | | Notes |
|-------------|--------------|---------------|-------------------|
| | Master | Slave | |
| 24 | 256 Fs | not supported | single-speed mode |

Figure 11. One Line Mode #2 Serial Audio Format

3.5.3 ADCIN1/ADCIN2 Serial Data Format

The two serial data lines which interface to the optional external ADCs, ADCIN1 and ADCIN2, support only left-justified, 24-bit samples at 64Fs or 128Fs. This interface is not affected by any of the serial port configuration register bit settings. These serial data lines are used when supporting One Line Mode of operation with external ADCs attached. If these signals are not being used, they should be tied together and wired to GND via a pull-down resistor.

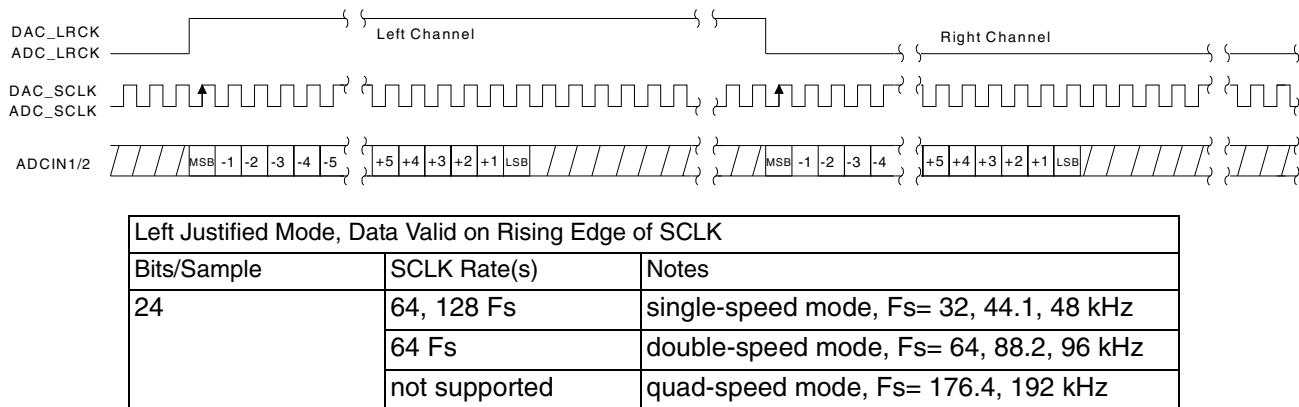


Figure 12. ADCIN1/ADCIN2 Serial Audio Format

For proper operation, the CS42426 must be configured to select which SCLK/LRCK is being used to clock the external ADCs. The EXT ADC SCLK bit in register “Misc Control (address 05h)” on page 36, must be set accordingly. Set this bit to ‘1’ if the external ADCs are wired using the DAC_SP clocks. If the ADCs are wired to use the ADC_SP clocks, set this bit to ‘0’.

3.5.4 One Line Mode(OLM) Configurations

3.5.4.1 OLM Config #1

One Line Mode Configuration #1 can support up to 6 channels of DAC data, and 6 channels of ADC data. This is the only configuration which will support up to 24-bit samples at a sampling frequency of 48 kHz on all channels for both the DAC and ADC.

| Register / Bit Settings | Description |
|---|--|
| <i>Functional Mode Register (addr = 03h)</i> | |
| <i>Set DAC_FMx = ADC_FMx = 00,01,10</i> | DAC_LRCK must equal ADC_LRCK; sample rate conversion not supported |
| <i>Set ADC_CLK_SEL = 0</i> | Configure ADC_SDOUT to be clocked from the DAC_SP clocks. |
| <i>Interface Format Register (addr = 04h)</i> | |
| <i>Set DIFx bits to proper serial format</i> | Select the digital interface format when not in one line mode |
| <i>Set ADC_Olx bits = 00,01,10</i> | Select ADC operating mode, see table below for valid combinations |
| <i>Set DAC_Olx bits = 00,01,10</i> | Select DAC operating mode, see table below for valid combinations |
| <i>Misc. Control Register (addr = 05h)</i> | |
| <i>Set DAC_SP M/S = 1</i> | Configure DAC Serial Port to master mode. |
| <i>Set ADC_SP M/S = 1</i> | Configure ADC Serial Port to master mode. |
| <i>Set EXT ADC SCLK = 0</i> | Identify external ADC clock source as ADC Serial Port. |

| | | DAC Mode | | |
|----------|-------------------|--|--|--|
| | | Not One Line Mode | One Line Mode #1 | One Line Mode #2 |
| ADC Mode | Not One Line Mode | DAC_SCLK=64Fs DAC_LRCK=SSM/DSM/QSM | DAC_SCLK=128Fs DAC_LRCK=SSM/DSM ADC_SCLK=64Fs ADC_LRCK=DAC_LRCK | not valid |
| | One Line Mode #1 | DAC_SCLK=128Fs DAC_LRCK=SSM/DSM ADC_SCLK=64Fs ADC_LRCK=DAC_LRCK | DAC_SCLK=128Fs DAC_LRCK=SSM/DSM ADC_SCLK=64Fs ADC_LRCK=DAC_LRCK | not valid |
| | One Line Mode #2 | DAC_SCLK=256Fs DAC_LRCK=SSM ADC_SCLK=64Fs ADC_LRCK=DAC_LRCK | not valid | DAC_SCLK=256Fs DAC_LRCK=SSM ADC_SCLK=64Fs ADC_LRCK=DAC_LRCK |

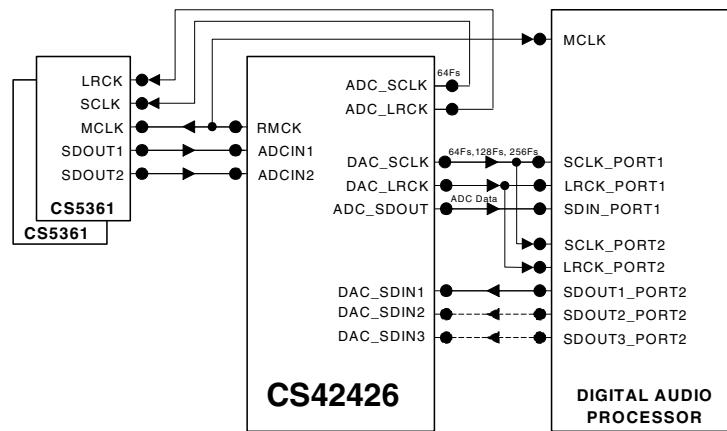


Figure 13. OLM Configuration #1

3.5.4.2 OLM Config #2

This configuration will support up to 6 channels of DAC data, 6 channels of ADC data and will handle up to 20-bit samples at a sampling frequency of 96 kHz on all channels for both the DAC and ADC. The output data stream of the internal and external ADCs is configured to use the ADC_SDOOUT output and run at the DAC Serial Port sample frequency.

| Register / Bit Settings | Description |
|---|---|
| <i>Functional Mode Register (addr = 03h)</i> | |
| <i>Set DAC_FMx = 00,01,10</i> | DAC_LRCK can run at SSM, DSM or QSM independent of ADC_LRCK |
| <i>Set ADC_FMx = 00,01,10</i> | ADC_LRCK can run at SSM, DSM or QSM independent of DAC_LRCK |
| <i>Set ADC_CLK_SEL = 1</i> | Configure ADC_SDOOUT to be clocked from the ADC_SP clocks. |
| <i>Interface Format Register (addr = 04h)</i> | |
| <i>Set DIFx bits to proper serial format</i> | Select the digital interface format when not in one line mode |
| <i>Set ADC_Olx bits = 00,01,10</i> | Select ADC operating mode, see table below for valid combinations |
| <i>Set DAC_Olx bits = 00,01</i> | Select DAC operating mode, see table below for valid combinations |
| <i>Misc. Control Register (addr = 05h)</i> | |
| <i>Set CODEC_SP M/S = 1</i> | Set CODEC Serial Port to master mode. |
| <i>Set SAI_SP M/S = 1</i> | Set Serial Audio Interface Port to master mode. |
| <i>Set EXT ADC SCLK = 1</i> | Identify external ADC clock source as DAC Serial Port. |

| | | DAC Mode | | |
|----------|-------------------|--|---|------------------|
| | | Not One Line Mode | One Line Mode #1 | One Line Mode #2 |
| ADC Mode | Not One Line Mode | DAC_SCLK=64Fs DAC_LRCK=SSM/DSM/QSM ADC_SCLK=64Fs ADC_LRCK=SSM/DSM/QSM | DAC_SCLK=128Fs DAC_LRCK=SSM ADC_SCLK=64Fs ADC_LRCK=SSM/DSM/QSM | not valid |
| | One Line Mode #1 | DAC_SCLK=64Fs DAC_LRCK=SSM/DSM ADC_SCLK=128Fs ADC_LRCK=CX_LRCK | DAC_SCLK=128Fs DAC_LRCK=SSM ADC_SCLK=128Fs ADC_LRCK=CX_LRCK | not valid |
| | One Line Mode #2 | DAC_SCLK=64Fs DAC_LRCK=SSM ADC_SCLK=256Fs ADC_LRCK=CX_LRCK | not valid | not valid |

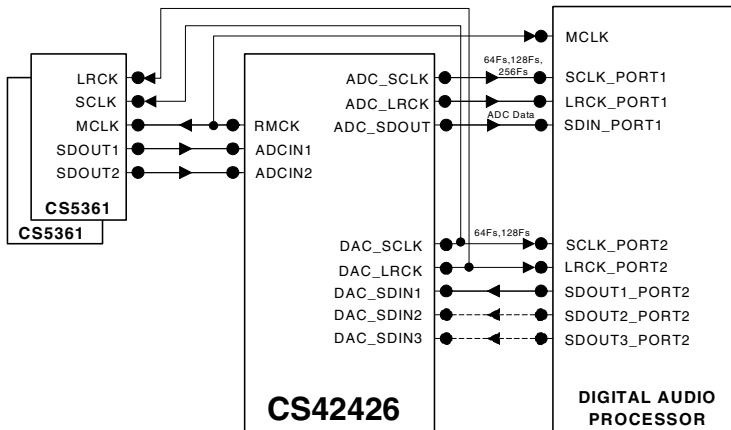


Figure 14. OLM Configuration #2

3.5.4.3 OLM Config #3

This configuration will support up to 6 channels of DAC data, and 6 channels of ADC data. OLM Config #3 will handle up to 20-bit ADC samples at an Fs of 48 kHz and 24-bit DAC samples at an Fs of 48 kHz. Since the ADCs data stream is configured to use the ADC_SDOUT output and the internal and external ADCs are clocked from the ADC_SP, then the sample rate for the DAC Serial Port can be different from the sample rate of the ADC serial port.

| Register / Bit Settings | Description |
|---|---|
| Functional Mode Register (addr = 03h) | |
| Set DAC_FMx = 00,01,10 | DAC_LRCK can run at SSM, DSM, or QSM independent of ADC_LRCK |
| Set ADC_FMx = 00,01,10 | ADC_LRCK can run at SSM, DSM, or QSM independent of DAC_LRCK |
| Set ADC_CLK_SEL = 1 | Configure ADC_SDOUT to be clocked from the ADC_SP clocks. |
| Interface Format Register (addr = 04h) | |
| Set DIFx bits to proper serial format | Select the digital interface format when not in one line mode |
| Set ADC_OLx bits = 00,01 | Select ADC operating mode, see table below for valid combinations |
| Set DAC_OLx bits = 00,01,10 | Select DAC operating mode, see table below for valid combinations |
| Misc. Control Register (addr = 05h) | |
| Set DAC_SP M/S = 1 | Set DAC Serial Port to master mode. |
| Set ADC_SP M/S = 0 or 1 | Set ADC Serial Port to master mode or slave mode. |
| Set EXT ADC SCLK = 0 | Identify external ADC clock source as ADC Serial Port. |

| | | DAC Mode | | |
|----------|-------------------|--|---|---|
| | | Not One Line Mode | One Line Mode #1 | One Line Mode #2 |
| ADC Mode | Not One Line Mode | DAC_SCLK=64Fs DAC_LRCK=SSM/DSM/QSM ADC_SCLK=64Fs ADC_LRCK=SSM/DSM/QSM | DAC_SCLK=128Fs DAC_LRCK=SSM/DSM ADC_SCLK=64Fs ADC_LRCK=SSM/DSM/QSM | DAC_SCLK=256Fs DAC_LRCK=SSM ADC_SCLK=64Fs ADC_LRCK=SSM/DSM/QSM |
| | One Line Mode #1 | DAC_SCLK=64Fs DAC_LRCK=SSM/DSM/QSM ADC_SCLK=128Fs ADC_LRCK=SSM | DAC_SCLK=128Fs DAC_LRCK=SSM/DSM ADC_SCLK=128Fs ADC_LRCK=SSM | DAC_SCLK=256Fs DAC_LRCK=SSM ADC_SCLK=128Fs ADC_LRCK=SSM |
| | One Line Mode #2 | not valid | not valid | not valid |

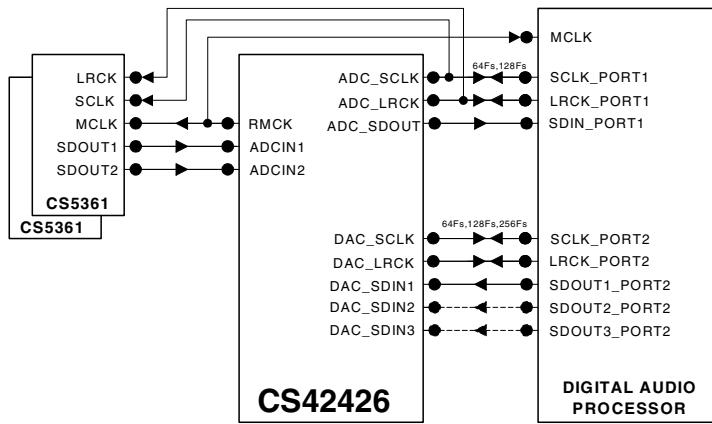


Figure 15. OLM Configuration #3

3.5.4.4 OLM Config #4

This One-Line Mode configuration can support up to 6 channels of DAC data on 2 DAC_SDIN pins, and 2 channels of ADC data and will handle up to 24-bit samples at a sampling frequency of 48 kHz on all channels for both the DAC and ADC. The output data stream of the internal ADCs can be configured to run at the DAC_SP clock speeds or to run at the ADC_SP rate. The DAC_SP and ADC_SP can operate at different Fs rates.

| Register / Bit Settings | Description |
|---|--|
| Functional Mode Register (addr = 03h) | |
| Set DAC_FMx = 00,01,10 | DAC_LRCK can run at SSM, DSM, or QSM independent of ADC_LRCK |
| Set ADC_FMx = 00,01,10 | ADC_LRCK can run at SSM, DSM, or QSM independent of DAC_LRCK |
| Set ADC_CLK_SEL = 0 or 1 | Configure ADC_SDOUT to be clocked from the ADC_SP or DAC_SP clocks. |
| Interface Format Register (addr = 04h) | |
| Set DIFx bits to proper serial format | Select the digital interface format when not in one line mode |
| Set ADC_Olx bits = 00 | Set ADC operating mode to Not One Line Mode since only 2 channels of ADC are supported |
| Set DAC_Olx bits = 00,01,10 | Select DAC operating mode, see table below for valid combinations |
| Misc. Control Register (addr = 05h) | |
| Set DAC_SP M/S = 0 or 1 | Set DAC Serial Port to master mode or slave mode. |
| Set ADC_SP M/S = 0 or 1 | Set ADC Serial Port to master mode or slave mode. |
| Set EXT ADC SCLK = 0 | External ADCs are not used. Leave bit in default state. |

| | | DAC Mode | | |
|----------|-------------------|--|---|---|
| | | Not One Line Mode | One Line Mode #1 | One Line Mode #2 |
| ADC Mode | Not One Line Mode | DAC_SCLK=64Fs/128Fs DAC_LRCK=SSM/DSM/QSM ADC_SCLK=64Fs/128Fs ADC_LRCK=SSM/DSM/QSM | DAC_SCLK=128Fs DAC_LRCK=SSM/DSM ADC_SCLK=64Fs/128Fs ADC_LRCK=SSM/DSM/QSM | DAC_SCLK=256Fs DAC_LRCK=SSM ADC_SCLK=64Fs/128Fs ADC_LRCK=SSM/DSM/QSM |
| | One Line Mode #1 | not valid | not valid | not valid |
| | One Line Mode #2 | not valid | not valid | not valid |

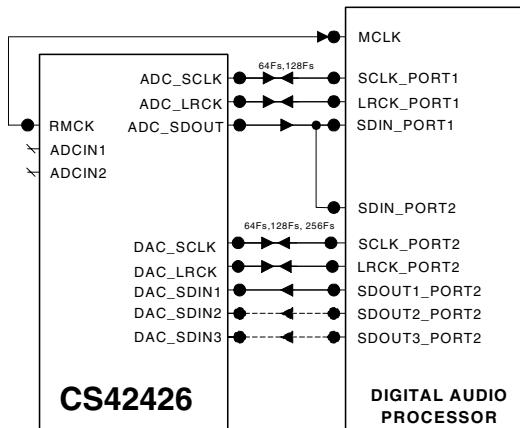


Figure 16. OLM Configuration #4

3.6 Control Port Description and Timing

The control port is used to access the registers, allowing the CS42426 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and I²C, with the CS42426 acting as a slave device. SPI mode is selected if there is a high to low transition on the AD0/CS pin, after the RST pin has been brought high. I²C mode is selected by connecting the AD0/CS pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

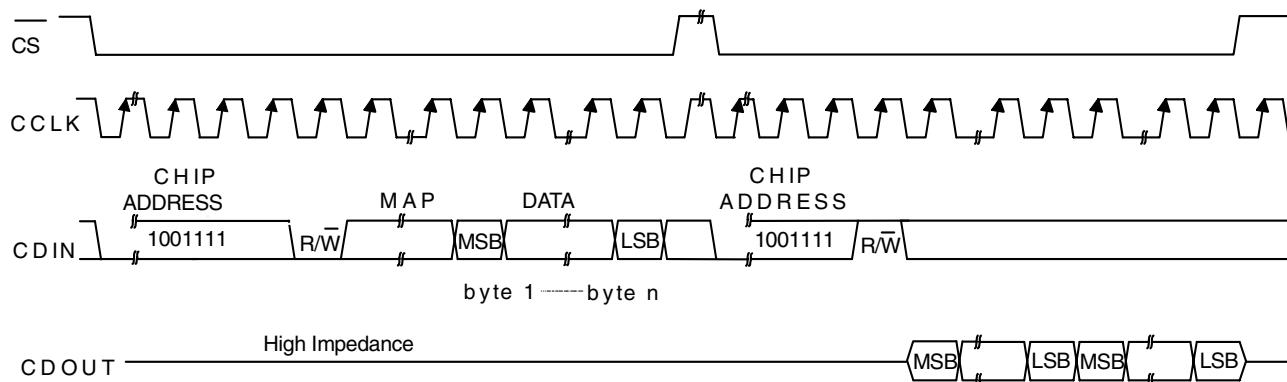
3.6.1 SPI Mode

In SPI mode, CS is the CS42426 chip select signal, CCLK is the control port bit clock (input into the CS42426 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 17 shows the operation of the control port in SPI mode. To write to a register, bring CS low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/W), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will autoincrement after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes (CS high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 17. Control Port Timing in SPI Mode

not, as desired. To begin a read, bring \overline{CS} low, send out the chip address and set the read/write bit (R/W) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

3.6.2 I^2C Mode

In I^2C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no \overline{CS} pin. Pins AD0 and AD1 form the two least significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS42426 is being reset.

The signal timings for a read and write cycle are shown in Figure 18 and Figure 19. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42426 after a Start condition consists of a 7 bit chip address field and a R/W bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS42426, the chip address field, which is the first byte sent to the CS42426, should match 10011 followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42426 after each input byte is read, and is input to the CS42426 from the microcontroller after each transmitted byte.

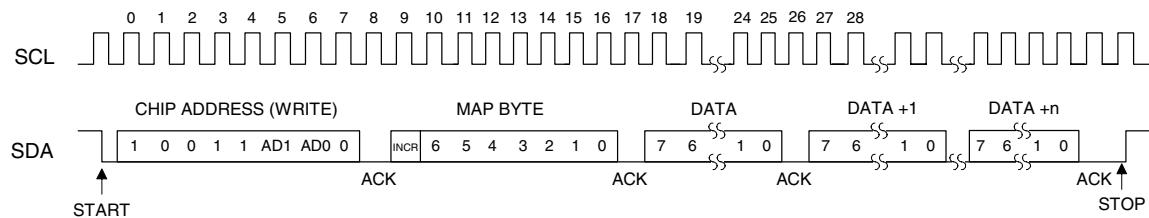


Figure 18. Control Port Timing, I^2C Slave Mode Write

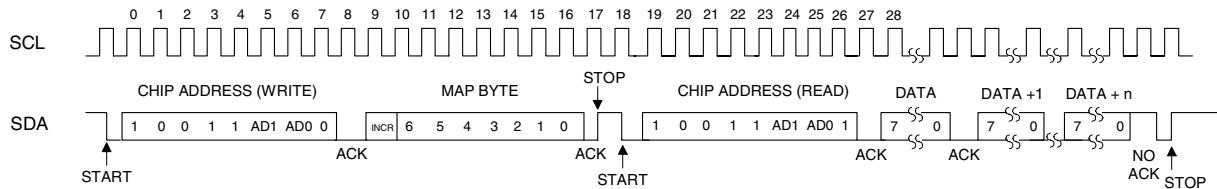


Figure 19. Control Port Timing, I^2C Slave Mode Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 19, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

```
Send start condition.  
Send 10011xx0 (chip address & write operation).  
Receive acknowledge bit.  
Send MAP byte, auto increment off.  
Receive acknowledge bit.  
Send stop condition, aborting write.  
Send start condition.  
Send 10011xx1(chip address & read operation).  
Receive acknowledge bit.  
Receive byte, contents of selected register.  
Send acknowledge bit.  
Send stop condition.
```

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

3.7 Interrupts

The CS42426 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be set to be active low, active high or active low with no active pull-up transistor. This last mode is used for active low, wired-OR hook-ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. See “Interrupt Status (address 20h) (Read Only)” on page 46. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

3.8 Reset and Power-up

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be activated if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

When $\overline{\text{RST}}$ is low, the CS42426 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. When $\overline{\text{RST}}$ is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 0 to the PDN bit in the Power Control Register will then cause the part to leave the low power state and begin operation. If the internal PLL is selected as the clock source, the serial audio outputs will be enabled after the PLL has settled. See “Power Control (address 02h)” on page 33 for more details.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the $\overline{\text{RST}}$ pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the FILT+ pin. A time delay of approximately 80ms is required after applying power to the device or after exiting a reset state. During this voltage reference ramp delay, all serial ports and DAC outputs will be automatically muted.

3.9 Power Supply, Grounding, and PCB layout

As with any high resolution converter, the CS42426 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA connected to clean supplies. VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

For applications where the output of the PLL is required to be low jitter, use a separate, low noise analog +5 V supply for VA, decoupled to AGND. In addition, a separate region of analog ground plane around the FILT+ , VQ, LPFLT, REFGND, AGND, and VA pins is recommended.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS42426 as possible. The low value ceramic capacitor should be the nearest to the pin and should be mounted on the same side of the board as the CS42426 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+ , VQ and LPFLT pins in order to avoid unwanted coupling into the modulators and PLL. The FILT+ and VQ decoupling capacitors, particularly the 0.1 μF , must be positioned to minimize the electrical path from FILT+ and REFGND. The CDB42418 evaluation board demonstrates the optimum layout and power supply arrangements.

4 REGISTER QUICK REFERENCE

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------------------------|-------------------|----------------|-----------------|-----------------|-----------------|------------------|-----------------|-----------------|
| 01h | ID default | Chip_ID3 1 | Chip_ID2 1 | Chip_ID1 1 | CHIP_ID0 0 | Rev_ID3 0 | Rev_ID2 0 | Rev_ID1 1 | Rev_ID0 1 |
| 02h | Power Control default | Reserved 0 | PDN_PLL 0 | PDN_ADC 0 | Reserved 0 | PDN_DAC3 0 | PDN_DAC2 0 | PDN_DAC1 0 | PDN 1 |
| 03h | Functional Mode default | DAC_FM1 0 | DAC_FM0 0 | ADC_FM1 0 | ADC_FM0 0 | Reserved 0 | ADC_CLK_SEL 0 | DAC DEM 0 | Reserved 0 |
| 04h | Interface Formats default | DIF1 0 | DIF0 1 | ADC_OL1 0 | ADC_OL0 0 | DAC_OL1 0 | DAC_OL0 0 | Reserved 0 | CODEC_RJ16 0 |
| 05h | Misc Control default | Ext ADC SCLK 0 | HiZ_RMCK 0 | Reserved 0 | FREEZE 0 | FILTSEL 0 | HPF_FREEZE 0 | DAC_SP M/S 1 | ADC_SP M/S 1 |
| 06h | Clock Control default | RMCK_DIV1 0 | RMCK_DIV0 0 | OMCK Freq1 0 | OMCK Freq0 0 | PLL_LRCK 0 | SW_CTRL1 0 | SW_CTRL0 1 | FRC_PLL_LK 0 |
| 07h | OMCK/PLL_CLK Ratio default | RATIO7 X | RATIO6 X | RATIO5 X | RATIO4 X | RATIO3 X | RATIO2 X | RATIO1 X | RATIO0 X |
| 08h | Clock Status default | Reserved X | Reserved X | Reserved X | Reserved X | Active_CLK X | PLL_CLK2 X | PLL_CLK1 X | PLL_CLK0 X |
| 09h-0Ch | Reserved default | Reserved X | Reserved X | Reserved X | Reserved X | Reserved X | Reserved X | Reserved X | Reserved X |
| 0Dh | Volume Control default | Reserved 0 | SNGVOL 0 | SZC1 0 | SZC0 0 | AMUTE 1 | Reserved 0 | RAMP_UP 0 | RAMP_DN 0 |
| 0Eh | Channel Mute default | Reserved 0 | Reserved 0 | B3_MUTE 0 | A3_MUTE 0 | B2_MUTE 0 | A2_MUTE 0 | B1_MUTE 0 | A1_MUTE 0 |
| 0Fh | Vol. Control A1 default | A1_VOL7 0 | A1_VOL6 0 | A1_VOL5 0 | A1_VOL4 0 | A1_VOL3 0 | A1_VOL2 0 | A1_VOL1 0 | A1_VOL0 0 |
| 10h | Vol. Control B1 default | B1_VOL7 0 | B1_VOL6 0 | B1_VOL5 0 | B1_VOL4 0 | B1_VOL3 0 | B1_VOL2 0 | B1_VOL1 0 | B1_VOL0 0 |
| 11h | Vol. Control A2 default | A2_VOL7 0 | A2_VOL6 0 | A2_VOL5 0 | A2_VOL4 0 | A2_VOL3 0 | A2_VOL2 0 | A2_VOL1 0 | A2_VOL0 0 |
| 12h | Vol. Control B2 default | B2_VOL7 0 | B2_VOL6 0 | B2_VOL5 0 | B2_VOL4 0 | B2_VOL3 0 | B2_VOL2 0 | B2_VOL1 0 | B2_VOL0 0 |
| 13h | Vol. Control A3 default | A3_VOL7 0 | A3_VOL6 0 | A3_VOL5 0 | A3_VOL4 0 | A3_VOL3 0 | A3_VOL2 0 | A3_VOL1 0 | A3_VOL0 0 |
| 14h | Vol. Control B3 default | B3_VOL7 0 | B3_VOL6 0 | B3_VOL5 0 | B3_VOL4 0 | B3_VOL3 0 | B3_VOL2 0 | B3_VOL1 0 | B3_VOL0 0 |
| 15h | Reserved default | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |
| 16h | Reserved default | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |
| 17h | Channel Invert default | Reserved 0 | Reserved 0 | INV_B3 0 | INV_A3 0 | INV_B2 0 | INV_A2 0 | INV_B1 0 | INV_A1 0 |
| 18h | Mixing Ctrl Pair 1 default | P1_A=B 0 | Reserved 0 | Reserved 0 | P1_ATAPI4 0 | P1_ATAPI3 1 | P1_ATAPI2 0 | P1_ATAPI1 0 | P1_ATAPI0 1 |

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------------|------------|------------|--------------|-------------|-------------|-------------|-------------|-------------|
| 19h | Mixing Ctrl Pair 2 default | P2_A=B 0 | Reserved 0 | Reserved 0 | P2_ATAPI4 0 | P2_ATAPI3 1 | P2_ATAPI2 0 | P2_ATAPI1 0 | P2_ATAPI0 1 |
| 1Ah | Mixing Ctrl Pair 3 default | P3_A=B 0 | Reserved 0 | Reserved 0 | P3_ATAPI4 0 | P3_ATAPI3 1 | P3_ATAPI2 0 | P3_ATAPI1 0 | P3_ATAPI0 1 |
| 1Bh | Reserved default | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 1 | Reserved 0 | Reserved 0 | Reserved 1 |
| 1Ch | ADC Left Ch. Gain default | Reserved 0 | Reserved 0 | LGAIN5 0 | LGAIN4 0 | LGAIN3 0 | LGAIN2 0 | LGAIN1 0 | LGAIN0 0 |
| 1Dh | ADC Right Ch. Gain default | Reserved 0 | Reserved 0 | RGAIN5 0 | RGAIN4 0 | RGAIN3 0 | RGAIN2 0 | RGAIN1 0 | RGAIN0 0 |
| 1Eh | Interrupt Control default | SP_SYNC 0 | Reserved 0 | DE-EMPH1 0 | DE-EMPH0 0 | INT1 0 | INT0 0 | Reserved 0 | Reserved 0 |
| 1Fh | Reserved default | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |
| 20h | Interrupt Status default | UNLOCK X | Reserved X | Reserved X | Reserved X | Reserved X | Reserved X | OverFlow X | Reserved X |
| 21h | Interrupt Mask default | UNLOCKM 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | OverFlowM 0 | Reserved 0 |
| 22h | Interrupt Mode MSB default | UNLOCK1 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | OF1 0 | Reserved 0 |
| 23h | Interrupt Mode LSB default | UNLOCK0 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | OF0 0 | Reserved 0 |
| 24h-27h | Reserved default | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |
| 28h | MUTEC default | Reserved 0 | Reserved 0 | MCPolarity 0 | M_AOUTA1 1 | M_AOUTB1 1 | M_AOUTA2 1 | M_AOUTB3 1 | Reserved 1 |
| 29h | GPO7 default | Mode1 0 | Mode0 0 | Polarity 0 | Function4 0 | Function3 0 | Function2 0 | Function1 0 | Function0 0 |
| 2Ah | GPO6 default | Mode1 0 | Mode0 0 | Polarity 0 | Function4 0 | Function3 0 | Function2 0 | Function1 0 | Function0 0 |
| 2Bh | GPO5 default | Mode1 0 | Mode0 0 | Polarity 0 | Function4 0 | Function3 0 | Function2 0 | Function1 0 | Function0 0 |
| 2Ch | GPO4 default | Mode1 0 | Mode0 0 | Polarity 0 | Function4 0 | Function3 0 | Function2 0 | Function1 0 | Function0 0 |
| 2Dh | GPO3 default | Mode1 0 | Mode0 0 | Polarity 0 | Function4 0 | Function3 0 | Function2 0 | Function1 0 | Function0 0 |
| 2Eh | GPO2 default | Mode1 0 | Mode0 0 | Polarity 0 | Function4 0 | Function3 0 | Function2 0 | Function1 0 | Function0 0 |
| 2Fh | GPO1 default | Mode1 0 | Mode0 0 | Polarity 0 | Function4 0 | Function3 0 | Function2 0 | Function1 0 | Function0 0 |

5 REGISTER DESCRIPTION

All registers are read/write except for I.D. and Revision Register, OMCK/PLL_CLK Ratio Register, Clock Status and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

5.1 Memory Address Pointer (MAP)

Not a register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| INCR | MAP6 | MAP5 | MAP4 | MAP3 | MAP2 | MAP1 | MAP0 |

5.1.1 INCREMENT(INCR)

Default = 1

Function:

Memory address pointer auto increment control

0 - MAP is not incremented automatically.

1 - Internal MAP is automatically incremented after each read or write.

5.1.2 MEMORY ADDRESS POINTER (MAPX)

Default = 0000001

Function:

Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

5.2 Chip I.D. and Revision Register (address 01h) (Read Only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|---------|---------|---------|---------|
| Chip_ID3 | Chip_ID2 | Chip_ID1 | CHIP_ID0 | Rev_ID3 | Rev_ID2 | Rev_ID1 | Rev_ID0 |

5.2.1 CHIP I.D. (CHIP_IDX)

Default = 1110

Function:

I.D. code for the CS42426. Permanently set to 1110.

5.2.2 CHIP REVISION (REV_IDX)

Default = 0001

Function:

CS42426 revision level. Revision C is coded as 0011.

5.3 Power Control (address 02h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|---------|----------|----------|----------|----------|-----|
| Reserved | PDN_PLL | PDN_ADC | Reserved | PDN_DAC3 | PDN_DAC2 | PDN_DAC1 | PDN |

5.3.1 POWER DOWN PLL (PDN_PLL)

Default = 0

Function:

When enabled, the PLL will remain in a reset state. It is advised that any change of this bit be made while the DACs are muted or the power down bit (PDN) is enabled to eliminate the possibility of audible artifacts.

5.3.2 POWER DOWN ADC (PDN_ADC)

Default = 0

Function:

When enabled the stereo analog to digital converter will remain in a reset state. It is advised that any change of this bit be made while the DACs are muted or the power down bit (PDN) is enabled to eliminate the possibility of audible artifacts.

5.3.3 POWER DOWN DAC PAIRS (PDN_DACX)

Default = 0

Function:

When enabled the respective DAC channel pair x (AOUTAx and AOUTBx) will remain in a reset state.

5.3.4 POWER DOWN (PDN)

Default = 1

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power down bit defaults to 'enabled' on power-up and must be disabled before normal operation can occur.

5.4 Functional Mode (address 03h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|----------|------------|---------|----------|
| DAC_FM1 | DAC_FM0 | ADC_FM1 | ADC_FM0 | Reserved | ADC_SP SEL | DAC_DEM | Reserved |

5.4.1 DAC FUNCTIONAL MODE (DAC_FMx)

Default = 00

00 - Single-Speed Mode (4 to 50 kHz sample rates)

01 - Double-Speed Mode (50 to 100 kHz sample rates)

10 - Quad-Speed Mode (100 to 192 kHz sample rates)

11 - Reserved

Function:

Selects the required range of sample rates for all converters clocked from the DAC serial port (DAC_SP). Bits must be set to the corresponding sample rate range when the DAC_SP is in Master or Slave mode.

5.4.2 ADC FUNCTIONAL MODE (ADC_FMX)

Default = 00

- 00 - Single-Speed Mode (4 to 50 kHz sample rates)
- 01 - Double-Speed Mode (50 to 100 kHz sample rates)
- 10 - Quad-Speed Mode (100 to 192 kHz sample rates)
- 11 - Reserved

Function:

Selects the required range of sample rates for the ADC serial port(ADC_SP). These bits must be set to the corresponding sample rate range when the ADC_SP is in Master or Slave mode.

5.4.3 ADC CLOCK SOURCE SELECT (ADC_CLK SEL)

Default = 0

- 0 - ADC_SDOOUT clocked from the DAC_SP.
- 1 - ADC_SDOOUT clocked from the ADC_SP.

Function:

Selects the desired clocks for the ADC serial output.

5.4.4 DAC DE-EMPHASIS CONTROL (DAC_DEM)

Default = 0

Function:

Enables the digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at the auto-detected sample rate of either 32, 44.1, or 48 kHz. De-emphasis will not be enabled, regardless of this register setting, at any other sample rate. If the FRC_PLL_LK bit is set to a '1'b, then the auto-detect sample rate feature is disabled. To apply the correct de-emphasis filter, use the DE-EMPH bits in the Interrupt Control (address 1Eh) register to set the appropriate sample rate.

| DAC_DEM reg03h[1] | FRC_PLL_LK reg06h[0] | DE-EMPH[1:0] reg1Eh[5:4] | De-Emphasis Mode |
|----------------------|-------------------------|-----------------------------|--|
| 0 | X | XX | No De-Emphasis |
| 1 | 0 | XX | Auto-Detect Fs |
| 1 | 1 | 00 01 10 11 | Reserved 32 kHz 44.1 kHz 48 kHz |

Table 6. DAC De-Emphasis

5.5 Interface Formats (address 04h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|---------|---------|---------|---------|----------|------------|
| DIF1 | DIF0 | ADC_OL1 | ADC_OL0 | DAC_OL1 | DAC_OL0 | Reserved | CODEC_RJ16 |

5.5.1 DIGITAL INTERFACE FORMAT (DIFX)

Default = 01

Function:

These bits select the digital interface format used for the ADC & DAC Serial Port when not in one_line mode. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 7 - 9.

| DIF1 | DIF0 | Description | Format | Figure |
|-------------|-------------|--|---------------|---------------|
| 0 | 0 | Left Justified, up to 24-bit data | 0 | 9 |
| 0 | 1 | I ² S, up to 24-bit data | 1 | 8 |
| 1 | 0 | Right Justified, 16-bit or 24-bit data | 2 | 7 |
| 1 | 1 | reserved | - | - |

Table 7. Digital Interface Formats

5.5.2 ADC ONE_LINE MODE (ADC_OLX)

Default = 00

Function:

These bits select which mode the ADC will use. By default one-line mode is disabled but can be selected using these bits. Please see Figures 10 and 11 to see the format of one-line mode 1 and one-line mode 2.

| ADC_OL1 | ADC_OL2 | Description | Format | Figure |
|----------------|----------------|--|---------------|---------------|
| 0 | 0 | DIF: take the DIF setting from reg04h[7:6] | - | - |
| 0 | 1 | One-Line #1 | 3 | 10 |
| 1 | 0 | One-Line #2 | 4 | 11 |
| 1 | 1 | reserved | - | - |

Table 8. ADC One_Line Mode

5.5.3 DAC ONE_LINE MODE (DAC_OLX)

Default = 00

Function:

These bits select which mode the DAC will use. By default one-line mode is disabled but can be selected using these bits. Please see Figures 10 and 11 to see the format of one-line mode 1 and one-line mode 2.

| DAC_OL1 | DAC_OL2 | Description | Format | Figure |
|----------------|----------------|--|---------------|---------------|
| 0 | 0 | DIF: take the DIF setting from reg04h[7:6] | - | - |
| 0 | 1 | One-Line #1 | 3 | 10 |
| 1 | 0 | One-Line #2 | 4 | 11 |
| 1 | 1 | reserved | - | - |

Table 9. DAC One_Line Mode

5.5.4 CODEC RIGHT JUSTIFIED BITS (CODEC_RJ16)

Default = 0

Function:

This bit determines how many bits to use during right justified mode for the DAC and ADC. By default the DAC and ADC will be in RJ24 bits but can be set to RJ16 bits.

0 - 24 bit mode.

1 - 16 bit mode.

5.6 Misc Control (address 05h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----------|----------|--------|----------|------------|---------------|---------------|
| Ext ADC SCLK | HIZ_RMCK | Reserved | FREEZE | FILT_SEL | HPF_FREEZE | DAC_SP M/S | ADC_SP M/S |

5.6.1 EXTERNAL ADC SCLK SELECT (EXT ADC SCLK)

Default = 0

Function:

This bit identifies the SCLK source for the external ADCs attached to the ADCIN1/2 ports when using one line mode of operation.

0 - ADC_SCLK is used as external ADC SCLK.

1 - DAC_SCLK is used as external ADC SCLK.

5.6.2 RMCK HIGH IMPEDANCE (HIZ_RMCK)

Default = 0

Function:

This bit is used to create a high impedance output on RMCK when the clock signal is not required.

5.6.3 FREEZE CONTROLS (FREEZE)

Default = 0

Function:

This function will freeze the previous output of, and allow modifications to be made, to the Volume Control (address 0Fh-16h), Channel Invert (address 17h) and Mixing Control Pair (address 18h-1Bh) registers without the changes taking effect until the FREEZE is disabled. To make multiple changes in these control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

5.6.4 INTERPOLATION FILTER SELECT (FILT_SEL)

Default = 0

Function:

This feature allows the user to select whether the DAC interpolation filter has a fast or slow roll off. For filter characteristics please See "D/A Digital Filter Characteristics" on page 56.

0 - Fast roll off.

1 - Slow roll off.

5.6.5 HIGH PASS FILTER FREEZE (HPF_FREEZE)

Default = 0

Function:

When this bit is set, the internal high-pass filter for the selected channel will be disabled. The current DC offset value will be frozen and continue to be subtracted from the conversion result. See "A/D Digital Filter Characteristics" on page 52.

5.6.6 DAC SERIAL PORT MASTER/SLAVE SELECT (DAC_SP M/S)

Default = 1

Function:

In Master mode, DAC_SCLK and DAC_LRCK are outputs. Internal dividers will divide the master clock to generate the serial clock and left/right clock. In Slave mode, DAC_SCLK and DAC_LRCK become inputs.

5.6.7 ADC SERIAL PORT MASTER/SLAVE SELECT (ADC_SP M/S)

Default = 1

Function:

In Master mode, ADC_SCLK and ADC_LRCK are outputs. Internal dividers will divide the master clock to generate the serial clock and left/right clock. In Slave mode, ADC_SCLK and ADC_LRCK become inputs.

To use the PLL to lock to ADC_LRCK, the ADC_SP must be in slave mode. When using the PLL to lock to LRCK, if ADC_SDOUT is configured to be clocked by the ADC_SP, then both ADC_SCLK and ADC_LRCK must be present. If ADC_SDOUT is configured to be clocked by the DAC_SP, then only the ADC_LRCK signal must be applied.

5.7 Clock Control (address 06h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----------|------------|------------|----------|----------|----------|------------|
| RMCK_DIV1 | RMCK_DIV0 | OMCK Freq1 | OMCK Freq0 | PLL_LRCK | SW_CTRL1 | SW_CTRL0 | FRC_PLL_LK |

5.7.1 RMCK DIVIDE (RMCK_DIVX)

Default = 00

Function:

Divides/multiplies the internal MCLK, either from the PLL or OMCK, by the selected factor.

| RMCK_DIV1 | RMCK_DIV0 | Description |
|-----------|-----------|---------------|
| 0 | 0 | Divide by 1 |
| 0 | 1 | Divide by 2 |
| 1 | 0 | Divide by 4 |
| 1 | 1 | Multiply by 2 |

Table 10. RMCK Divider Settings

5.7.2 OMCK FREQUENCY (OMCK FREQX)

Default = 00

Function:

Sets the appropriate frequency for the supplied OMCK.

| OMCK Freq1 | OMCK Freq0 | Description |
|------------|------------|----------------------------|
| 0 | 0 | 11.2896 MHz or 12.2880 MHz |
| 0 | 1 | 16.9344 MHz or 18.4320 MHz |
| 1 | 0 | 22.5792 MHz or 24.5760 MHz |
| 1 | 1 | Reserved |

Table 11. OMCK Frequency Settings

5.7.3 PLL LOCK TO LRCK (PLL_LRCK)

Default = 0

0 - *Disabled*

1 - *Enabled*

Function:

When enabled, the internal PLL of the CS42426 will lock to the LRCK of the ADC serial port (ADC_LRCK) while the ADC_SP is in slave mode.

5.7.4 MASTER CLOCK SOURCE SELECT (SW_CTRLX)

Default = 01

Function:

These two bits, along with the UNLOCK bit in register “Interrupt Status (address 20h) (Read Only)” on page 46, determine the master clock source for the CS42426. When SW_CTRL1 and SW_CTRL0 are set to '00'b, selecting the output of the PLL as the internal clock source, and the PLL becomes unlocked, then RMCK will equal OMCK, but all internal and serial port timings are not valid.

| SW_CTRL1 | SW_CTRL0 | UNLOCK | Description |
|----------|----------|--------|---|
| 0 | 0 | X | Manual setting, MCLK sourced from PLL. |
| 0 | 1 | X | Manual setting, MCLK sourced from OMCK. |
| 1 | 0 | 0 | Hold, keep same MCLK source. |
| 1 | 0 | 1 | Auto switch, MCLK sourced from OMCK. |
| 1 | 1 | 0 | Auto switch, MCLK sourced from PLL. |
| 1 | 1 | 1 | Auto switch, MCLK sourced from OMCK. |

Table 12. Master Clock Source Select

5.7.5 FORCE PLL LOCK (FRC_PLL_LK)

Default = 0

Function:

This bit is used to enable the PLL to lock to the ADC_LRCK with the absence of a clock signal on OMCK. When set to a '1'b, the auto-detect sample frequency feature will be disabled. The OMCK/PLL_CLK Ratio (address 07h) (Read Only) register contents are not valid and the PLL_CLK[2:0] bits will be set to '111'b. Use the DE-EMPH[1:0] bits to properly apply de-emphasis filtering.

5.8 OMCK/PLL_CLK Ratio (address 07h) (Read Only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------------|-------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| RATIO7(2 ¹) | RATIO6(2 ⁰) | RATIO5(2 ⁻¹) | RATIO4(2 ⁻²) | RATIO3(2 ⁻³) | RATIO2(2 ⁻⁴) | RATIO1(2 ⁻⁵) | RATIO0(2 ⁻⁶) |

5.8.1 OMCK/PLL_CLK RATIO (RATIOX)

Default = sixth

Function:

This register allows the user to find the exact absolute frequency of the recovered MCLK coming from the PLL. This value is represented as an integer (RATIO7:6) and a fractional (RATIO5:0) part. For example, an OMCK/PLL_CLK ratio of 1.5 would be displayed as 60h.

5.9 Clock Status (address 08h) (Read Only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|------------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Active_CLK | PLL_CLK2 | PLL_CLK1 | PLL_CLK0 |

5.9.1 SYSTEM CLOCK SELECTION (ACTIVE_CLK)

Default = x

0 - Output of PLL

1 - OMCK

Function:

This bit identifies the source of the internal system clock (MCLK).

5.9.2 PLL CLOCK FREQUENCY (PLL_CLKX)

Default = xxxxh

Function:

The CS42426 will auto-detect the ratio between the OMCK and the recovered clock from the PLL, which is displayed in register 07h. Based on this ratio, the absolute frequency of the PLL clock can be determined, and this information is displayed according to the following table. If the absolute frequency of the PLL clock does not match one of the given frequencies, this register will display the closest available value.

NOTE: These bits are set to '111'b when the FRC_PLL_LK bit is '1'b.

| PLL_CLK2 | PLL_CLK1 | PLL_CLK0 | Description |
|----------|----------|----------|-------------|
| 0 | 0 | 0 | 8.1920 MHz |
| 0 | 0 | 1 | 11.2896 MHz |
| 0 | 1 | 0 | 12.288 MHz |
| 0 | 1 | 1 | 16.3840 MHz |
| 1 | 0 | 0 | 22.5792 MHz |
| 1 | 0 | 1 | 24.5760 MHz |
| 1 | 1 | 0 | 45.1584 MHz |
| 1 | 1 | 1 | 49.1520 MHz |

Table 13. PLL Clock Frequency Detection



5.10 Volume Control (address 0Dh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------|------|------|-------|-------------|---------|---------|
| Reserved | SNGVOL | SZC1 | SZC0 | AMUTE | MUTE ADC_SP | RAMP_UP | RAMP_DN |

5.10.1 SINGLE VOLUME CONTROL (SNGVOL)

Default = 0

Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the A1 Channel Volume Control register and the other Volume Control registers are ignored.

5.10.2 SOFT RAMP AND ZERO CROSS CONTROL (SZCX)

Default = 00

00 - Immediate Change

01 - Zero Cross

10 - Soft Ramp

11 - Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

5.10.3 AUTO-MUTE (AMUTE)

Default = 1

0 - Disabled

1 - Enabled

Function:

The Digital-to-Analog converters of the CS42426 will mute the output following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the MUTEC pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits (S2C[1:0]).

5.10.4 SOFT VOLUME RAMP-UP AFTER ERROR (RMP_UP)

Default = 0

0 - Disabled

1 - Enabled

Function:

An un-mute will be performed after executing a filter mode change, after a MCLK/LRCK ratio change or error, and after changing the Functional Mode. When this feature is enabled, this un-mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits (S2C[1:0]). When disabled, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this bit be used in conjunction with the RMP_DN bit.

5.10.5 SOFT RAMP-DOWN BEFORE FILTER MODE CHANGE (RMP_DN)

Default = 0

0 - Disabled

1 - Enabled

Function:

A mute will be performed prior to executing a filter mode or de-emphasis mode change. When this feature is enabled, this mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits (S2C[1:0]). When disabled, an immediate mute is performed prior to executing a filter mode or de-emphasis mode change.

Note: For best results, it is recommended that this bit be used in conjunction with the RMP_UP bit.

5.11 Channel Mute (address 0Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|---------|---------|---------|---------|---------|---------|
| Reserved | Reserved | B3_MUTE | A3_MUTE | B2_MUTE | A2_MUTE | B1_MUTE | A1_MUTE |

5.11.1 INDEPENDENT CHANNEL MUTE (XX_MUTE)

Default = 0

0 - Disabled

1 - Enabled

Function:

The Digital-to-Analog converter outputs of the CS42426 will mute when enabled. The quiescent voltage on the outputs will be retained. The muting function is affected, similar to attenuation changes, by the Soft and Zero Cross bits (S2C[1:0]).

5.12 Volume Control (addresses 0Fh, 10h, 11h, 12h, 13h, 14h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| xx_VOL7 | xx_VOL6 | xx_VOL5 | xx_VOL4 | xx_VOL3 | xx_VOL2 | xx_VOL1 | xx_VOL0 |

5.12.1 VOLUME CONTROL (XX_VOL)

Default = 0

Function:

The Digital Volume Control registers allow independent control of the signal levels in 0.5 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 14. The volume changes are implemented as dictated by the Soft and Zero Cross bits (SZC[1:0]). All volume settings less than -127 dB are equivalent to enabling the MUTE bit for the given channel.

| Binary Code | Decimal Value | Volume Setting |
|-------------|---------------|----------------|
| 00000000 | 0 | 0 dB |
| 00101000 | 40 | -20 dB |
| 01010000 | 80 | -40 dB |
| 01111000 | 120 | -60 dB |
| 10110100 | 180 | -90 dB |

Table 14. Example Digital Volume Settings

5.13 Channel Invert (address 17h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|--------|--------|--------|--------|--------|--------|
| Reserved | Reserved | INV_B3 | INV_A3 | INV_B2 | INV_A2 | INV_B1 | INV_A1 |

5.13.1 INVERT SIGNAL POLARITY (INV_XX)

Default = 0

0 - Disabled

1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

5.14 Mixing Control Pair 1 (Channels A1 & B1)(address 18h)

Mixing Control Pair 2 (Channels A2 & B2)(address 19h)

Mixing Control Pair 3 (Channels A3 & B3)(address 1Ah)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|----------|-----------|-----------|-----------|-----------|-----------|
| Px_A=B | Reserved | Reserved | Px_ATAPI4 | Px_ATAPI3 | Px_ATAPI2 | Px_ATAPI1 | Px_ATAPI0 |

5.14.1 CHANNEL A VOLUME = CHANNEL B VOLUME (PX_A=B)

Default = 0

0 - Disabled

1 - Enabled

Function:

The AOUTAx and AOUTBx volume levels are independently controlled by the A and the B Channel Volume Control registers when this function is disabled. The volume on both AOUTAx and AOUTBx are determined by the A Channel Volume Control registers (per A-B pair), and the B Channel Volume Control registers are ignored when this function is enabled.

5.14.2 ATAPI CHANNEL MIXING AND MUTING (PX_ATAPIX)

Default = 01001

Function:

The CS42426 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 15 and Figure 5 for additional information.

| ATAPI4 | ATAPI3 | ATAPI2 | ATAPI1 | ATAPI0 | AOUTAx | AOUTBx |
|--------|--------|--------|--------|--------|-------------|-------------|
| 0 | 0 | 0 | 0 | 0 | MUTE | MUTE |
| 0 | 0 | 0 | 0 | 1 | MUTE | bR |
| 0 | 0 | 0 | 1 | 0 | MUTE | bL |
| 0 | 0 | 0 | 1 | 1 | MUTE | b[(L+R)/2] |
| 0 | 0 | 1 | 0 | 0 | aR | MUTE |
| 0 | 0 | 1 | 0 | 1 | aR | bR |
| 0 | 0 | 1 | 1 | 0 | aR | bL |
| 0 | 0 | 1 | 1 | 1 | aR | b[(L+R)/2] |
| 0 | 1 | 0 | 0 | 0 | aL | MUTE |
| 0 | 1 | 0 | 0 | 1 | aL | bR |
| 0 | 1 | 0 | 1 | 0 | aL | bL |
| 0 | 1 | 0 | 1 | 1 | aL | b[(L+R)/2] |
| 0 | 1 | 1 | 0 | 0 | a[(L+R)/2] | MUTE |
| 0 | 1 | 1 | 0 | 1 | a[(L+R)/2] | bR |
| 0 | 1 | 1 | 1 | 0 | a[(L+R)/2] | bL |
| 0 | 1 | 1 | 1 | 1 | a[(L+R)/2] | b[(L+R)/2] |
| 1 | 0 | 0 | 0 | 0 | MUTE | MUTE |
| 1 | 0 | 0 | 0 | 1 | MUTE | bR |
| 1 | 0 | 0 | 1 | 0 | MUTE | bL |
| 1 | 0 | 0 | 1 | 1 | MUTE | [(aL+bR)/2] |
| 1 | 0 | 1 | 0 | 0 | aR | MUTE |
| 1 | 0 | 1 | 0 | 1 | aR | bR |
| 1 | 0 | 1 | 1 | 0 | aR | bL |
| 1 | 0 | 1 | 1 | 1 | aR | [(bL+aR)/2] |
| 1 | 1 | 0 | 0 | 0 | aL | MUTE |
| 1 | 1 | 0 | 0 | 1 | aL | bR |
| 1 | 1 | 0 | 1 | 0 | aL | bL |
| 1 | 1 | 0 | 1 | 1 | aL | [(aL+bR)/2] |
| 1 | 1 | 1 | 0 | 0 | [(aL+bR)/2] | MUTE |
| 1 | 1 | 1 | 0 | 1 | [(aL+bR)/2] | bR |
| 1 | 1 | 1 | 1 | 0 | [(bL+aR)/2] | bL |
| 1 | 1 | 1 | 1 | 1 | [(aL+bR)/2] | [(aL+bR)/2] |

Table 15. ATAPI Decode

5.15 ADC Left Channel Gain (address 1Ch)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|--------|--------|--------|--------|--------|--------|
| Reserved | Reserved | LGAIN5 | LGAIN4 | LGAIN3 | LGAIN2 | LGAIN1 | LGAIN0 |

5.15.1 ADC LEFT CHANNEL GAIN (LGAINX)

Default = 00h

Function:

The level of the left analog channel can be adjusted in 1 dB increments as dictated by the Soft and Zero Cross bits (S2C[1:0]) from +15 to -15 dB. Levels are decoded in two's complement, as shown in Table 16.

5.16 ADC Right Channel Gain (address 1Dh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|--------|--------|--------|--------|--------|--------|
| Reserved | Reserved | RGAIN5 | RGAIN4 | RGAIN3 | RGAIN2 | RGAIN1 | RGAIN0 |

5.16.1 ADC RIGHT CHANNEL GAIN (RGAINX)

Default = 00h

Function:

The level of the right analog channel can be adjusted in 1dB increments as dictated by the Soft and Zero Cross bits (S2C[1:0]) from +15 to -15dB. Levels are decoded in two's complement, as shown in Table 16.

| Binary Code | Decimal Value | Volume Setting |
|-------------|---------------|----------------|
| 001111 | +15 | +15 dB |
| 001010 | +10 | +10 dB |
| 000101 | +5 | +5 dB |
| 000000 | 0 | 0 dB |
| 111011 | -5 | -5 dB |
| 110110 | -10 | -10 dB |
| 110001 | -15 | -15 dB |

Table 16. Example ADC Input Gain Settings

5.17 Interrupt Control (address 1Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----------|----------|------|------|----------|----------|
| SP_SYNC | Reserved | DE-EMPH1 | DE-EMPH0 | INT1 | INT0 | Reserved | Reserved |

5.17.1 SERIAL PORT SYNCHRONIZATION (SP_SYNC)

Default = 0

0 - DAC & ADC Serial Port timings not in phase

1 - DAC & ADC Serial Port timings are in phase

Function:

Forces the LRCK and SCLK from the DAC & ADC Serial Ports to align and operate in phase. This function will operate when both ports are running at the same sample rate or when operating at different sample rates.



5.17.2 DE-EMPHASIS SELECT BITS (DE-EMPHX)

Default = 00

00 - Reserved

01 - De-Emphasis for 32 kHz sample rate.

10 - De-Emphasis for 44.1 kHz sample rate.

11 - De-Emphasis for 48 kHz sample rate.

Function:

Used to specify which de-emphasis filter to apply when the FORCE PLL LOCK (FRC_PLL_LK) in reg06h is enabled.

5.17.3 INTERRUPT PIN CONTROL (INTX)

Default = 00

00 - Active high; high output indicates interrupt condition has occurred

01 - Active low, low output indicates an interrupt condition has occurred

10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.

11 - Reserved

Function:

Determines how the interrupt pin (INT) will indicate an interrupt condition.

5.18 Interrupt Status (address 20h) (Read Only)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|----------|----------|----------|----------|----------|----------|
| UNLOCK | Reserved | Reserved | Reserved | Reserved | Reserved | OverFlow | Reserved |

For all bits in this register, a "1" means the associated interrupt condition has occurred at least once since the register was last read. A "0" means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0. Status bits that are masked off in the associated mask register will always be "0" in this register.

5.18.1 PLL UNLOCK (UNLOCK)

Default = 0

Function:

PLL unlock status bit. This bit will go high if the PLL becomes unlocked.

5.18.2 ADC OVERFLOW (OVERFLOW)

Default = 0

Function:

Indicates that there is an over-range condition anywhere in the CS42426 ADC signal path.

5.19 Interrupt Mask (address 21h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----------|----------|----------|----------|-----------|----------|
| UNLOCKM | Reserved | Reserved | Reserved | Reserved | Reserved | OverFlowM | Reserved |

Default = 00000000

Function:

The bits of this register serve as a mask for the interrupt sources found in the register “Interrupt Status (address 20h) (Read Only)” on page 46. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in the Interrupt Status register.

5.20 Interrupt Mode MSB (address 22h)

Interrupt Mode LSB (address 23h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----------|----------|----------|----------|-----|----------|
| UNLOCK1 | Reserved | Reserved | Reserved | Reserved | Reserved | OF1 | Reserved |
| UNLOCK0 | Reserved | Reserved | Reserved | Reserved | Reserved | OF0 | Reserved |

Default = 00000000

Function:

The two Interrupt Mode registers form a 2-bit code for each Interrupt Status register function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level(Active High or Low) only depends on the INT(1:0) bits located in the register “Interrupt Control (address 1Eh)” on page 45.

00 - Rising edge active

01 - Falling edge active

10 - Level active

11 - Reserved

5.21 MuteC Pin Control (address 28h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|------------|----------|----------|----------------------|----------------------|----------|
| Reserved | Reserved | MCPolarity | M_AOUTA1 | M_AOUTB1 | M_AOUTA2 M_AOUTB2 | M_AOUTA3 M_AOUTB3 | Reserved |

5.21.1 MUTEC POLARITY SELECT (MCPOLARITY)

Default = 0

0 - Active low

1 - Active high

Function:

Determines the polarity of the MUTEC pin.

5.21.2 CHANNEL MUTES SELECT (M_AOUTXX)

Default = 1111

0 - Channel mute is not mapped to the MUTEC pin

1 - Channel mute is mapped to the MUTEC pin

Function:

Determines which channel mutes will be mapped to the MUTEC pin. If no channel mute bits are mapped, then the MUTEC pin is driven to the "active" state as defined by the POLARITY bit. These Channel Mute Select bits are "ANDed" together in order for the MUTEC pin to go active. This means that if multiple Channel Mutes are selected to be mapped to the MUTEC pin, then all corresponding channels must be muted before the MUTEC will go active.

5.22 General Purpose Pin Control (addresses 29h to 2Fh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|----------|-----------|-----------|-----------|-----------|-----------|
| Mode1 | Mode0 | Polarity | Function4 | Function3 | Function2 | Function1 | Function0 |

5.22.1 MODE CONTROL (MODEX)

Default = 00

00 - Reserved

01 - Mute Mode

10 - GPO/Overflow Mode

11 - GPO, Drive High Mode

Function:

Mute Mode - The pin is configured as a dedicated mute pin. The muting function is controlled by the Function bits.

GPO/Overflow Mode - The pin is configured as a general purpose output driven low or as a dedicated ADC overflow pin indicating an over-range condition anywhere in the ADC signal path for either the left or right channel. The Functionx bits determine the operation of the pin. When configured as a GPO with the output driven low, the driver is a CMOS driver. When configured to identify an ADC Overflow condition, the driver is an open drain driver requiring a pull-up resistor.

GPO, Drive High Mode - The pin is configured as a general purpose output driven high.

5.22.2 POLARITY SELECT (POLARITY)

Default = 0

Function:

Mute Mode - If the pin is configured as a dedicated mute output pin, then the polarity bit determines the polarity of the mapped pin according to the following

0 - Active low

1 - Active high

GPO/Overflow Mode - If the pin is configured as a GPO/Overflow Mode pin, the polarity bit is ignored. It is recommended that in this mode this bit be set to 0.

GPO, Drive High Mode - If the pin is configured as a general purpose output driven high, the polarity bit is ignored. It is recommended that in this mode this bit be set to 0.

5.22.3 FUNCTIONAL CONTROL (FUNCTIONX)

Default = 00000

Function:

Mute Mode - If the pin is configured as a dedicated mute pin, then the functional bits determine which channel mutes will be mapped to this pin according to the following table.

0 - Channel mute is not mapped to the GPOx pin

1 - Channel mute is mapped to the GPOx pin:

| GPOx | Reg Address | Function4 | Function3 | Function2 | Function1 | Function0 |
|----------------|-------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|-----------|
| GPO7 pin 42 | 29h | <i>M_AOUTA1</i> | <i>M_AOUTB1</i> | <i>M_AOUTA2</i> <i>M_AOUTB2</i> | <i>M_AOUTA3</i> <i>M_AOUTB3</i> | Reserved |
| GPO6 pin 43 | 2Ah | <i>M_AOUTA1</i> <i>M_AOUTB1</i> | <i>M_AOUTA2</i> | <i>M_AOUTB2</i> | <i>M_AOUTA3</i> <i>M_AOUTB3</i> | Reserved |
| GPO5 pin 44 | 2Bh | <i>M_AOUTA1</i> <i>M_AOUTB1</i> | <i>M_AOUTA2</i> | <i>M_AOUTB2</i> | <i>M_AOUTA3</i> <i>M_AOUTB3</i> | Reserved |
| GPO4 pin 45 | 2Ch | <i>M_AOUTA1</i> <i>M_AOUTB1</i> | <i>M_AOUTA2</i> <i>M_AOUTB2</i> | <i>M_AOUTA3</i> | <i>M_AOUTB3</i> | Reserved |
| GPO3 pin 46 | 2Dh | <i>M_AOUTA1</i> <i>M_AOUTB1</i> | <i>M_AOUTA2</i> <i>M_AOUTB2</i> | <i>M_AOUTA3</i> | <i>M_AOUTB3</i> | Reserved |
| GPO2 pin 47 | 2Eh | <i>M_AOUTA1</i> <i>M_AOUTB1</i> | <i>M_AOUTA2</i> <i>M_AOUTB2</i> | <i>M_AOUTA3</i> <i>M_AOUTB3</i> | Reserved | Reserved |
| GPO1 pin 48 | 2Fh | <i>M_AOUTA1</i> <i>M_AOUTB1</i> | <i>M_AOUTA2</i> <i>M_AOUTB2</i> | <i>M_AOUTA3</i> <i>M_AOUTB3</i> | Reserved | Reserved |

GPO/Overflow Mode - If the pin is configured as a GPO/Overflow Mode pin, then the Function1 and Function0 bits determine how the output will behave according to the following table. It is recommended that in this mode the remaining functional bits be set to 0.

| Function1 | Function0 | GPOx | Driver Type |
|-----------|-----------|-------------|-------------|
| 0 | 0 | Drive Low | CMOS |
| 1 | 1 | OVFL R or L | Open Drain |

GPO, Drive High Mode - If the pin is configured as a general purpose output, then the functional bits are ignored and the pin is driven high. It is recommended that in this mode all the functional bits be set to 0.

6 CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A = 25^\circ C$.)

SPECIFIED OPERATING CONDITIONS ($T_A = 25^\circ C$; AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|----------------------------------|------------|--------|------------|--------------------------|
| DC Power Supply | Analog power | VA | 4.75 | 5.0 | V |
| | Digital internal power | VD | 3.13 | 3.3 | V |
| | Serial data port interface power | VLS | 1.8 | 5.0 | V |
| | Control port interface power | VLC | 1.8 | 5.0 | V |
| Ambient Operating Temperature (power applied) CS42426-CQ CS42426-DQ | T_A | -10 -40 | - - | +70 +85 | $^\circ C$ $^\circ C$ |

ABSOLUTE MAXIMUM RATINGS (AGND = DGND = 0 V; all voltages with respect to ground.)

| Parameters | Symbol | Min | Max | Units |
|--|----------------------------------|-------------|------------|--------------------------|
| DC Power Supply | Analog power | VA | -0.3 | V |
| | Digital internal power | VD | -0.3 | V |
| | Serial data port interface power | VLS | -0.3 | V |
| | Control port interface power | VLC | -0.3 | V |
| Input Current (Note 1) | I_{in} | - | ± 10 | mA |
| Analog Input Voltage (Note 2) | V_{IN} | AGND-0.7 | $VA+0.7$ | V |
| Digital Input Voltage (Note 2) | Serial data port interface | V_{IND-S} | $VLS+ 0.4$ | V |
| | Control port interface | V_{IND-C} | $VLC+ 0.4$ | V |
| Ambient Operating Temperature(power applied) CS42426-CQ CS42426-DQ | T_A | -20 -50 | +85 +95 | $^\circ C$ $^\circ C$ |
| Storage Temperature | T_{stg} | -65 | +150 | $^\circ C$ |

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Any pin except supplies. Transient currents of up to ± 100 mA on the analog input pins will not cause SCR latch-up.
2. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS ($T_A = 25^\circ C$; $VA = 5 V$, $VD = 3.3 V$, Logic "0" = DGND)

=AGND = 0 V; Logic "1" = VLS = VLC = 5 V; Measurement Bandwidth 10 Hz to 20 kHz unless otherwise specified.
 Full scale input sine wave, 997 Hz.; OMCK = 12.288 MHz; Single speed Mode DAC_SCLK = 3.072 MHz; Double Speed Mode DAC_SCLK = 6.144 MHz; Quad Speed Mode DAC_SCLK = 12.288 MHz.)

| Parameter (Note 3) | Symbol | Min | CS42426-CQ | | | Min | CS42426-DQ | | | Unit |
|--|-----------------------------|-----|------------|--------|-----|------|------------|-----|---|--------|
| Single Speed Mode (Fs=48 kHz) | | | | | | | | | | |
| Dynamic Range | A-weighted | | 108 | 114 | - | 106 | 114 | - | - | dB |
| | unweighted | | 105 | 111 | - | 103 | 111 | - | - | dB |
| Total Harmonic Distortion + Noise | THD+N | | | -100 | -94 | | -100 | -92 | - | dB |
| (Note 4) | -1 dB | | | -91 | - | | -91 | - | - | dB |
| | -20 dB | | | -51 | - | | -51 | - | - | dB |
| | -60 dB | | | | | | | | | dB |
| Double Speed Mode (Fs=96 kHz) | | | | | | | | | | |
| Dynamic Range | A-weighted | | 108 | 114 | - | 106 | 114 | - | - | dB |
| | unweighted | | 105 | 111 | - | 103 | 111 | - | - | dB |
| | 40 kHz bandwidth unweighted | | - | 108 | - | - | 108 | - | - | dB |
| Total Harmonic Distortion + Noise | THD+N | | | -100 | -94 | | -100 | -92 | - | dB |
| (Note 4) | -1 dB | | | -91 | - | | -91 | - | - | dB |
| | -20 dB | | | -51 | - | | -51 | - | - | dB |
| | -60 dB | | | | | | | | | dB |
| 40 kHz bandwidth | -1 dB | | | -97 | - | | -97 | - | - | dB |
| Quad Speed Mode (Fs=192 kHz) | | | | | | | | | | |
| Dynamic Range | A-weighted | | 108 | 114 | - | 106 | 114 | - | - | dB |
| | unweighted | | 105 | 111 | - | 103 | 111 | - | - | dB |
| | 40 kHz bandwidth unweighted | | - | 108 | - | - | 108 | - | - | dB |
| Total Harmonic Distortion + Noise | THD+N | | | -100 | -94 | | -100 | -92 | - | dB |
| (Note 4) | -1 dB | | | -91 | - | | -91 | - | - | dB |
| | -20 dB | | | -51 | - | | -51 | - | - | dB |
| | -60 dB | | | | | | | | | dB |
| 40 kHz bandwidth | -1 dB | | | -97 | - | | -97 | - | - | dB |
| Dynamic Performance for All Modes | | | | | | | | | | |
| Interchannel Isolation | | - | | 110 | - | - | 110 | - | - | dB |
| Interchannel Phase Deviation | | - | | 0.0001 | - | - | 0.0001 | - | - | Degree |
| DC Accuracy | | | | | | | | | | |
| Interchannel Gain Mismatch | | - | | 0.1 | - | - | 0.1 | - | - | dB |
| Gain Drift | | - | | +/-100 | - | - | +/-100 | - | - | ppm/°C |
| Offset Error | HPF_FREEZE enabled | | - | 0 | - | - | 0 | - | - | LSB |
| | HPF_FREEZE disabled | | - | 100 | - | - | 100 | - | - | LSB |
| Analog Input | | | | | | | | | | |
| Full-scale Differential Input Voltage | | 1.9 | 2.0 | 2.1 | 1.8 | 2.0 | 2.2 | | | Vrms |
| Input Impedance(differential) (Note 5) | | 37 | - | - | 37 | - | - | - | - | kΩ |
| Common Mode Rejection Ratio | CMRR | - | 82 | - | - | 82 | - | - | - | dB |
| VQ Nominal Voltage | | - | 2.7 | - | - | 2.7 | - | - | - | V |
| Output Impedance | | - | 50 | - | - | 50 | - | - | - | kΩ |
| Maximum allowable DC current | | - | 0.01 | - | - | 0.01 | - | - | - | mA |

| | | | | | | | |
|------------------------------|---|------|---|---|------|---|----|
| FILT+ Nominal Voltage | - | 5.0 | - | - | 5.0 | - | V |
| Output Impedance | - | 35 | - | - | 35 | - | kΩ |
| Maximum allowable DC current | - | 0.01 | - | - | 0.01 | - | mA |

Notes:

3. Typical performance numbers are taken at 25° C. Min/Max performance numbers are guaranteed across the specified temperature range, T_A .
4. Referred to the typical full-scale voltage.
5. Measured between AIN+ and AIN-.

A/D DIGITAL FILTER CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-----------------|------|-----------|--------|------|
| <i>Single Speed Mode (2 to 50 kHz sample rates)</i> | | | | | |
| Passband (-0.1 dB) | (Note 6) | 0 | - | 0.47 | Fs |
| Passband Ripple | | - | - | ±0.035 | dB |
| Stopband (Note 6) | | 0.58 | - | - | Fs |
| Stopband Attenuation | | -95 | - | - | dB |
| Total Group Delay (Fs = Output Sample Rate) | t_{gd} | - | 12/Fs | - | s |
| Group Delay Variation vs. Frequency | Δt_{gd} | - | - | 0.0 | μs |
| <i>Double Speed Mode (50 to 100 kHz sample rates)</i> | | | | | |
| Passband (-0.1 dB) | (Note 6) | 0 | - | 0.45 | Fs |
| Passband Ripple | | - | - | ±0.035 | dB |
| Stopband (Note 6) | | 0.68 | - | - | Fs |
| Stopband Attenuation | | -92 | - | - | dB |
| Total Group Delay (Fs = Output Sample Rate) | t_{gd} | - | 9/Fs | - | s |
| Group Delay Variation vs. Frequency | Δt_{gd} | - | - | 0.0 | μs |
| <i>Quad Speed Mode (100 to 192 kHz sample rates)</i> | | | | | |
| Passband (-0.1 dB) | (Note 6) | 0 | - | 0.24 | Fs |
| Passband Ripple | | - | - | ±0.035 | dB |
| Stopband (Note 6) | | 0.78 | - | - | Fs |
| Stopband Attenuation | | -97 | - | - | dB |
| Total Group Delay (Fs = Output Sample Rate) | t_{gd} | - | 5/Fs | - | s |
| Group Delay Variation vs. Frequency | Δt_{gd} | - | - | 0.0 | μs |
| <i>High Pass Filter Characteristics</i> | | | | | |
| Frequency Response -3.0 dB | | - | 1 | - | Hz |
| -0.13 dB (Note 7) | | 20 | - | - | Hz |
| Phase Deviation @ 20 Hz (Note 7) | | - | 10 | - | Deg |
| Passband Ripple | | - | - | 0 | dB |
| Filter Setting Time | | - | $10^5/Fs$ | - | s |

Notes:

6. The filter frequency response scales precisely with Fs.
7. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

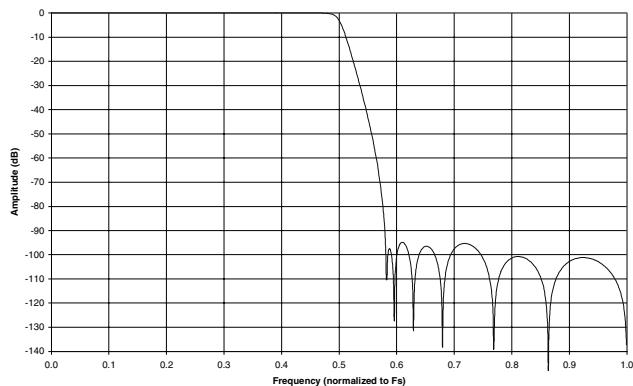


Figure 20. Single Speed Mode Stopband Rejection

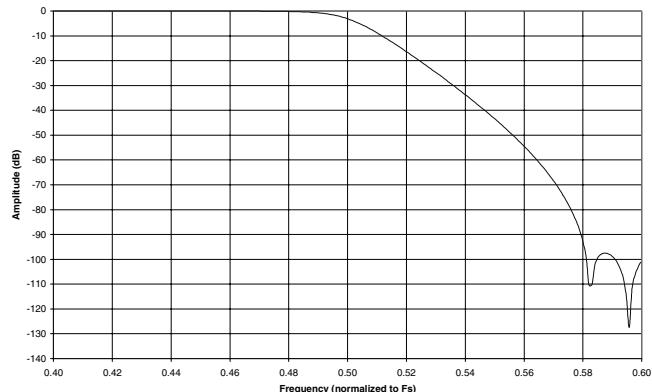


Figure 21. Single Speed Mode Transition Band

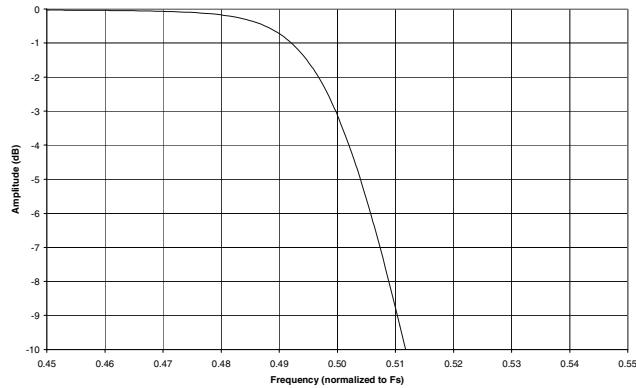


Figure 22. Single Speed Mode Transition Band (Detail)

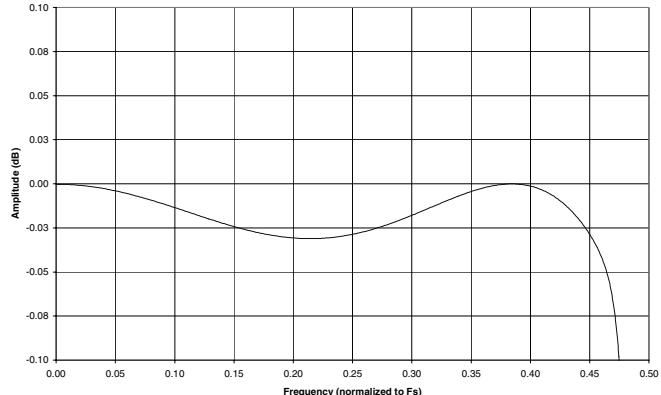


Figure 23. Single Speed Mode Passband Ripple

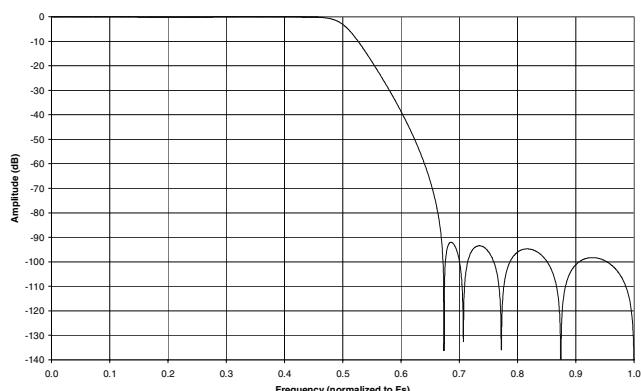


Figure 24. Double Speed Mode Stopband Rejection

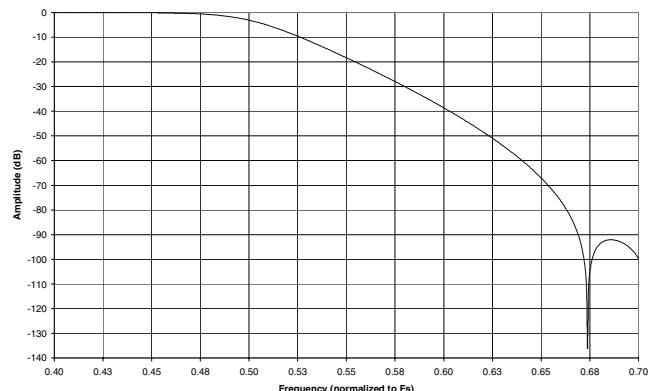


Figure 25. Double Speed Mode Transition Band

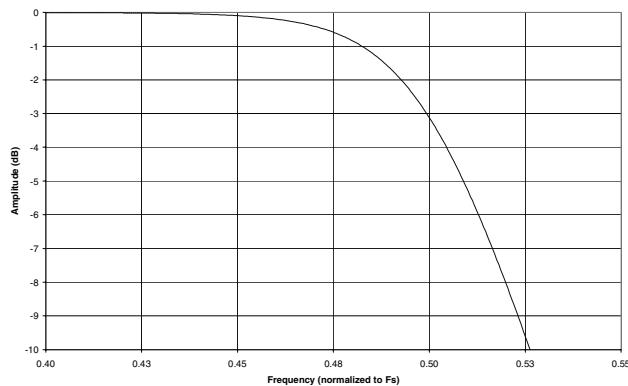


Figure 26. Double Speed Mode Transition Band (Detail)

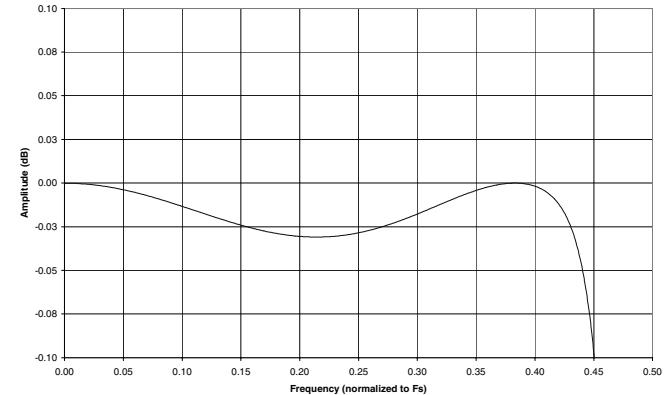


Figure 27. Double Speed Mode Passband Ripple

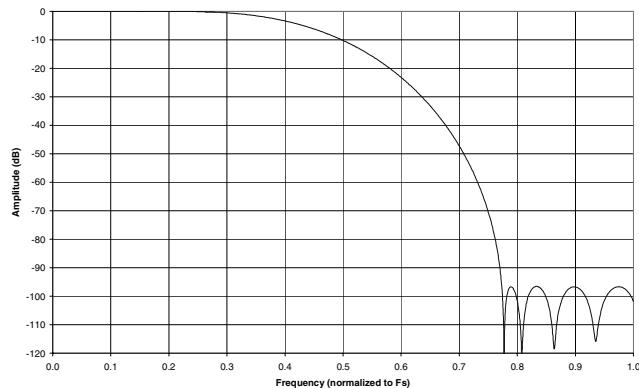


Figure 28. Quad Speed Mode Stopband Rejection

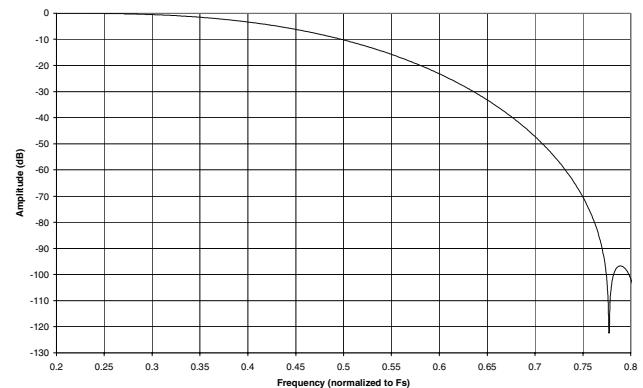


Figure 29. Quad Speed Mode Transition Band

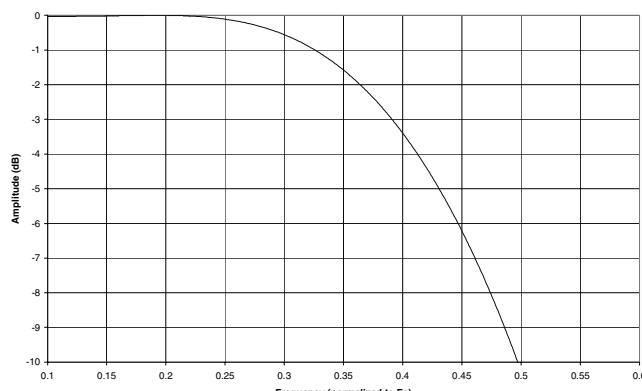


Figure 30. Quad Speed Mode Transition Band (Detail)

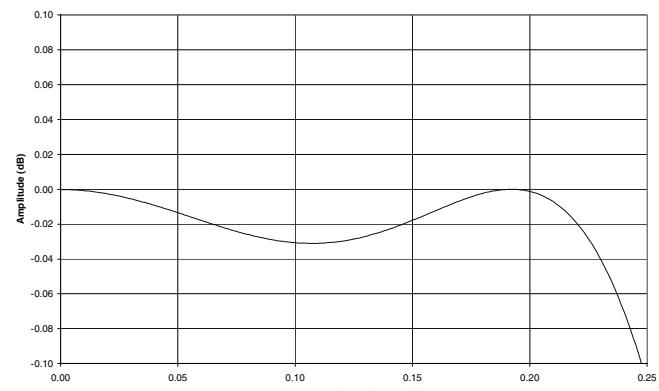


Figure 31. Quad Speed Mode Passband Ripple



ANALOG OUTPUT CHARACTERISTICS ($T_A = 25^\circ C$; $V_A = 5 V$, $V_D = 3.3 V$, Logic "0" = DGND = AGND = 0 V; Logic "1" = VLS = VLC = 5V; Measurement Bandwidth 10 Hz to 20 kHz unless otherwise specified.; Full scale output 997 Hz sine wave, Test load $R_L = 3 k\Omega$, $C_L = 30 pF$; OMCK = 12.288 MHz; Single speed Mode, DAC_SCLK = 3.072 MHz; Double Speed Mode, DAC_SCLK = 6.144 MHz; Quad Speed Mode, DAC_SCLK = 12.288 MHz.)

| Parameter | Symbol | Min | CS42426-CQ Typ | Max | Min | CS42426-DQ Typ | Max | Unit |
|---|-----------|-------|-------------------|-------|-------|-------------------|-------|-----------|
| <i>Dynamic performance for all modes</i> | | | | | | | | |
| Dynamic Range (Note 8) | | | | | | | | |
| 24-bit A-weighted | | 108 | 114 | - | 108 | 114 | - | dB |
| unweighted | | 105 | 111 | - | 105 | 111 | - | dB |
| 16-bit A-Weighted | | - | 97 | - | - | 97 | - | dB |
| (Note 9) unweighted | | - | 94 | - | - | 94 | - | dB |
| Total Harmonic Distortion + Noise | THD+N | | | | | | | |
| 24-bit | 0 dB | - | -100 | -94 | - | -100 | -94 | dB |
| | -20 dB | - | -91 | - | - | -91 | - | dB |
| | -60 dB | - | -51 | - | - | -51 | - | dB |
| 16-bit | 0 dB | - | -94 | - | - | -94 | - | dB |
| (Note 9) | -20 dB | - | -74 | - | - | -74 | - | dB |
| | -60 dB | - | -34 | - | - | -34 | - | dB |
| Idle Channel Noise/Signal-to-noise ratio | | - | 114 | - | - | 114 | - | dB |
| Interchannel Isolation (1 kHz) | | - | 90 | - | - | 90 | - | dB |
| <i>Analog Output Characteristics for all modes</i> | | | | | | | | |
| Full Scale Differential Output | | .88VA | .92VA | .94VA | .88VA | .92VA | .94VA | Vpp |
| Interchannel Gain Mismatch | | - | 0.1 | - | - | 0.1 | - | dB |
| Gain Drift | | - | 100 | - | - | 100 | - | ppm/°C |
| Output Impedance | Z_{OUT} | - | 100 | - | - | 100 | - | Ω |
| AC-Load Resistance | R_L | 3 | - | - | 3 | - | - | $k\Omega$ |
| Load Capacitance | C_L | - | - | 30 | - | - | 30 | pF |

Notes: 8. One-half LSB of triangular PDF dither is added to data.
 9. Performance limited by 16-bit quantization noise.



D/A DIGITAL FILTER CHARACTERISTICS

| Parameter | Fast Roll-Off | | | Slow Roll-Off | | | Unit |
|---|---------------|--------|----------|---------------|--------|----------|------|
| | Min | Typ | Max | Min | Typ | Max | |
| Combined Digital and On-chip Analog Filter Response - Single Speed Mode - 48 kHz | | | | | | | |
| Passband (Note 10) to -0.01 dB corner | 0 | - | 0.4535 | 0 | - | 0.4166 | Fs |
| to -3 dB corner | 0 | - | 0.4998 | 0 | - | 0.4998 | Fs |
| Frequency Response 10 Hz to 20 kHz | -0.01 | - | +0.01 | -0.01 | - | +0.01 | dB |
| StopBand | 0.5465 | - | - | 0.5834 | - | - | Fs |
| StopBand Attenuation (Note 11) | 90 | - | - | 64 | - | - | dB |
| Group Delay | - | 12/Fs | - | - | 6.5/Fs | - | s |
| Passband Group Delay Deviation 0 - 20 kHz | - | - | ±0.41/Fs | - | - | ±0.14/Fs | s |
| De-emphasis Error (Note 12) Fs = 32 kHz | - | - | ±0.23 | - | - | ±0.23 | dB |
| (Relative to 1 kHz) Fs = 44.1 kHz | - | - | ±0.14 | - | - | ±0.14 | dB |
| Fs = 48 kHz | - | - | ±0.09 | - | - | ±0.09 | dB |
| Combined Digital and On-chip Analog Filter Response - Double Speed Mode - 96 kHz | | | | | | | |
| Passband (Note 10) to -0.01 dB corner | 0 | - | 0.4166 | 0 | - | 0.2083 | Fs |
| to -3 dB corner | 0 | - | 0.4998 | 0 | - | 0.4998 | Fs |
| Frequency Response 10 Hz to 20 kHz | -0.01 | - | 0.01 | -0.01 | - | 0.01 | dB |
| StopBand | 0.5834 | - | - | 0.7917 | - | - | Fs |
| StopBand Attenuation (Note 11) | 80 | - | - | 70 | - | - | dB |
| Group Delay | - | 4.6/Fs | - | - | 3.9/Fs | - | s |
| Passband Group Delay Deviation 0 - 20 kHz | - | - | ±0.03/Fs | - | - | ±0.01/Fs | s |
| Combined Digital and On-chip Analog Filter Response - Quad Speed Mode - 192 kHz | | | | | | | |
| Passband (Note 10) to -0.01 dB corner | 0 | - | 0.1046 | 0 | - | 0.1042 | Fs |
| to -3 dB corner | 0 | - | 0.4897 | 0 | - | 0.4813 | Fs |
| Frequency Response 10 Hz to 20 kHz | -0.01 | - | 0.01 | -0.01 | - | 0.01 | dB |
| StopBand | 0.6355 | - | - | 0.8683 | - | - | Fs |
| StopBand Attenuation (Note 11) | 90 | - | - | 75 | - | - | dB |
| Group Delay | - | 4.7/Fs | - | - | 4.2/Fs | - | s |
| Passband Group Delay Deviation 0 - 20 kHz | - | - | ±0.01/Fs | - | - | ±0.01/Fs | s |

Notes:

10. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 32 to 55) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
11. Single and Double Speed Mode Measurement Bandwidth is from stopband to 3 Fs. Quad Speed Mode Measurement Bandwidth is from stopband to 1.34 Fs.
12. De-emphasis is available only in Single Speed Mode.

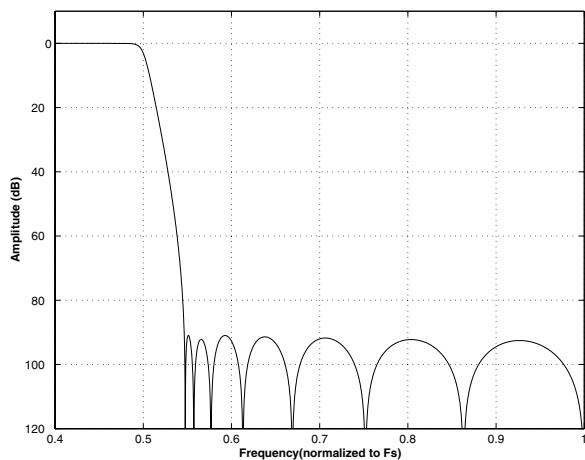


Figure 32. Single Speed (fast) Stopband Rejection

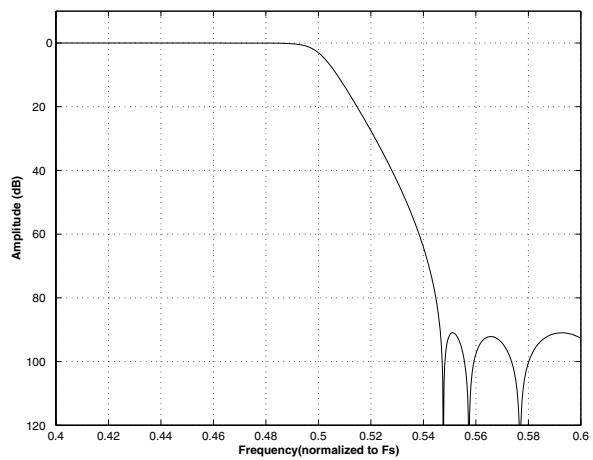


Figure 33. Single Speed (fast) Transition Band

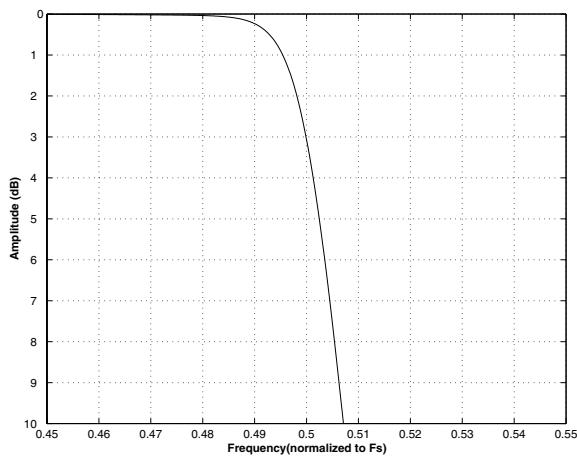


Figure 34. Single Speed (fast) Transition Band (detail)

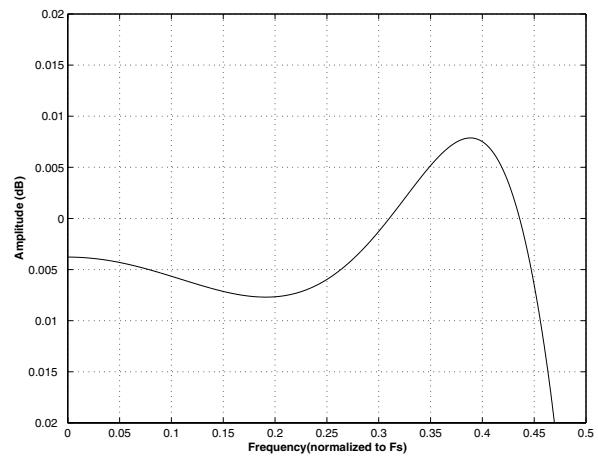


Figure 35. Single Speed (fast) Passband Ripple

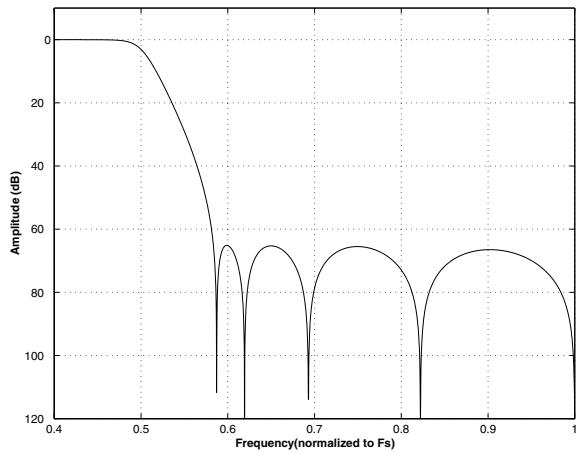


Figure 36. Single Speed (slow) Stopband Rejection

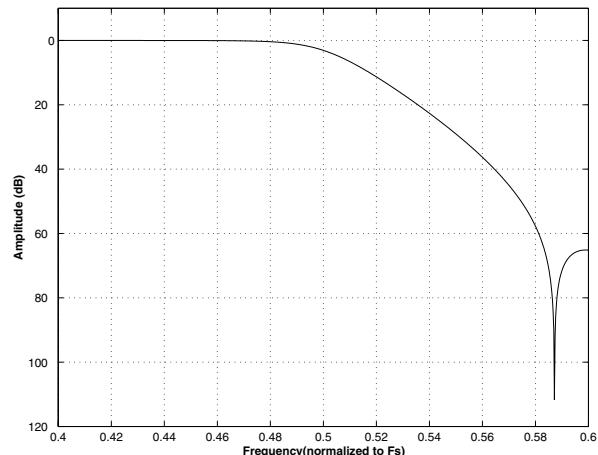


Figure 37. Single Speed (slow) Transition Band

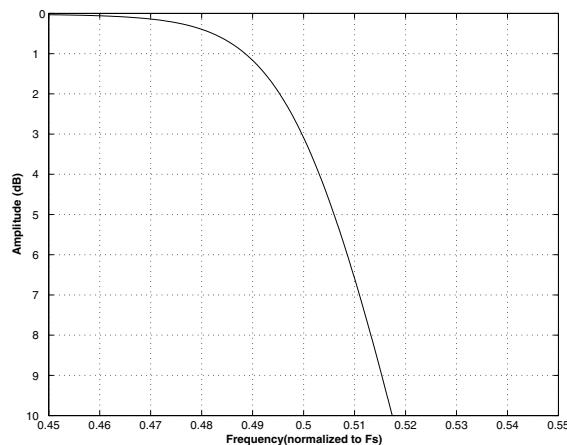


Figure 38. Single Speed (slow) Transition Band (detail)

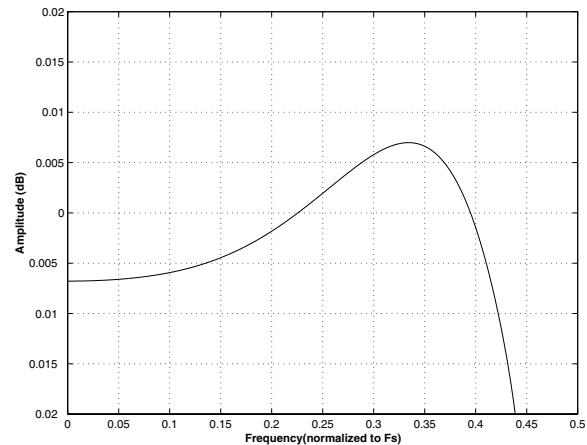


Figure 39. Single Speed (slow) Passband Ripple

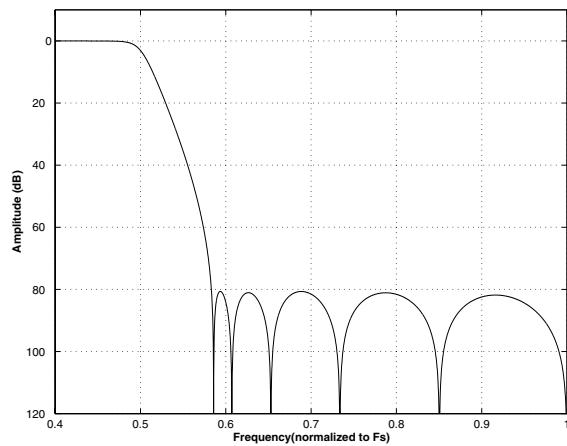


Figure 40. Double Speed (fast) Stopband Rejection

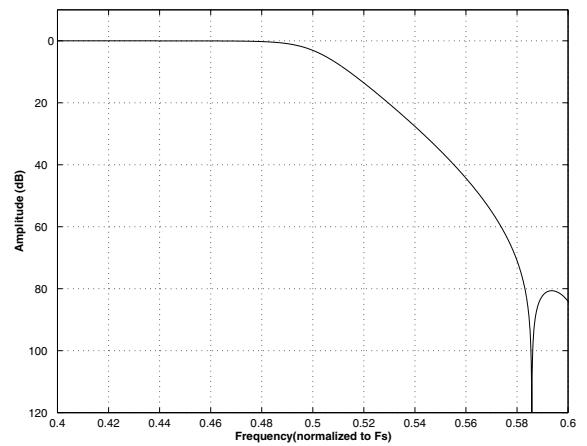


Figure 41. Double Speed (fast) Transition Band

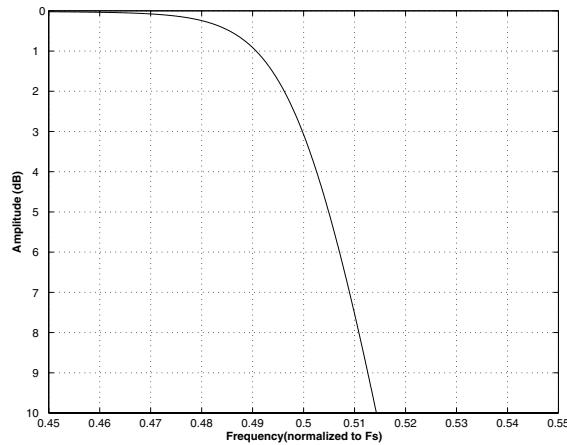


Figure 42. Double Speed (fast) Transition Band (detail)

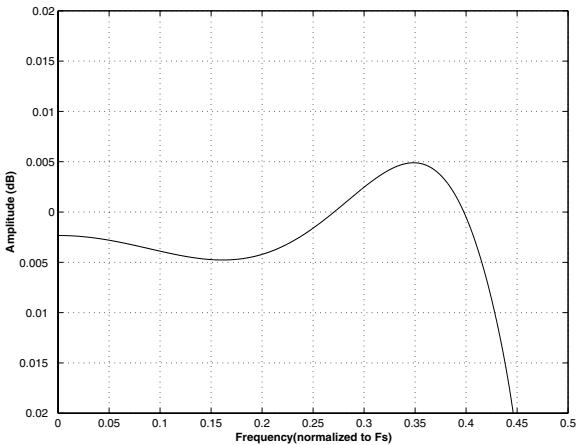


Figure 43. Double Speed (fast) Passband Ripple

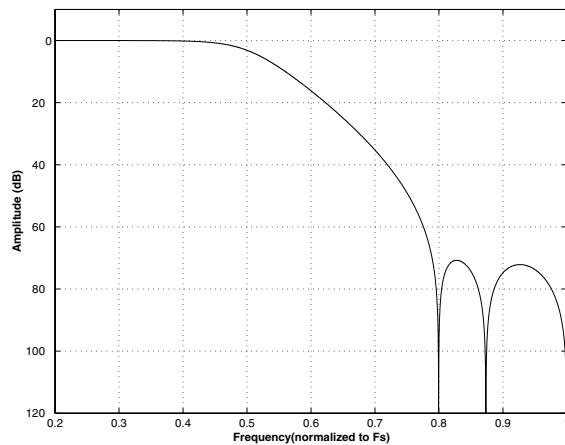


Figure 44. Double Speed (slow) Stopband Rejection

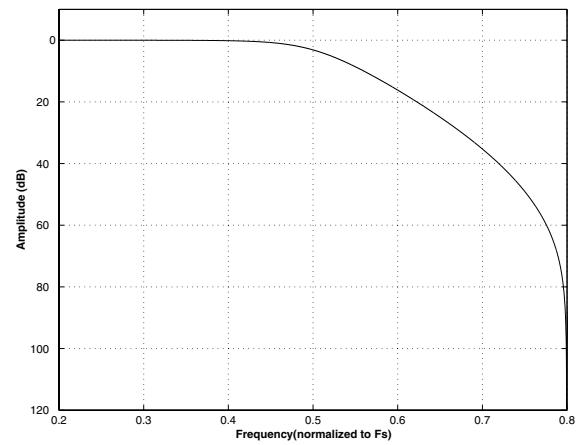


Figure 45. Double Speed (slow) Transition Band

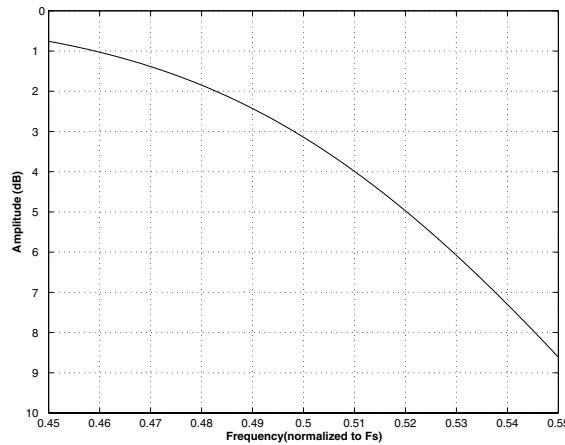


Figure 46. Double Speed (slow) Transition Band (detail)

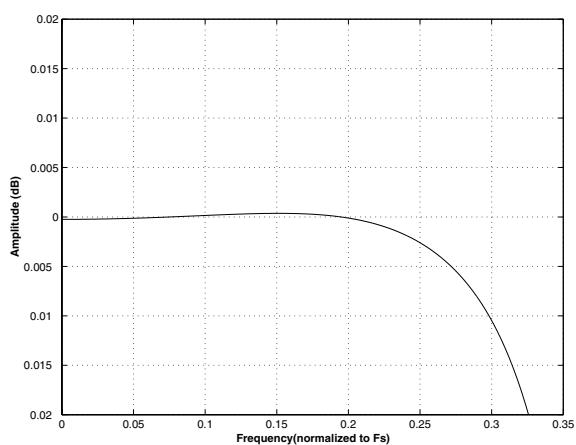


Figure 47. Double Speed (slow) Passband Ripple

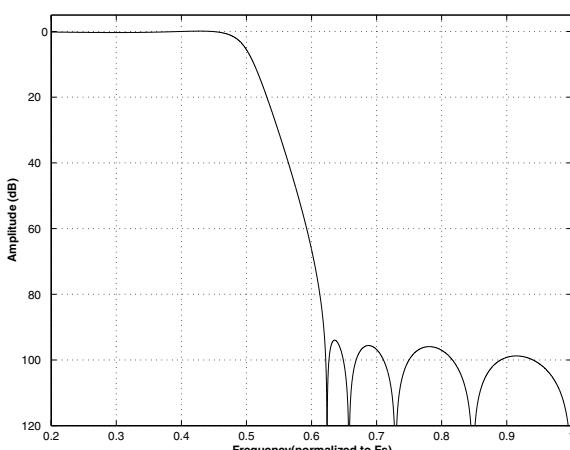


Figure 48. Quad Speed (fast) Stopband Rejection

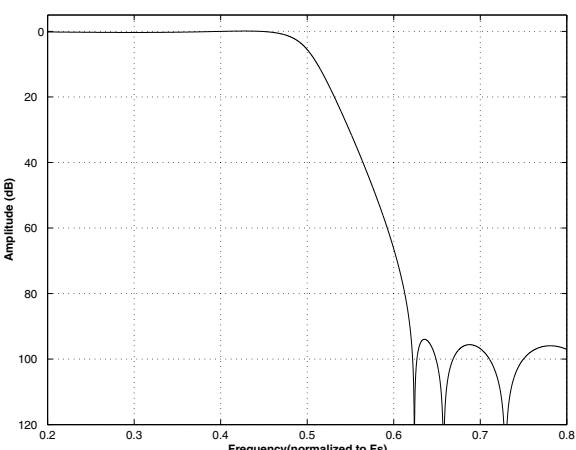


Figure 49. Quad Speed (fast) Transition Band

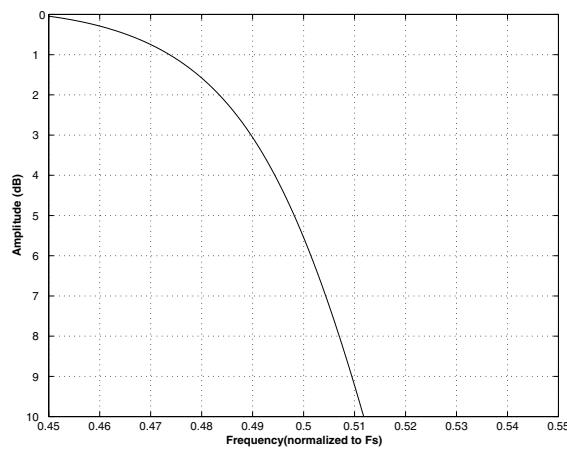


Figure 50. Quad Speed (fast) Transition Band (detail)

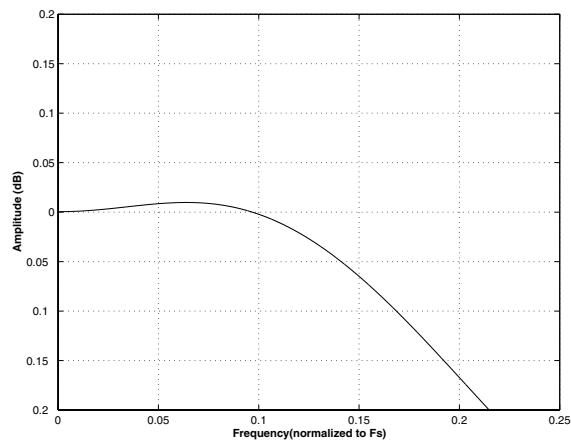


Figure 51. Quad Speed (fast) Passband Ripple

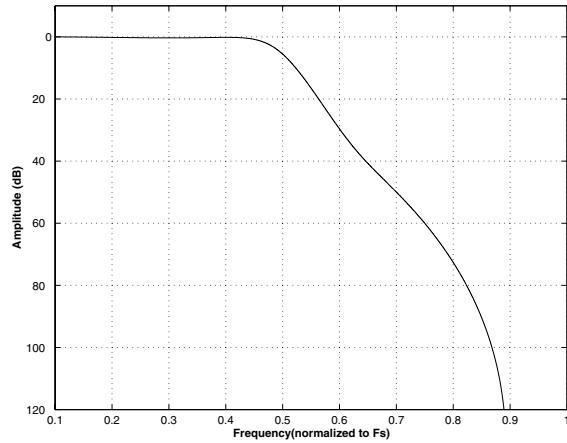


Figure 52. Quad Speed (slow) Stopband Rejection

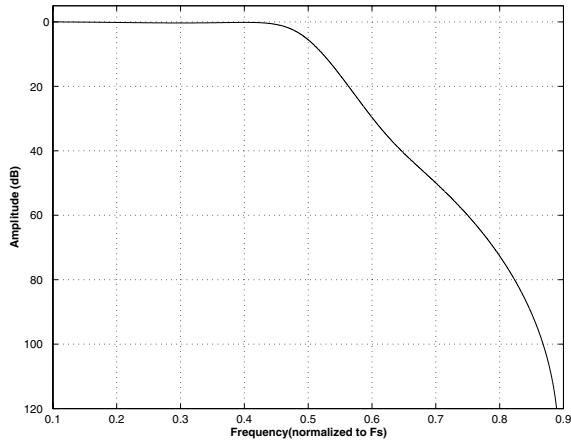


Figure 53. Quad Speed (slow) Transition Band

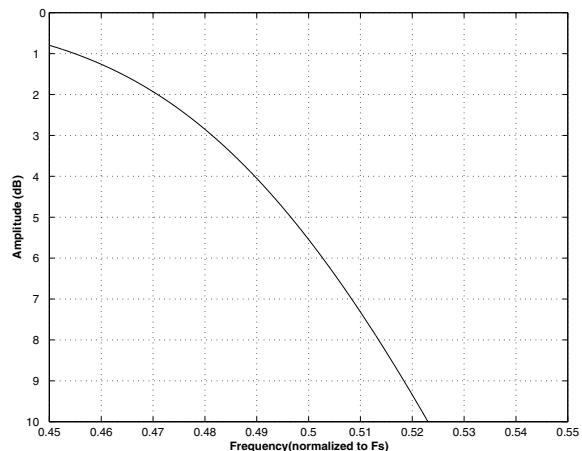


Figure 54. Quad Speed (slow) Transition Band (detail)

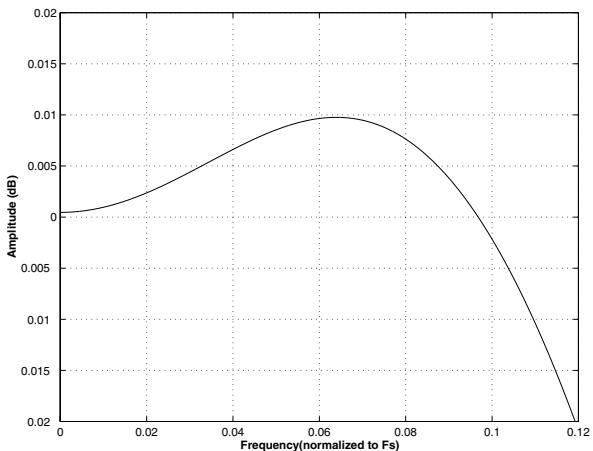


Figure 55. Quad Speed (slow) Passband Ripple

SWITCHING CHARACTERISTICS

(For CQ, $T_A = -10$ to $+70^\circ C$; For DQ, $T_A = -40$ to $+85^\circ C$;
 $V_A = 5 V$, $V_D = VLC = 3.3 V$, $VLS = 1.8 V$ to $5.25 V$; Inputs: Logic 0 = DGND, Logic 1 = VLS, $C_L = 30 pF$)

| Parameters | Symbol | Min | Typ | Max | Units |
|--|-------------|-----|-----|-----|--------|
| RST pin Low Pulse Width (Note 13) | | 1 | - | - | ms |
| PLL Clock Recovery Sample Rate Range | | 30 | - | 200 | kHz |
| RMCK output jitter (Note 15) | | - | 200 | - | ps RMS |
| RMCK output duty cycle | | 45 | 50 | 55 | % |
| OMCK Duty Cycle (Note 14) | | 40 | 50 | 60 | % |
| DAC_SCLK, ADC_SCLK Duty Cycle | | 45 | 50 | 55 | % |
| DAC_LRCK, ADC_LRCK Duty Cycle | | 45 | 50 | 55 | % |
| Master Mode | | | | | |
| RMCK to DAC_SCLK, ADC_SCLK active edge delay | t_{smd} | 0 | - | 10 | ns |
| RMCK to DAC_LRCK, ADC_LRCK delay | t_{lmd} | 0 | - | 10 | ns |
| Slave Mode | | | | | |
| DAC_SCLK, ADC_SCLK Falling Edge to ADC_SDOUT, ADC_SDOUT Output Valid | t_{dpd} | | - | 50 | ns |
| DAC_LRCK, ADC_LRCK Edge to MSB Valid | t_{lrd} | | - | 20 | ns |
| DAC_SDIN Setup Time Before DAC_SCLK Rising Edge | t_{ds} | | - | 10 | ns |
| DAC_SDIN Hold Time After DAC_SCLK Rising Edge | t_{dh} | | - | 30 | ns |
| DAC_SCLK, ADC_SCLK High Time | t_{sckh} | 20 | - | - | ns |
| DAC_SCLK, ADC_SCLK Low Time | t_{sckl} | 20 | - | - | ns |
| DAC_SCLK, ADC_SCLK rising to DAC_LRCK, SAI_LRCK Edge | t_{lrckd} | 25 | - | - | ns |
| DAC_LRCK, ADC_LRCK Edge to DAC_SCLK, ADC_SCLK Rising | t_{lrcks} | 25 | - | - | ns |

Notes: 13. After powering up the CS42426, RST should be held low after the power supplies and clocks are settled.
 14. See Table 2 on page 15 for suggested OMCK frequencies
 15. Limit the loading on RMCK to 1 CMOS load if operating above 24.576 MHz.

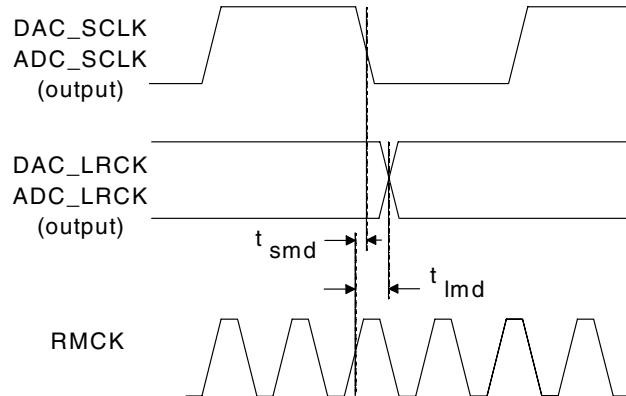


Figure 56. Serial Audio Port Master Mode Timing

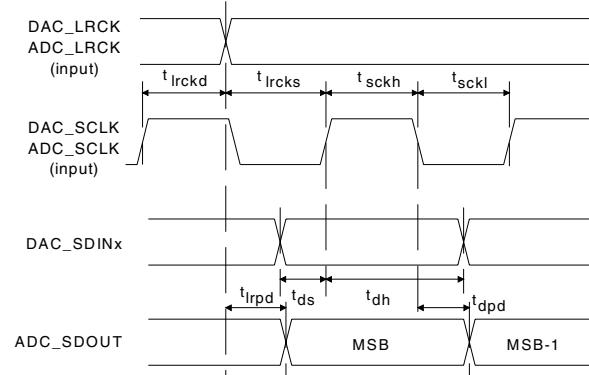


Figure 57. Serial Audio Port Slave Mode Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(For CQ, T_A = -10 to +70° C; For DQ, T_A = -40 to +85° C; V_A = 5 V, V_D = V_{LS} = 3.3 V; VLC = 1.8 V to 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

| Parameter | Symbol | Min | Max | Unit |
|--|-------------------|-----|-----------|------|
| SCL Clock Frequency | f _{scl} | - | 100 | kHz |
| RST Rising Edge to Start | t _{irs} | 500 | - | ns |
| Bus Free Time Between Transmissions | t _{buf} | 4.7 | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | t _{hdst} | 4.0 | - | μs |
| Clock Low time | t _{low} | 4.7 | - | μs |
| Clock High Time | t _{high} | 4.0 | - | μs |
| Setup Time for Repeated Start Condition | t _{sust} | 4.7 | - | μs |
| SDA Hold Time from SCL Falling (Note 16) | t _{hdd} | 0 | - | μs |
| SDA Setup time to SCL Rising | t _{sud} | 250 | - | ns |
| Rise Time of SCL and SDA | t _{rc} | - | 1 | μs |
| Fall Time SCL and SDA | t _{fc} | - | 300 | ns |
| Setup Time for Stop Condition | t _{susp} | 4.7 | - | μs |
| Acknowledge Delay from SCL Falling (Note 17) | t _{ack} | - | (Note 18) | ns |

Notes: 16. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

17. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.

18. $\frac{15}{256 \times F_s}$ for Single-Speed Mode, $\frac{15}{128 \times F_s}$ for Double-Speed Mode, $\frac{15}{64 \times F_s}$ for Quad-Speed Mode

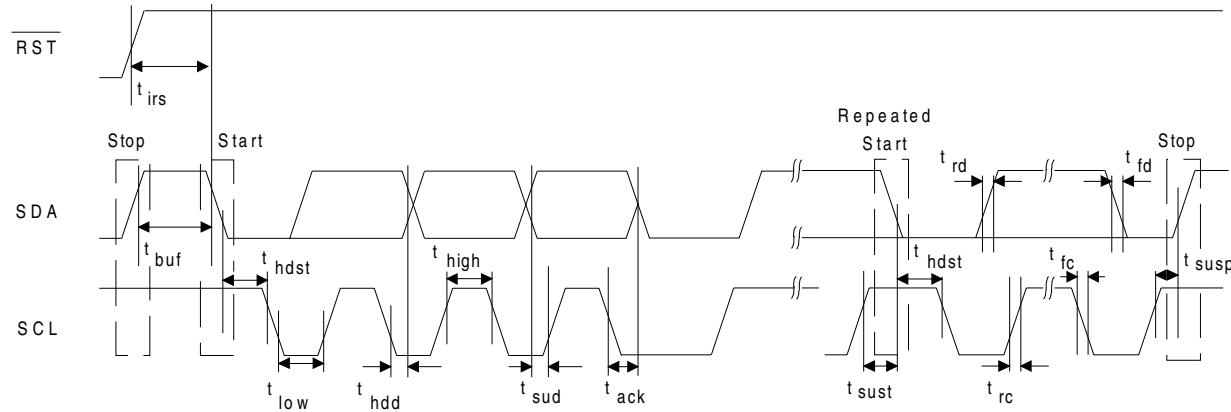


Figure 58. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(For CQ, $T_A = -10$ to $+70^\circ C$; For DQ, $T_A = -40$ to $+85^\circ C$; $VA = 5 V$, $VD = VLS = 3.3 V$; $VLC = 1.8 V$ to $5.25 V$;
Inputs: Logic 0 = DGND, Logic 1 = VLC, $C_L = 30 pF$)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|-----------|-----|-----|-----|---------|
| CCLK Clock Frequency (Note 19) | f_{sck} | 0 | - | 6.0 | MHz |
| CS High Time Between Transmissions | t_{csh} | 1.0 | - | - | μs |
| CS Falling to CCLK Edge | t_{css} | 20 | - | - | ns |
| CCLK Low Time | t_{scl} | 66 | - | - | ns |
| CCLK High Time | t_{sch} | 66 | - | - | ns |
| CDIN to CCLK Rising Setup Time | t_{dsu} | 40 | - | - | ns |
| CCLK Rising to DATA Hold Time (Note 20) | t_{dh} | 15 | - | - | ns |
| CCLK Falling to CDOUT Stable | t_{pd} | - | - | 50 | ns |
| Rise Time of CDOUT | t_{r1} | - | - | 25 | ns |
| Fall Time of CDOUT | t_{f1} | - | - | 25 | ns |
| Rise Time of CCLK and CDIN (Note 21) | t_{r2} | - | - | 100 | ns |
| Fall Time of CCLK and CDIN (Note 21) | t_{f2} | - | - | 100 | ns |

Notes: 19. If F_s is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128 F_s . This is dictated by the timing requirements necessary to access the Channel Status and User Bit buffer memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 8 kHz, so choosing CCLK to be less than or equal to 1.024 MHz should be safe for all possible conditions.

20. Data must be held for sufficient time to bridge the transition time of CCLK.

21. For $f_{sck} < 1$ MHz.

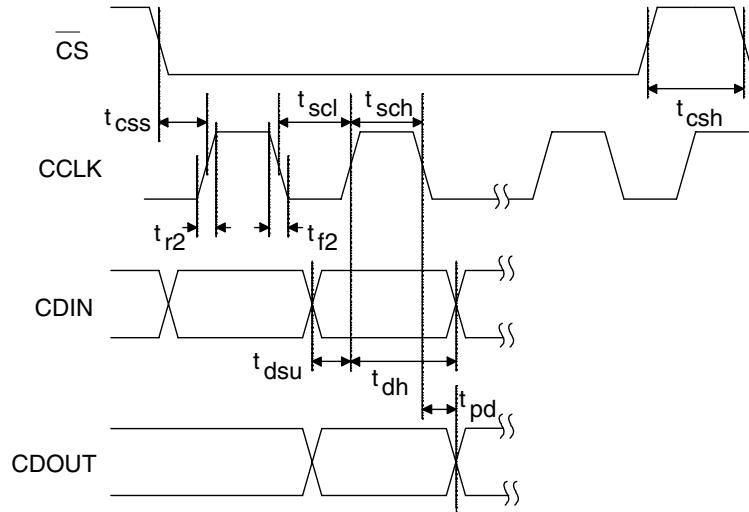


Figure 59. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ C$; AGND=DGND=0, all voltages with respect to ground; OMCK=12.288 MHz; Master Mode)

| Parameter | Symbol | Min | Typ | Max | Units | |
|---|----------|-----------|------------------------|------|---------|----|
| Power Supply Current (Note 22) | I_A | - | 90 | - | mA | |
| | I_D | - | 150 | - | mA | |
| | I_D | - | 100 | - | mA | |
| | I_{LC} | - | 250 | - | μA | |
| | I_{LS} | - | 250 | - | μA | |
| | I_{pd} | - | 250 | - | μA | |
| Power Consumption VA=5 V, VD=VLS=VLC=3.3 V | | (Note 22) | - | 780 | mW | |
| | | | normal operation | 1.25 | mW | |
| | | | power-down (Note 24) | - | mW | |
| | | | VA=5 V, VD=VLS=VLC=5 V | 950 | 1050 | mW |
| | | | normal operation | - | mW | |
| | | | power-down (Note 24) | 1.25 | - | mW |
| Power Supply Rejection Ratio (Note 25) | PSRR | - | 60 | - | dB | |
| | | (1 kHz) | - | 40 | dB | |
| | | (60 Hz) | - | - | | |

Notes: 22. Current consumption increases with increasing FS and increasing OMCK. Max values are based on highest FS and highest OMCK. Variance between speed modes is negligible.

23. I_{LC} measured with no external loading on the SDA pin.

24. Power down mode is defined as \overline{RST} pin = Low with all clock and data lines held static.

25. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure .

DIGITAL INTERFACE CHARACTERISTICS

(For CQ, $T_A = +25^\circ C$; For DQ, $T_A = -40$ to $+85^\circ C$)

| Parameters (Note 26) | Symbol | Min | Typ | Max | Units |
|--|----------|---------|-----|----------|---------|
| High-Level Input Voltage Serial Port Control Port | V_{IH} | 0.7xVLS | - | - | V |
| | | 0.7xVLC | - | - | V |
| Low-Level Input Voltage Serial Port Control Port | V_{IL} | - | - | 0.2xVLS | V |
| | | - | - | 0.2xVLC | V |
| High-Level Output Voltage at $I_o=2$ mA (Note 27) Serial Port Control Port MUTEC, GPOx | V_{OH} | VLS-1.0 | - | - | V |
| | | VLC-1.0 | - | - | V |
| | | VA-1.0 | - | - | V |
| Low-Level Output Voltage at $I_o=2$ mA (Note 27) Serial Port, Control Port, MUTEC, GPOx | V_{OL} | - | - | 0.4 | V |
| Input Leakage Current | I_{in} | - | - | ± 10 | μA |
| Input Capacitance | | - | 8 | - | pF |
| MUTEC Drive Current | | - | 3 | - | mA |

Notes: 26. Serial Port signals include: RMCK, OMCK, ADC_SCLK, ADC_LRCK, DAC_SCLK, DAC_LRCK, ADC_SDOUT, DAC_SDIN1-3 ADCIN1/2
Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/CS, AD1/CDIN, INT, \overline{RST}

27. When operating RMCK above 24.576 MHz, limit the loading on the signal to 1 CMOS load.

7 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

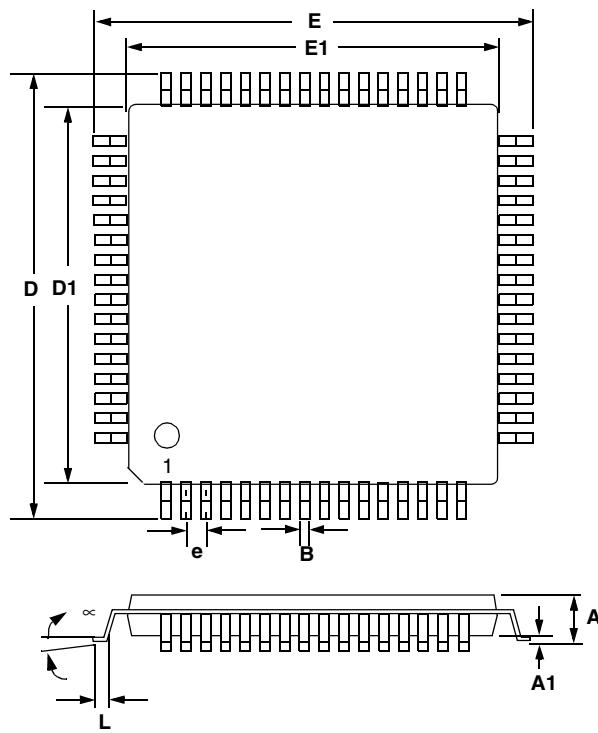
The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

8 REFERENCES

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- 7) Cirrus Logic, How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters, by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.
- 8) Cirrus Logic, A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range, by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
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9 PACKAGE DIMENSIONS

64L LQFP PACKAGE DRAWING



| DIM | INCHES | | | MILLIMETERS | | |
|-----|--------|-----------|--------|-------------|----------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | 0.55 | 0.063 | --- | 1.40 | 1.60 |
| A1 | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| B | 0.007 | 0.008 | 0.011 | 0.17 | 0.20 | 0.27 |
| D | 0.461 | 0.472 BSC | 0.484 | 11.70 | 12.0 BSC | 12.30 |
| D1 | 0.390 | 0.393 BSC | 0.398 | 9.90 | 10.0 BSC | 10.10 |
| E | 0.461 | 0.472 BSC | 0.484 | 11.70 | 12.0 BSC | 12.30 |
| E1 | 0.390 | 0.393 BSC | 0.398 | 9.90 | 10.0 BSC | 10.10 |
| e* | 0.016 | 0.020 BSC | 0.024 | 0.40 | 0.50 BSC | 0.60 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| ∞ | 0.000° | 4° | 7.000° | 0.00° | 4° | 7.00° |

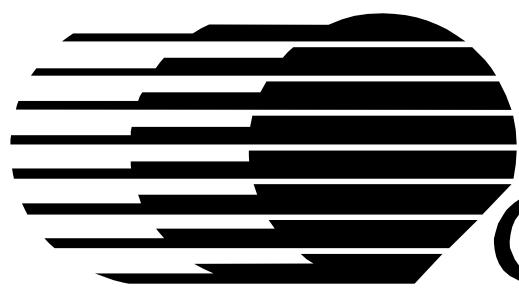
* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.

JEDEC Designation: MS022

THERMAL CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Units |
|---------------------------------------|---------------|-----|-----|------|---------|
| Allowable Junction Temperature | | - | - | +135 | °C |
| Junction to Ambient Thermal Impedance | θ_{JA} | - | 48 | - | °C/Watt |



CIRRUS LOGIC®