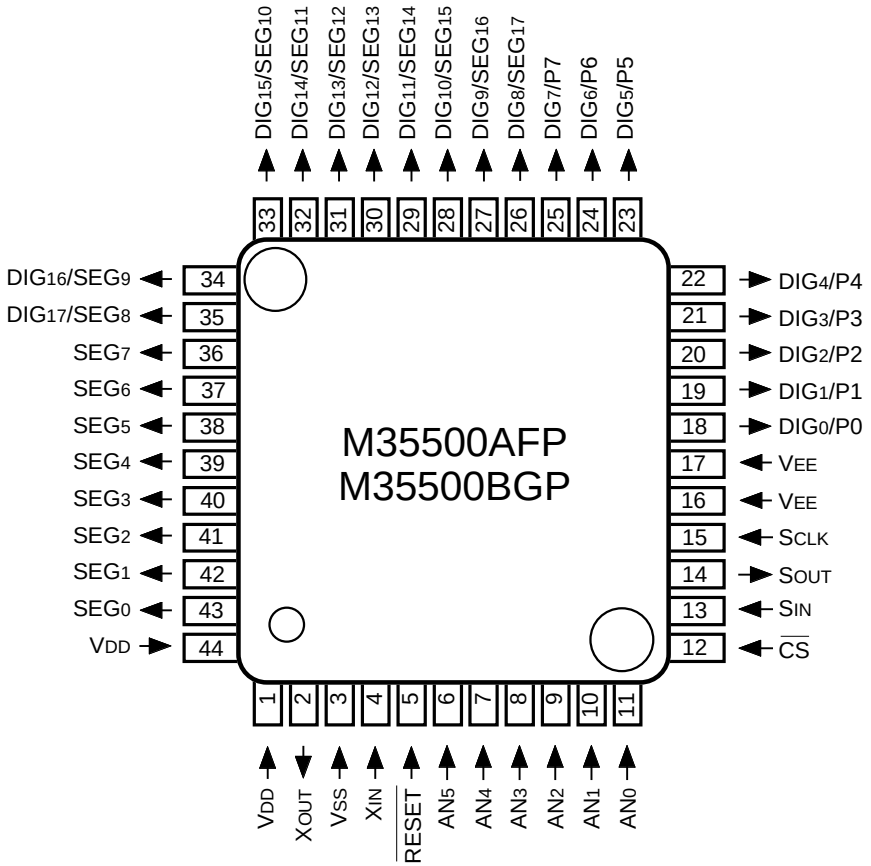
M35500AFP/BGP

FLD(VFD) CONTROLLER

DESCRIPTION/FEATURES

- High-breakdown-voltage output port 26
  - Segment output ..... 8 to 18
  - Digit output ..... 7 to 10
  - (Ports P0 to P7 are also used as ordinary output ports)
  - Output breakdown ..... Vcc – 45 V
  - Output current ..... –18 mA (DIG0 to DIG17), –7 mA (SEG0 to SEG7)
  - Pull-down resistor ..... build-in
  - Dimmer switch ..... 4 levels
- A-D converter ..... 8-bit × 6 channels
  - Absolute accuracy ..... ±3 LSB
- Serial I/O ..... 4 (CS controller, external clock)
  - Noise filter ..... build-in (in serial input pin and clock pin, 2 MHz sampling)
  - FLD display data ..... input
  - A-D conversion data ..... output
  - Command ..... input
- Package 44P6N/44P6X
- Oscillating circuit ..... RC oscillating cirucit (external capacitor)
  - Oscillating frequency ..... 4 MHz
- Power source voltage ..... 4.0 to 5.5 V

PIN CONFIGURATION (TOP VIEW)



Package type: 44P6N-A/44P6X

Fig. 1. Pin configuration of M35500AFP/BGP

FUNCTIONAL BLOCK

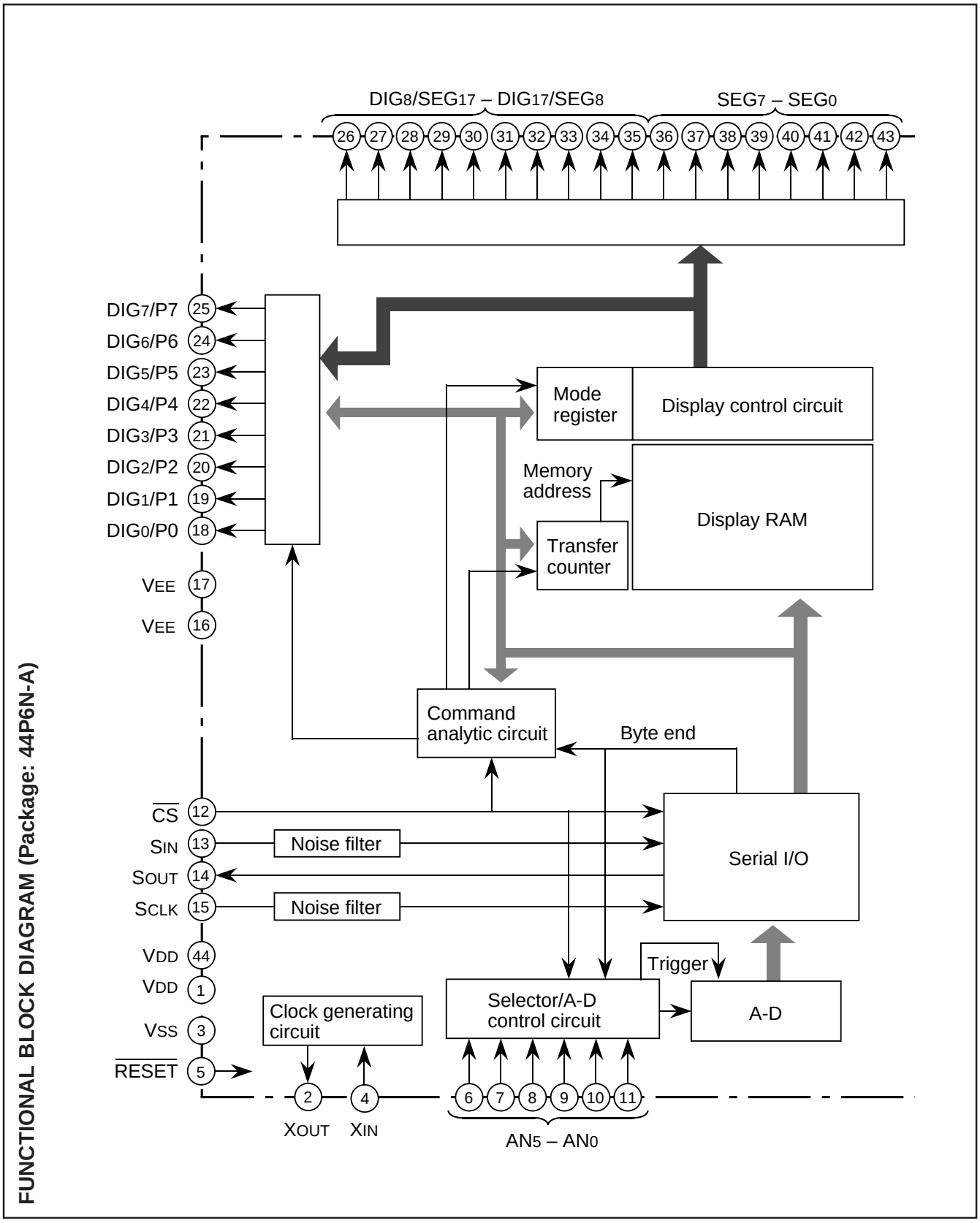


Fig. 2. Functional block diagram

PIN DESCRIPTION

Table. 1. Pin description

Pin	Name	Input	Output	Function
V_{CC}, V_{SS}	Power source			• Apply voltage of 5 V to V_{CC}, and 0 V to V_{SS}.
V_{EE}	Pull-down power source			• Applies voltage supplied to pull-down resistors.
X_{IN}	Clock input	Input		• RC oscillator pins for system clock.
X_{OUT}	Clock output		Output	
$\overline{RESET}$	$\overline{RESET}$ input	CMOS input		• Reset input pin for active “L”. • Internal pull-up resistors connected between the $\overline{RESET}$ and V_{CC} pins.
$\overline{CS}$	Chip select	CMOS input		• Serial transfer is possible by inputting “L” signal.
S_{CLK}	Serial clock	CMOS input Noise filter		• Clock for serial transfer is input. • Read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
S_{OUT}	Serial output		N-channel open-drain	• Serial data is output. • During reset it is in high-impedance state.
S_{IN}	Serial input	CMOS input Noise filter		• Serial data is input. • Read a clock twice with 2 MHz sampling clock and judge if it is a noise or not.
DIG_0/P0 – DIG_7/P7	Digit/Port		P-channel open-drain	• Pin for ordinary output or digit output. • At reset this port is set to V_{EE} level through a pull-down resistor.
DIG_8/SEG_{17} – DIG_{17}/SEG_8	Digit/Segment		P-channel open-drain	• Pin for digit output or segment output. • At reset this port is set to V_{EE} level through a pull-down resistor.
SEG_0 – SEG_7	Segment		P-channel open-drain	• Pin for segment output. • At reset this port is set to V_{EE} level through a pull-down resistor.

PORT BLOCK

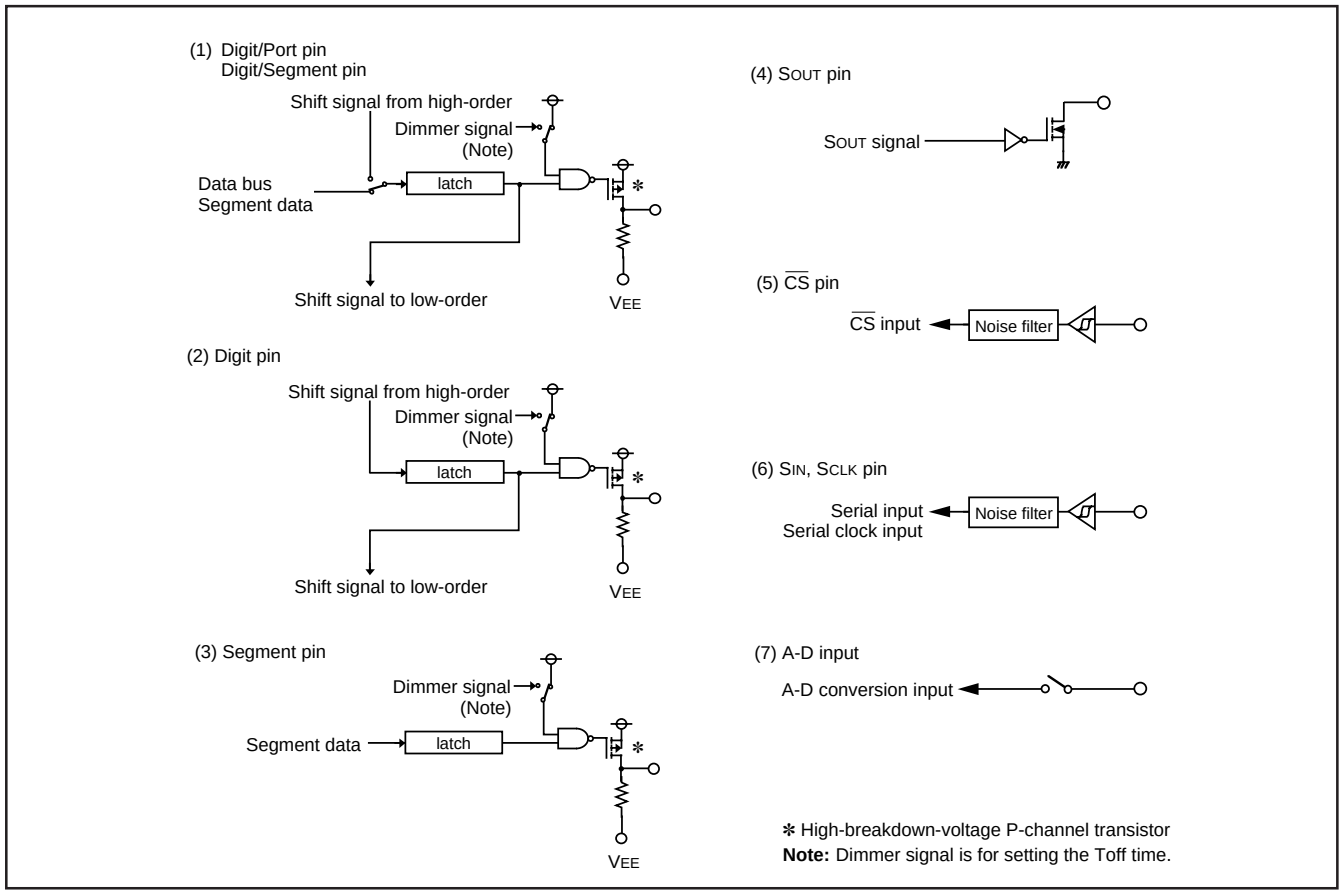
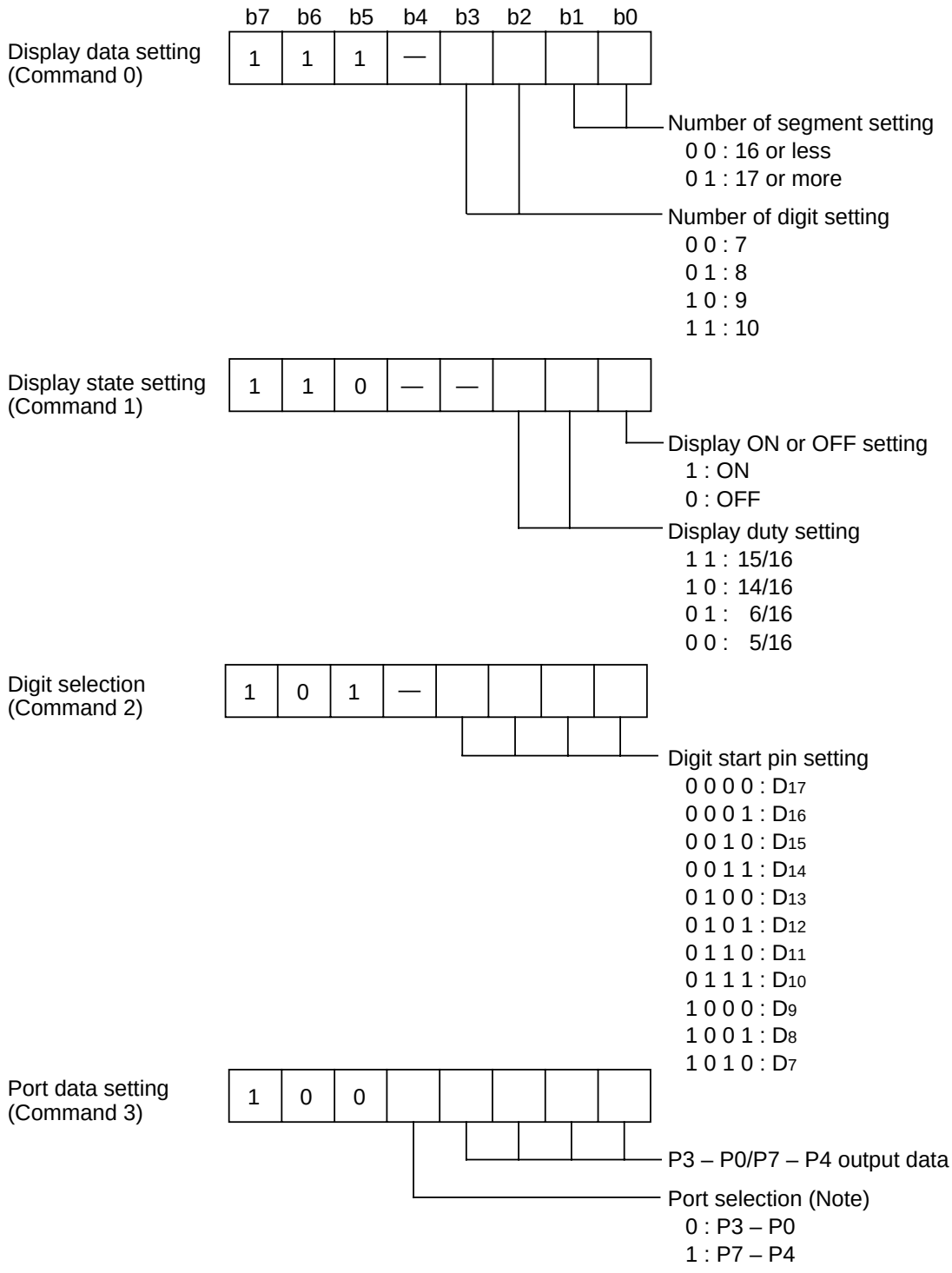


Fig. 3. Port block diagram

COMMAND STYLE

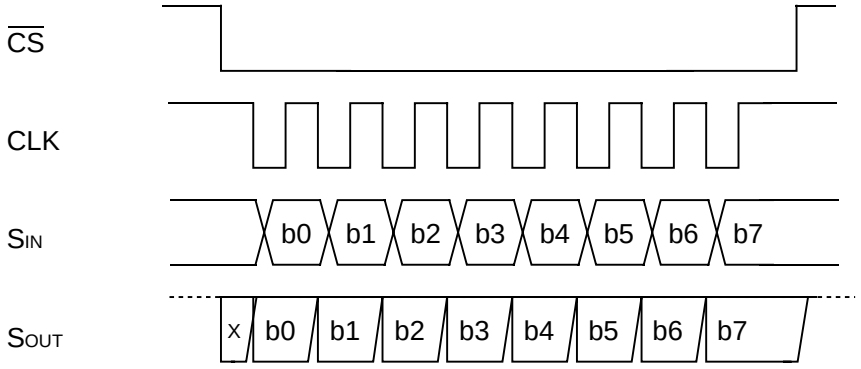


Note: When a digit or a port has to be selected, a digit output is selected for having higher priority.

Fig. 4. Command style

SERIAL I/O PROTOCOL

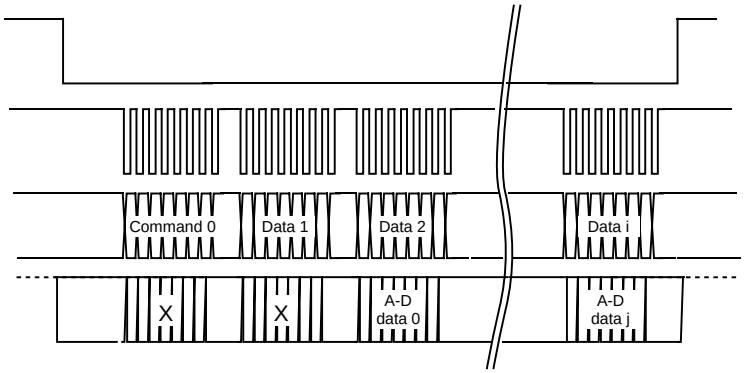
Byte protocol



Note: SOUT is in high-impedance state during CS signal is "H".

Command protocol

Display data setting (Command 0)



Note 1: The serial data which is transmitted after executing command 0 is recognized as a display data.
"A-D data 6 or more" data is defined as an undefined "X".

Note 2: Set the CS signal to "H" level after transferring a display data.

Other setting except display data setting (Command 1 to 3)

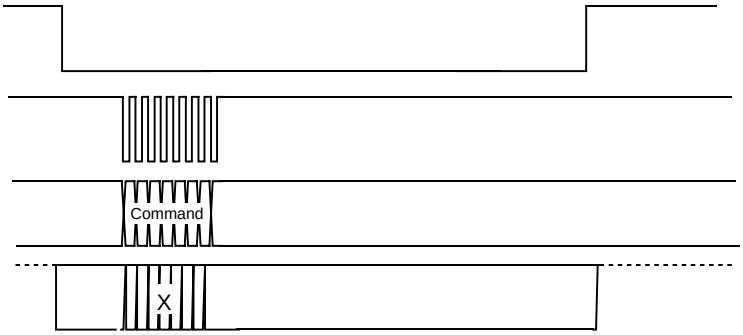
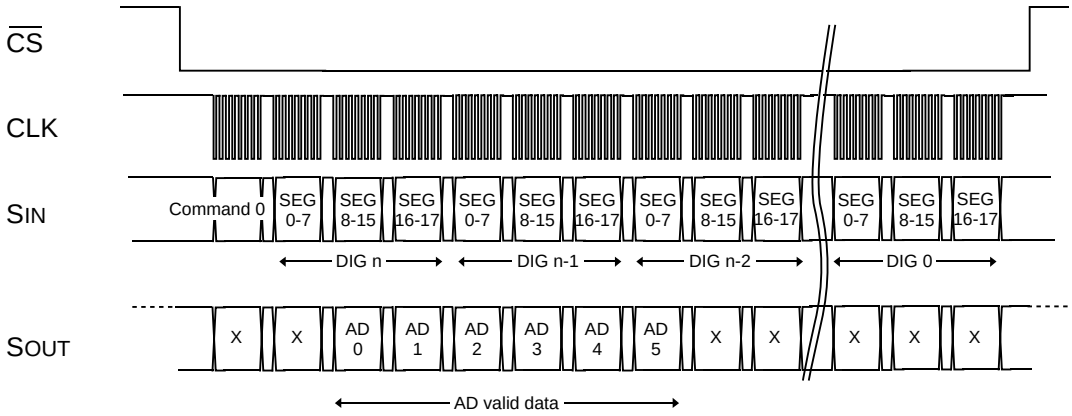


Fig. 5. Serial I/O protocol

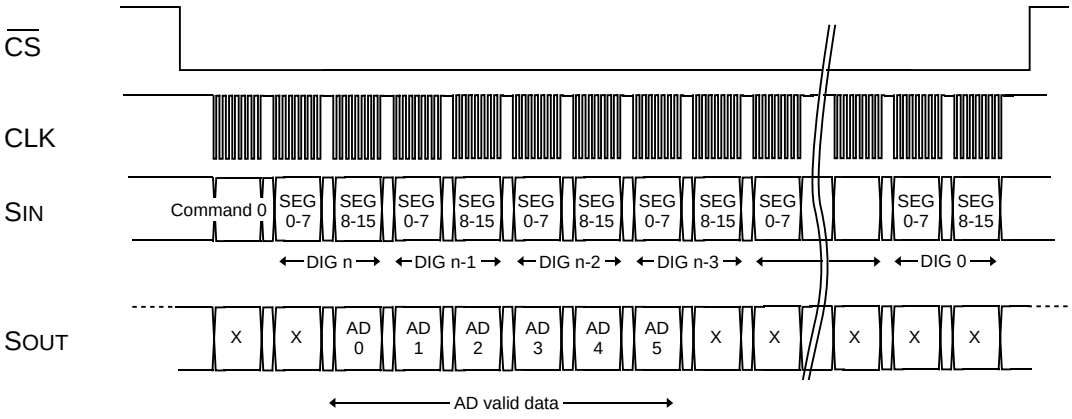
SERIAL COMMUNICATION FORMAT (DISPLAY DATA, A-D OUTPUT)

17 or more segments (3-byte transfer)



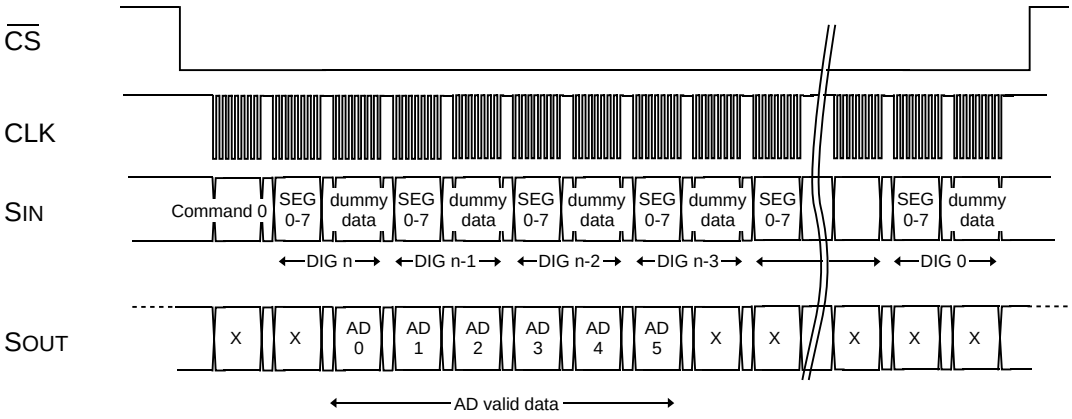
Note: 2 bytes "X" data is output before outputting AD valid data.

16 or less segments (2-byte transfer)



Note: 2 bytes "X" data is output before outputting AD valid data.

8 or less segments (2-byte transfer)



Note: 2 bytes "X" data is output before outputting AD valid data.

Fig. 6. Serial communication format

FLD DISPLAY TIMING

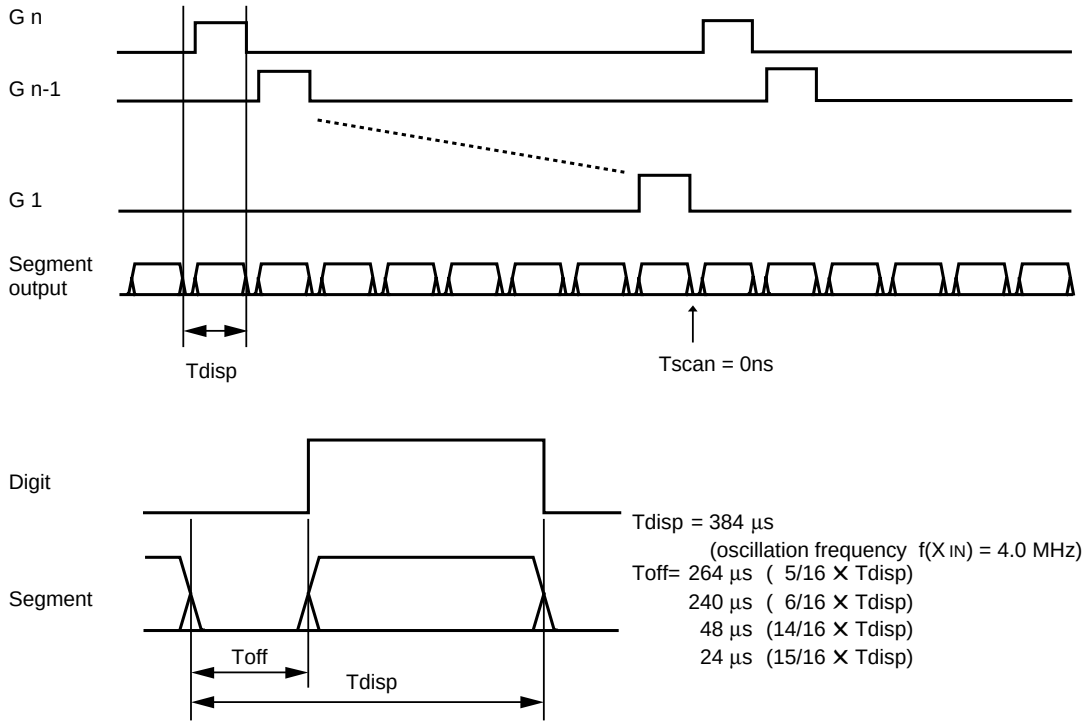


Fig. 7. FLD display timing diagram

SEGMENT/DIGIT SETTING EXAMPLE

	PORT	DIG	SEG	Grid : 7 Segment : 8	Grid : 10 Segment : 8	Grid : 10 Segment : 16	Grid : 7 Segment : 18
1			SEG_0	S1	S1	S1	S1
2			SEG_1	S2	S2	S2	S2
3			SEG_2	S3	S3	S3	S3
4			SEG_3	S4	S4	S4	S4
5			SEG_4	S5	S5	S5	S5
6			SEG_5	S6	S6	S6	S6
7			SEG_6	S7	S7	S7	S7
8			SEG_7	S8	S8	S8	S8
9		DIG_{17}	SEG_8	G7	G10	S9	S9
10		DIG_{16}	SEG_9	G6	G9	S10	S10
11		DIG_{15}	SEG_{10}	G5	G8	S11	S11
12		DIG_{14}	SEG_{11}	G4	G7	S12	S12
13		DIG_{13}	SEG_{12}	G3	G6	S13	S13
14		DIG_{12}	SEG_{13}	G2	G5	S14	S14
15		DIG_{11}	SEG_{14}	G1	G4	S15	S15
16		DIG_{10}	SEG_{15}		G3	S16	S16
17		DIG_9	SEG_{16}		G2	G10	S17
18		DIG_8	SEG_{17}		G1	G9	S18
19	P7	DIG_7				G8	G7
20	P6	DIG_6				G7	G6
21	P5	DIG_5				G6	G5
22	P4	DIG_4				G5	G4
23	P3	DIG_3				G4	G3
24	P2	DIG_2				G3	G2
25	P1	DIG_1				G2	G1
26	P0	DIG_0				G1	

Fig. 8. Segment/Digit setting example

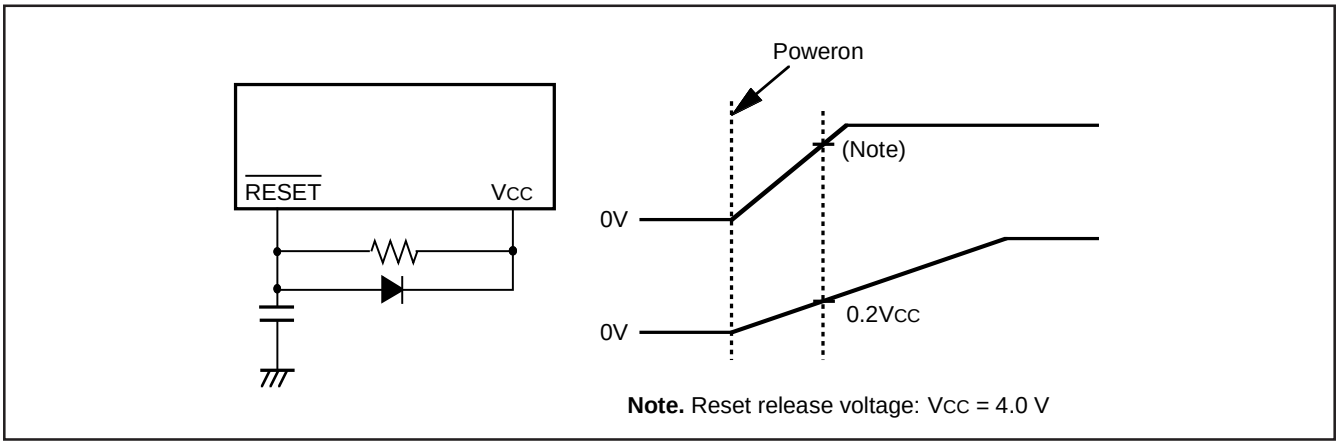
BIT ALLOCATION FOR DISPLAY RAM

ADDRESS	b7							b0	
09_{16}							SEG 17	SEG 16	Digit0
$0A_{16}$	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
$0B_{16}$	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
$0D_{16}$							SEG 17	SEG 16	Digit1
$0E_{16}$	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
$0F_{16}$	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
11_{16}							SEG 17	SEG 16	Digit2
12_{16}	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
13_{16}	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
15_{16}							SEG 17	SEG 16	Digit3
16_{16}	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
17_{16}	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
19_{16}							SEG 17	SEG 16	Digit4
$1A_{16}$	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
$1B_{16}$	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
$1D_{16}$							SEG 17	SEG 16	Digit5
$1E_{16}$	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
$1F_{16}$	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
21_{16}							SEG 17	SEG 16	Digit6
22_{16}	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
23_{16}	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
25_{16}							SEG 17	SEG 16	Digit7
26_{16}	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
27_{16}	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
29_{16}							SEG 17	SEG 16	Digit8
$2A_{16}$	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
$2B_{16}$	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	
$2D_{16}$							SEG 17	SEG 16	Digit9
$2E_{16}$	SEG 15	SEG 14	SEG 13	SEG 12	SEG 11	SEG 10	SEG 9	SEG 8	
$2F_{16}$	SEG 7	SEG 6	SEG 5	SEG 4	SEG 3	SEG 2	SEG 1	SEG 0	

Fig. 9. Bit allocation for display RAM

RESET CIRCUIT

To reset the controller, the $\overline{\text{RESET}}$ pin should be held at a “L” level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between 4.0 V and 5.5 V, and XIN oscillation is stable), reset is released.
Make sure that the reset input voltage is 0.5 V or less for 4.0 V of VCC.



Note. Reset release voltage: VCC = 4.0 V

Fig. 10. Reset circuit example

CLOCK GENERATING CIRCUIT

Oscillating circuit is built up by connecting pins XIN and XOUT as short as possible and connecting a capacitor between pins XIN (XOUT) and VSS.
When supplying a clock externally, input it to XIN pin and leave XOUT pin open.

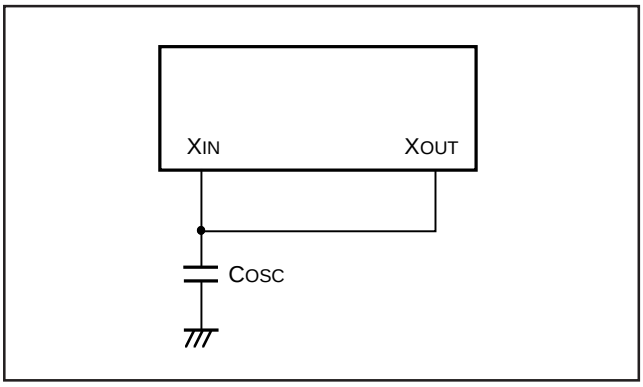


Fig. 11. RC generating circuit

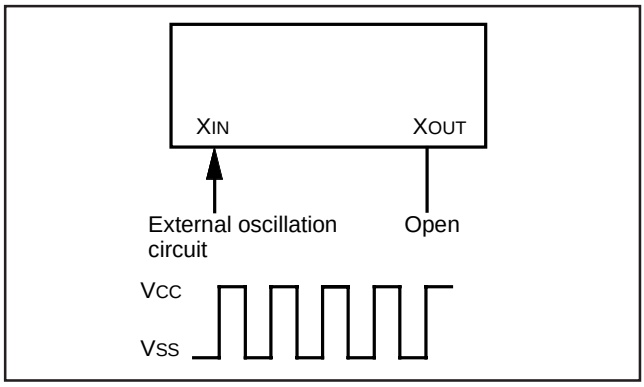


Fig. 12. External clock input circuit

HANDLING OF UNUSED PINS

Handle unused pins as the follow.

Table. 2. Handling of unused pins

Pin	Handling
Segment	Open
Digit	Open
Analog input	Connect to VCC or VSS through a resistor.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	• All voltage are based on V_{SS}. • Output transistors are cut off.	–0.3 to 7.0	V
V_{EE}	Pull-down power source voltage		V_{CC}–45 to V_{CC}+0.3	V
V_I	Input voltage AN_0 – AN_5		–0.3 to V_{CC}+0.3	V
V_I	Input voltage $\overline{CS}$, S_{IN}, S_{CLK}		–0.3 to V_{CC}+0.3	V
V_I	Input voltage $\overline{RESET}$		–0.3 to V_{CC}+0.3	V
V_O	Output voltage DIG_0 – DIG_{17}		V_{CC}–45 to V_{CC}+0.3	V
	SEG_0 – SEG_{17}	• All voltage are based on V_{SS}. • Output transistors are cut off. • A waveform: 450 μs or more frequency and 30 μs or less pulse width. • Connect only capacitor load (C_L = 200pF).	V_{CC}–50 to V_{CC}+0.3	
V_O	Output voltage S_{OUT}	• All voltage are based on V_{SS}. • Output transistors are cut off.	–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25 °C	600	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage	4.0	5.0	5.5	V
V_{SS}	Power source voltage		0		V
V_{EE}	Pull-down power source voltage	V_{CC}–38		V_{CC}	V
V_{IH}	"H" input voltage $\overline{CS}$, S_{IN}, S_{CLK}	0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $\overline{CS}$, S_{IN}, S_{CLK}	0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	DIG_0 – DIG_{17}, SEG_0 – SEG_{17} (Note 1)			–240	mA
$\Sigma I_{OH(avg)}$	"H" total peak output current	DIG_0 – DIG_{17}, SEG_0 – SEG_{17}			–120	mA
$I_{OH(peak)}$	"H" peak output current	DIG_0 – DIG_{17} (Note 2)			–40	mA
$I_{OH(peak)}$	"H" peak output current	SEG_0 – SEG_7 (Note 2)			–20	mA
$I_{OL(peak)}$	"L" peak output current	S_{OUT}			10	mA
$I_{OH(avg)}$	"H" peak output current	DIG_0 – DIG_{17} (Note 3)			–18	mA
$I_{OH(avg)}$	"H" peak output current	SEG_0 – SEG_7 (Note 3)			–7	mA
$I_{OL(avg)}$	"L" peak output current	S_{OUT}			5.0	mA
f(X_{IN})	Main clock input oscillation frequency	(Note 4)		4.0	5.2	MHz
f(S_{CLK})	Serial I/O external clock frequency			250		kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.
4: When the oscillation frequency has a 50 % duty cycle.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	DIG output	I_{OH} = –18 mA	V_{CC}–2.0			V
		SEG output	I_{OH} = –7 mA	V_{CC}–2.0			V
V_{OL}	"L" output voltage	S_{OUT}	I_{OL} = 5 mA			2.0	V
V_{T+} — V_{T-}	Hysteresis	S_{IN}, S_{CLK}, $\overline{CS}$	V_{CC} = 5.0 V		0.5		V
		$\overline{RESET}$, X_{IN}			0.5		V
I_{IH}	"H" input voltage	S_{IN}, S_{CLK}, $\overline{CS}$	V_I = V_{CC}			5.0	µA
		$\overline{RESET}$				5.0	µA
		X_{IN}			4.0		µA
I_{IL}	"L" input voltage	S_{IN}, S_{CLK}, $\overline{CS}$	V_I = V_{SS}			–5.0	µA
		$\overline{RESET}$			–150		µA
		X_{IN}			–4.0		µA
I_{LOAD}	Output load current	DIG_0 – DIG_{17} SEG_0 – SEG_{17}	V_{EE} = V_{CC}–36 V V_{OL} = V_{CC} Output transistors "off"	250	500	750	µA
I_{LEAK}	Output leakage current	DIG_0 – DIG_{17} SEG_0 – SEG_{17}	V_{EE} = V_{CC}–38 V V_{OL} = V_{CC}–38 V Output transistors "off"			–10	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{RAM}	RAM hold voltage	When clock is stopped	2.0		5.5	V
I_{CC}	Power source current	V_{CC} = 5 V, f(X_{IN}) = 4.2 MHz Output transistors "off" at A-D converter operating		0.5	1.0	mA

A-D CONVERTER CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	V_{CC} = 5.12 V			±3	LSB
T_{conv}	Conversion time				100	tc(X_{IN})
V_{IA}	Analog input voltage		0		V_{CC}	V
I_{IA}	Analog port input current			0.5	5.0	µA
R_{LADDER}	Ladder resistor			35		kΩ

TIMING REQUIREMENTS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(XIN)}$	Main clock input cycle time (X_{IN} input)	238			ns
$t_{wH(XIN)}$	Main clock input “H” pulse width	60			ns
$t_{wL(XIN)}$	Main clock input “L” pulse width	60			ns
$t_{c(SCLK)}$	Serial clock input cycle time (Note)	5			CLKs
$t_{wH(SCLK)}$	Serial clock input “H” pulse width (Note)	2			CLKs
$t_{wL(SCLK)}$	Serial clock input “L” pulse width (Note)	3			CLKs
$t_{su(SIN-SCLK)}$	Serial input setup time (Note)	2			CLKs
$t_{h(SCLK-SIN)}$	Serial input hold time (Note)	3			CLKs
$t_{su(\overline{CS})}$	Serial input setup time	50 $t_{c(XIN)}$			ns
$t_{h(\overline{CS})}$	Serial input hold time	50 $t_{c(XIN)}$			ns
$t_{re(SCLK)}$	Serial clock interval time	50 $t_{c(XIN)}$			ns

Note: The unit means a number of noise filter sampling clock (2 × $t_{c(XIN)}$).

SWITCHING CHARACTERISTICS (V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(SCLK-SOUT)}$	Serial I/O output delay time (Note 1)				3	CLKs
$t_{v(SCLK-SOUT)}$	Serial I/O output valid time		2		3	CLKs
$t_{r(Pch)}$	High-breakdown-voltage P-channel open-drain output rising time	C_L = 100pF V_{EE} = V_{CC}–36 V		1.8		µs
C_{OSC}	External capacitor size (Note 2)			22		pF

Note 1: The unit means a number of noise filter sampling clock (2 × $t_{c(XIN)}$).
2: An external capacitor size varies with a mounted condition.

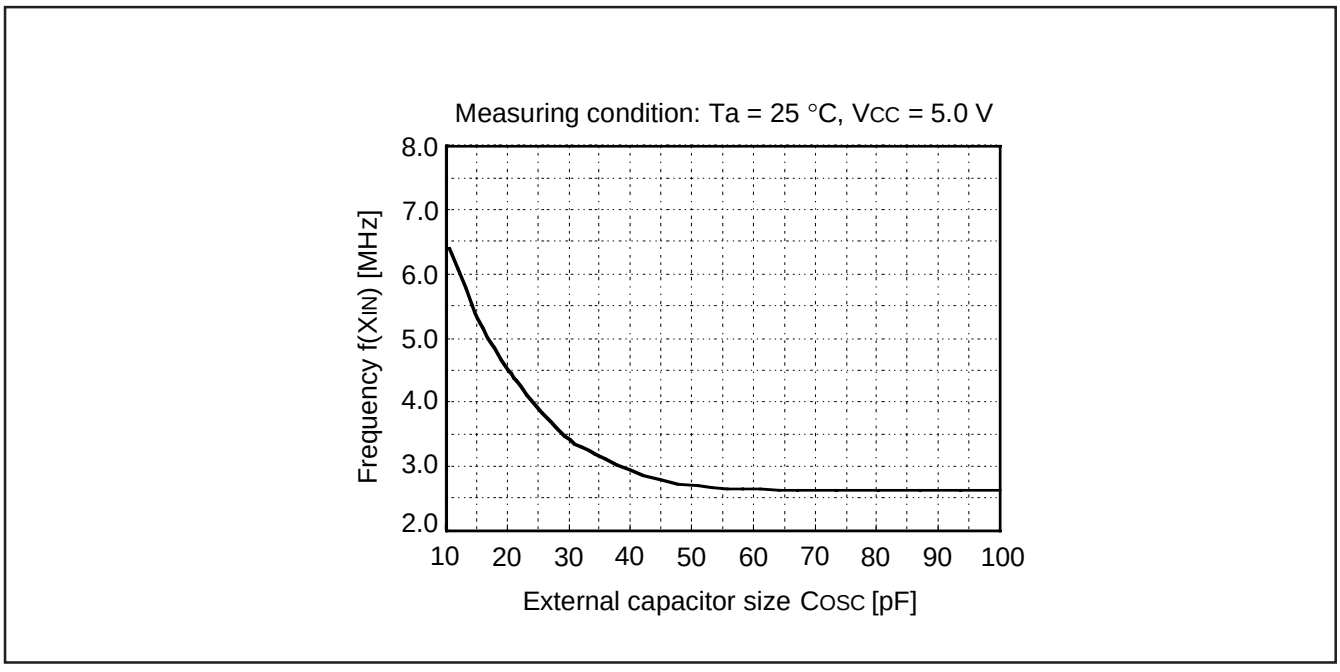


Fig. 13. Standard characteristic example of $f(X_{IN})$–C_{OSC}

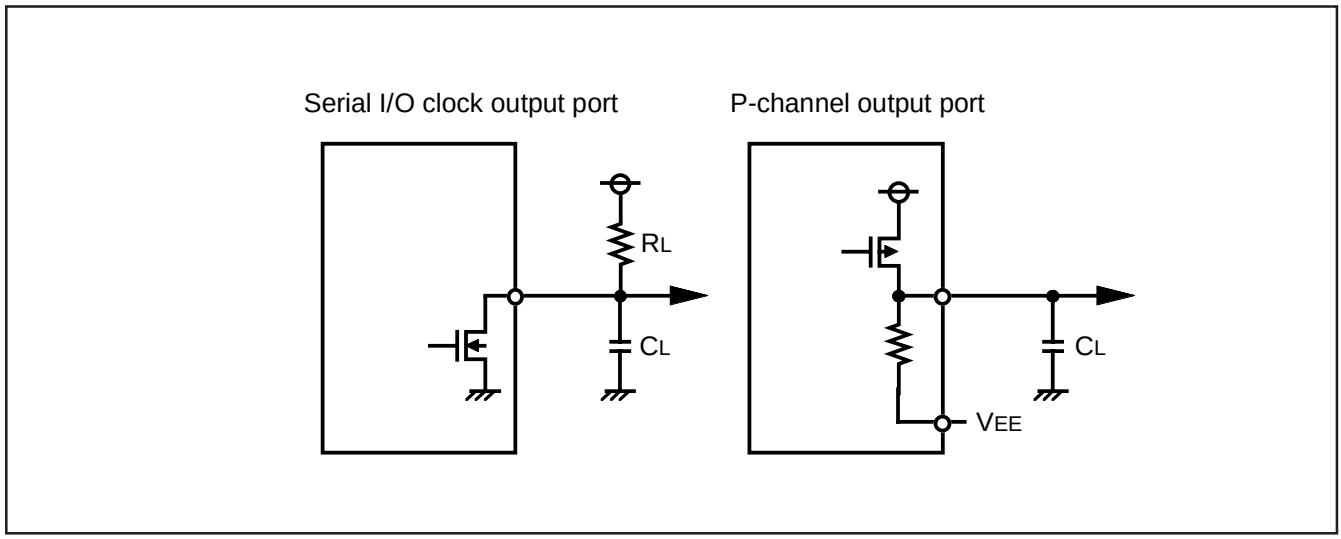


Fig. 14. Output switching characteristics measurement circuit diagram

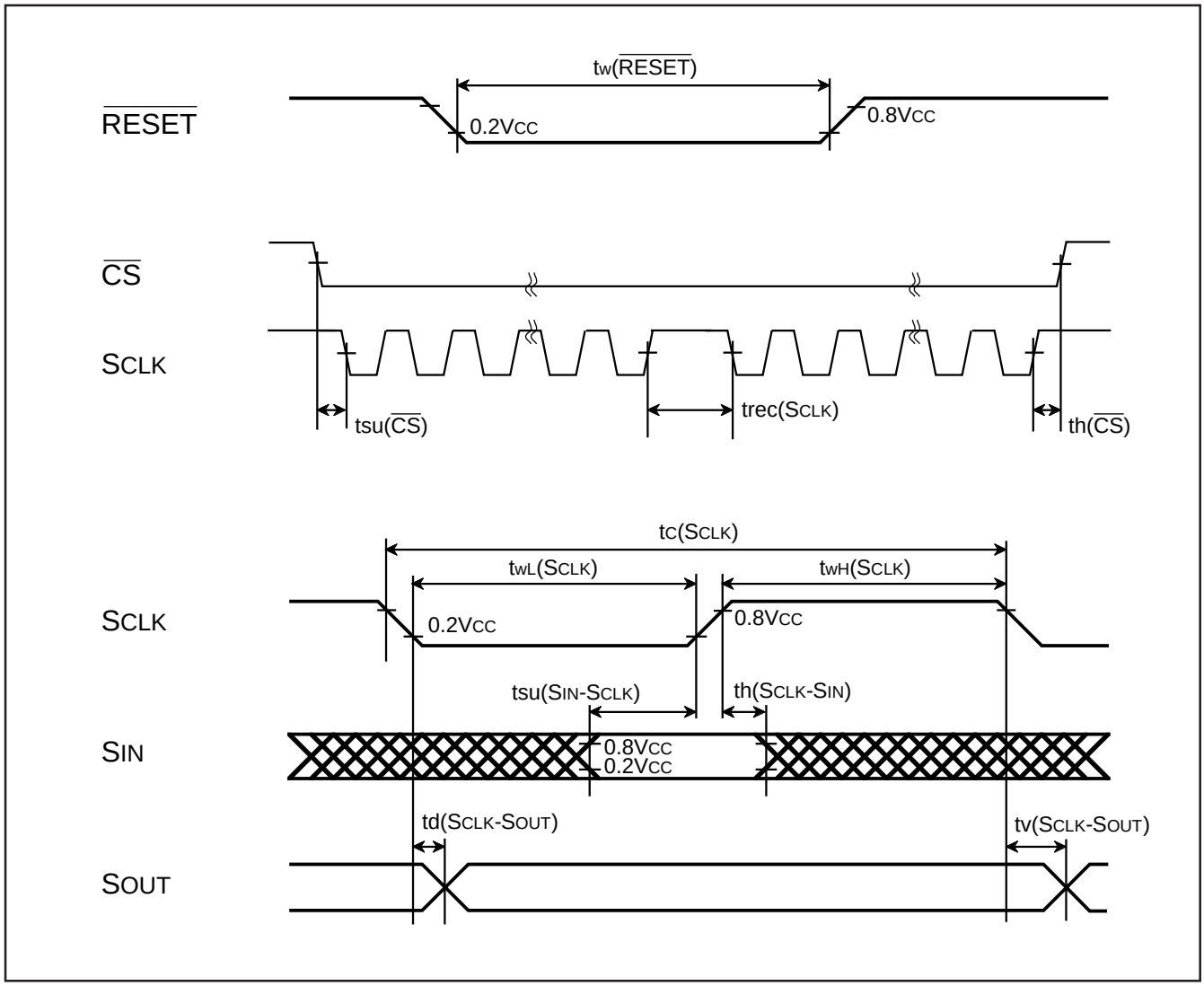


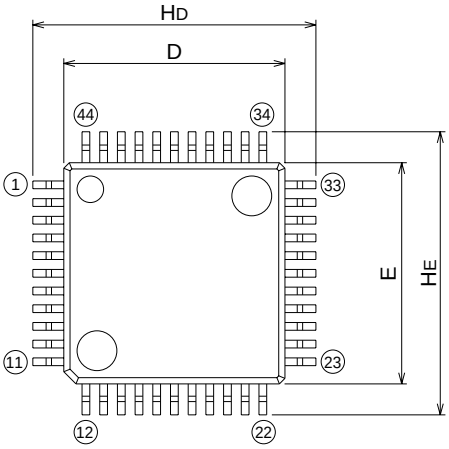
Fig. 15. Timing diagram

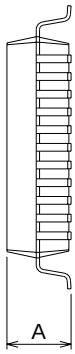
PACKAGE OUTLINE

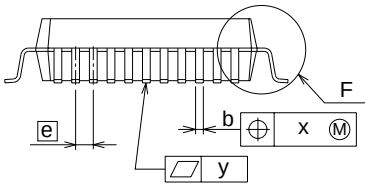
44P6N-A

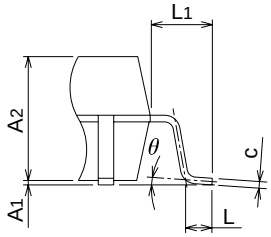
Plastic 44pin 10X10mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP44-P-1010-0.80	–	0.59	Alloy 42

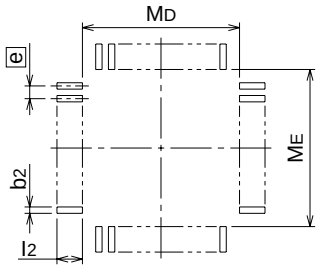








Detail F



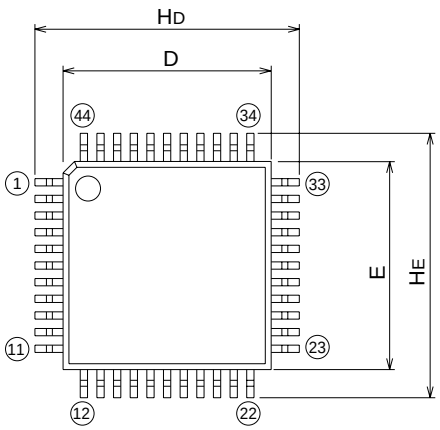
Recommended Mount Pad

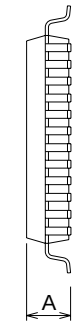
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	9.8	10.0	10.2
e	–	0.8	–
H_D	12.5	12.8	13.1
H_E	12.5	12.8	13.1
L	0.4	0.6	0.8
L_1	–	1.4	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
l_2	1.3	–	–
M_D	–	10.6	–
M_E	–	10.6	–

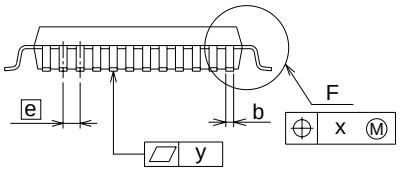
44P6X

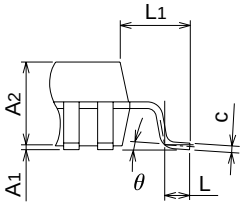
Plastic 44pin 10X10mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP44-P-1010-0.80	–	–	Cu Alloy

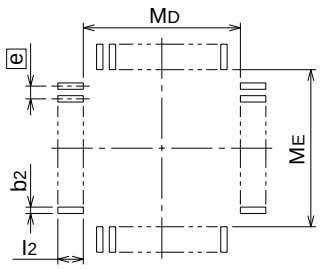








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.3
A1	0	0.1	0.2
A2	–	2.0	–
b	0.3	0.375	0.45
c	0.15	0.175	0.2
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	–	0.8	–
HD	12.5	12.8	13.1
HE	12.5	12.8	13.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
l2	1.3	–	–
MD	–	10.6	–
ME	–	10.6	–

MITSUBISHI ELECTRIC

REVISION HISTORY	M35500AFP/BGP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition; As M35500AFP/AGP	11/15/97
2.0	The followings are updated: Product M35500AGP is switched to M35500BGP. Page 1: Oscillating circuit.....RC oscillating... Page 3, Table 1: RC oscillator Page 9: Fig. 11. RC generating circuit Page 12, TIMING REQUIREMENTS: Limits of $t_{c(SCLK)}$ and $t_{WL(SCLK)}$ Page 12, SWITCHING CHARACTERISTICS: Limits and Unit of $t_{v(SCLK-SOUT)}$	01/07/00
2.1	Page 15: The 44P6X package outline is added.	03/09/00