

ISL2110, ISL2111

100V, 3A/4A Peak, High Frequency Half-Bridge Drivers

The [ISL2110](#), [ISL2111](#) are 100V, high frequency, half-bridge N-Channel power MOSFET driver ICs. They are based on the popular HIP2100, HIP2101 half-bridge drivers, but offer several performance improvements. Peak output pull-up/pull-down current has been increased to 3A/4A, which significantly reduces switching power losses and eliminates the need for external totem-pole buffers in many applications. Also, the low end of the V_{DD} operational supply range has been extended to 8VDC. The ISL2110 has additional input hysteresis for superior operation in noisy environments and the inputs of the ISL2111, like those of the ISL2110, can now safely swing to the V_{DD} supply rail.

Applications

- Telecom half-bridge DC/DC converters
- Telecom full-bridge DC/DC converters
- Two-switch forward converters
- Active-clamp forward converters
- Class-D audio amplifiers

Features

- Drives N-Channel MOSFET half-bridge
- SOIC, DFN, and TDFN package options
- SOIC, DFN, and TDFN packages compliant with 100V conductor spacing guidelines per IPC-2221
- Pb-free (RoHS compliant)
- Bootstrap supply max voltage to 114VDC
- On-chip 1W bootstrap diode
- Fast propagation times for multi-MHz circuits
- Drives 1nF load with typical rise/fall times of 9ns/7.5ns
- CMOS compatible input thresholds (ISL2110)
- 3.3V/TTL compatible input thresholds (ISL2111)
- Independent inputs provide flexibility
- No start-up problems
- Outputs unaffected by supply glitches, HS ringing below ground or HS slewing at high dv/dt
- Low power consumption
- Wide supply voltage range (8V to 14V)
- Supply undervoltage protection
- 1.6W/1W typical output pull-up/pull-down resistance

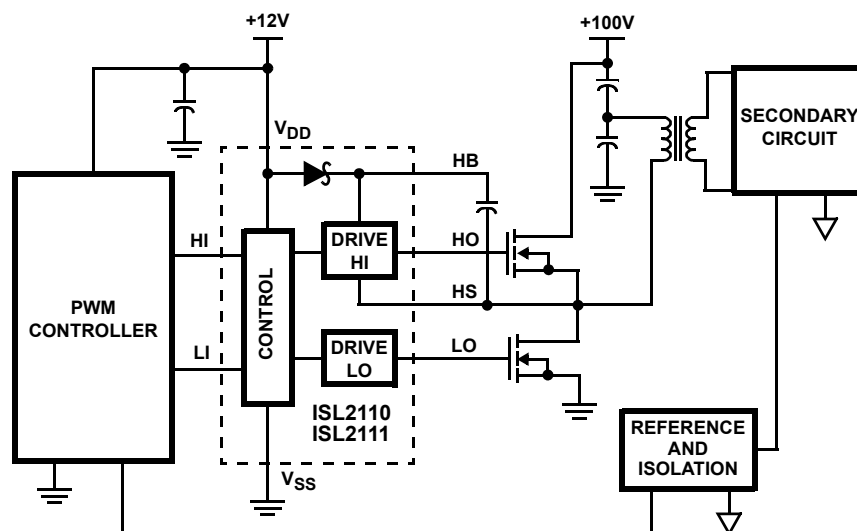
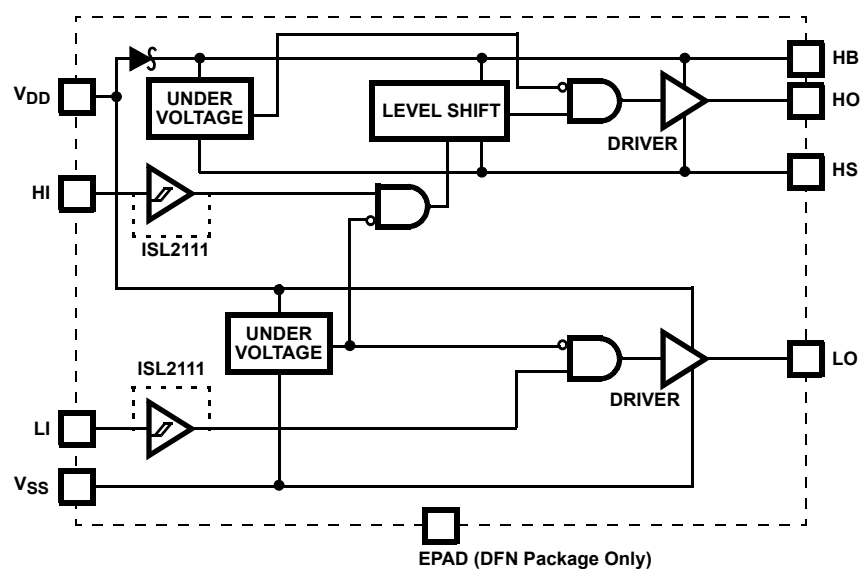


FIGURE 1. APPLICATION BLOCK DIAGRAM

Functional Block Diagram



*EPAD = Exposed Pad. The EPAD is electrically isolated from all other pins. For best thermal performance, connect the EPAD to the PCB power ground plane.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Application Diagrams

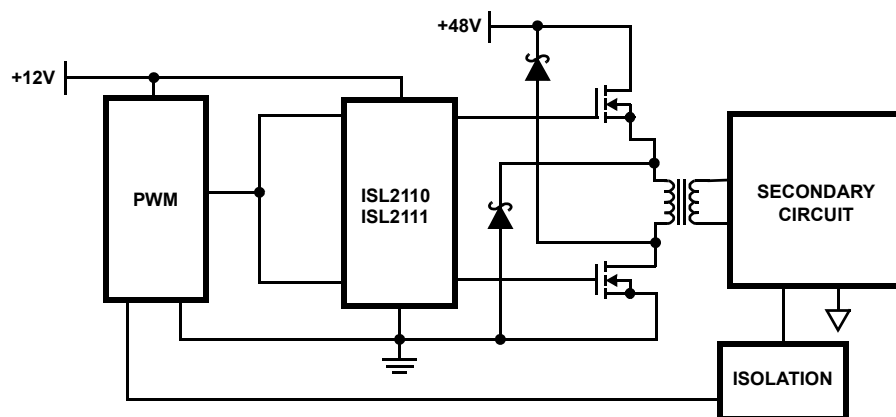


FIGURE 3. TWO-SWITCH FORWARD CONVERTER

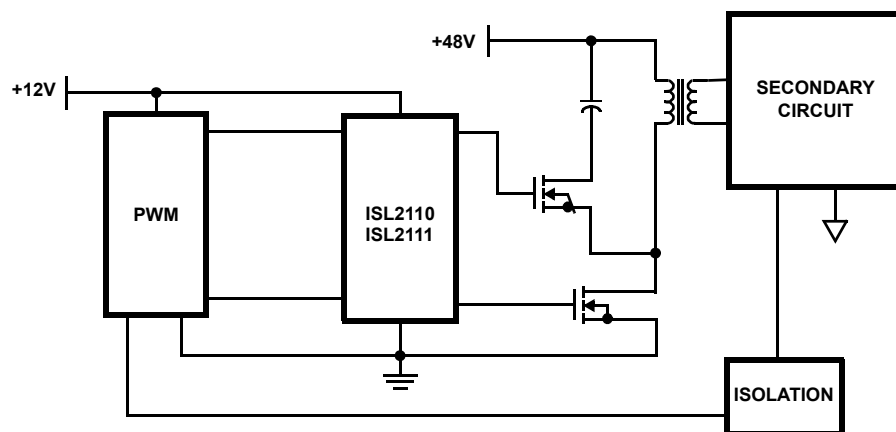


FIGURE 4. FORWARD CONVERTER WITH AN ACTIVE-CLAMP

Ordering Information

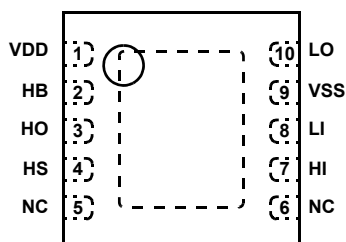
PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE DESCRIPTION (RoHS COMPLIANT)	PKG. DWG. #	CARRIER TYPE (Notes 1)	TEMP RANGE
ISL2110ABZ	2110 ABZ	8 Ld SOIC	M8.15	Tube	-40 to +125°C
ISL2110ABZ-T				Reel, 2.5k	
ISL2110AR4Z	211 0AR4Z	12 Ld 4x4 DFN	L12.4x4A	Tube	
ISL2110AR4Z-T				Reel, 6k	
ISL2111ABZ	2111 ABZ	8 Ld SOIC	M8.15	Tube	
ISL2111ABZ-T				Reel, 2.5k	
ISL2111AR4Z	211 1AR4Z	12 Ld 4x4 DFN	L12.4x4A	Tube	
ISL2111AR4Z-T				Reel, 6k	
ISL2111ARTZ	211 1ARTZ	10 Ld 4x4 TDFN	L10.4x4	Tube	
ISL2111ARTZ-T				Reel, 6k	
ISL2111BR4Z	211 1BR4Z	8 Ld 4x4 DFN	L8.4x4	Tube	
ISL2111BR4Z-T				Reel, 6k	

NOTES:

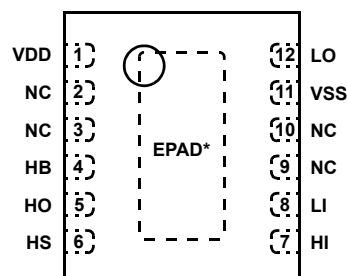
- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), please see device information page for [ISL2110](#), [ISL2111](#). For more information on MSL, see [TB363](#).

Pin Configurations

ISL2111ARTZ
(10 LD 4x4 TDFN)
TOP VIEW

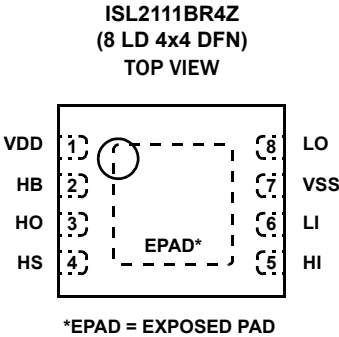
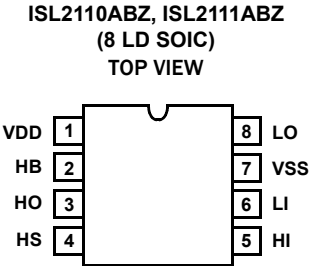


ISL2110AR4Z, ISL2111AR4Z
(12 LD 4x4 DFN)
TOP VIEW



*EPAD = EXPOSED PAD

Pin Configurations



Pin Descriptions

SYMBOL	DESCRIPTION
VDD	Positive supply to lower gate driver. Bypass this pin to VSS.
HB	High-side bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
HO	High-side output. Connect to gate of high-side power MOSFET.
HS	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	High-side input
LI	Low-side input
VSS	Chip negative supply, which will generally be ground.
LO	Low-side output. Connect to gate of low-side power MOSFET.
NC	No connect
EPAD	Exposed pad. Connect to ground or float. The EPAD is electrically isolated from all other pins.

Absolute Maximum Ratings

Supply Voltage, V_{DD} , V_{HB} - V_{HS} (Notes 4, 5)	0.3V to 18V
LI and HI Voltages (Note 5)	-0.3V to $V_{DD} + 0.3V$
Voltage on LO (Note 5)	-0.3V to $V_{DD} + 0.3V$
Voltage on HO relative to HS (Repetitive Transient < 100ns)	-2V
Voltage on LO relative to GND (Repetitive Transient < 100ns)	-2V
Voltage on HO (Note 5)	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
Voltage on HS (Continuous) (Note 5)	-1V to 110V
Voltage on HB (Note 5)	118V
Average Current in V_{DD} to HB Diode	100mA

Maximum Recommended Operating Conditions

Supply Voltage, V_{DD}	8V to 14V
Voltage on HS	-1V to 100V
Voltage on HS (Repetitive Transient < 100ns)	-5V to 105V
Voltage on HB	$V_{HS} + 7V$ to $V_{HS} + 14V$ and $V_{DD} - 1V$ to $V_{DD} + 100V$
HS Slew Rate	<50V/ns

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- The ISL2110 and ISL2111 are capable of derated operation at supply voltages exceeding 14V. Figure 24 shows the high-side voltage derating curve for this mode of operation.
- All voltages referenced to V_{SS} unless otherwise specified.
- θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
- For θ_{JC} , the "case temp" location is taken at the package top center.

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC (Notes 6, 9)	95	46
10 Ld TDFN (Notes 7, 8)	40	2.5
12 Ld DFN (Notes 7, 8)	39	2.5
8 Ld DFN (Notes 7, 8)	40	4.0
Max Power Dissipation at +25°C in Free Air		
8 Ld SOIC (Notes 6, 9)		1.3W
10 Ld TDFN (Notes 7, 8)		3.0W
12 Ld DFN (Notes 7, 8)		3.1W
8 Ld DFN (Notes 7, 8)		3.1W
Storage Temperature Range		-65°C to +150°C
Junction Temperature Range		-55°C to +150°C
Pb-Free Reflow Profile		see TB493

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, no load on LO or HO, unless otherwise specified.

PARAMETERS	SYMBOL	TEST CONDITIONS	T _J = +25°C			T _J = -40°C to +125°C		UNIT
			MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	MAX (Note 10)	
SUPPLY CURRENTS								
V _{DD} Quiescent Current	I _{DD}	ISL2110; LI = HI = 0V	-	0.10	0.25	-	0.30	mA
V _{DD} Quiescent Current	I _{DD}	ISL2111; LI = HI = 0V	-	0.30	0.45	-	0.55	mA
V _{DD} Operating Current	I _{DDO}	ISL2110; f = 500kHz	-	3.4	5.0	-	5.5	mA
V _{DD} Operating Current	I _{DDO}	ISL2111; f = 500kHz	-	3.5	5.0	-	5.5	mA
Total HB Quiescent Current	I _{HB}	LI = HI = 0V	-	0.10	0.15	-	0.20	mA
Total HB Operating Current	I _{HBO}	f = 500kHz	-	3.4	5.0	-	5.5	mA
HB to V _{SS} Current, Quiescent	I _{HBS}	LI = HI = 0V; V _{HB} = V _{HS} = 114V	-	0.05	1.50	-	10	μA
HB to V _{SS} Current, Operating	I _{HBSO}	f = 500kHz; V _{HB} = V _{HS} = 114V	-	1.2	-	-	-	mA
INPUT PINS								
Low Level Input Voltage Threshold	V _{IL}	ISL2110	3.7	4.4	-	3.5	-	V
Low Level Input Voltage Threshold	V _{IL}	ISL2111	1.4	1.8	-	1.2	-	V
High Level Input Voltage Threshold	V _{IH}	ISL2110	-	6.6	7.4	-	7.6	V
High Level Input Voltage Threshold	V _{IH}	ISL2111	-	1.8	2.2	-	2.4	V
Input Voltage Hysteresis	V _{IHYS}	ISL2110	-	2.2	-	-	-	V

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, no load on LO or HO, unless otherwise specified. (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^{\circ}C$			$T_J = -40^{\circ}C \text{ to } +125^{\circ}C$		UNIT
			MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	MAX (Note 10)	
Input Pull-Down Resistance	R_I		-	210	-	100	500	k Ω
UNDervoltage PROTECTION								
V_{DD} Rising Threshold	V_{DDR}		6.1	6.6	7.1	5.8	7.4	V
V_{DD} Threshold Hysteresis	V_{DDH}		-	0.6	-	-	-	V
HB Rising Threshold	V_{HBR}		5.5	6.1	6.8	5.0	7.1	V
HB Threshold Hysteresis	V_{HBH}		-	0.6	-	-	-	V
BOOTSTRAP DIODE								
Low Current Forward Voltage	V_{DL}	$I_{VDD-HB} = 100\mu A$	-	0.5	0.6	-	0.7	V
High Current Forward Voltage	V_{DH}	$I_{VDD-HB} = 100mA$	-	0.7	0.9	-	1	V
Dynamic Resistance	R_D	$I_{VDD-HB} = 100mA$	-	0.7	1	-	1.5	Ω
LO GATE DRIVER								
Low Level Output Voltage	V_{OLL}	$I_{LO} = 100mA$	-	0.1	0.18	-	0.25	V
High Level Output Voltage	V_{OHL}	$I_{LO} = -100mA$, $V_{OHL} = V_{DD} - V_{LO}$	-	0.16	0.23	-	0.3	V
Peak Pull-Up Current	I_{OHL}	$V_{LO} = 0V$	-	3	-	-	-	A
Peak Pull-Down Current	I_{OLL}	$V_{LO} = 12V$	-	4	-	-	-	A
HO GATE DRIVER								
Low Level Output Voltage	V_{OLH}	$I_{HO} = 100mA$	-	0.1	0.18	-	0.25	V
High Level Output Voltage	V_{OHH}	$I_{HO} = -100mA$, $V_{OHH} = V_{HB} - V_{HO}$	-	0.16	0.23	-	0.3	V
Peak Pull-Up Current	I_{OHH}	$V_{HO} = 0V$	-	3	-	-	-	A
Peak Pull-Down Current	I_{OLH}	$V_{HO} = 12V$	-	4	-	-	-	A

Switching Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, unless otherwise specified.

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^{\circ}C$			$T_J = -40^{\circ}C \text{ to } +125^{\circ}C$		UNIT
			MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	MAX (Note 10)	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	32	50	-	60	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	32	50	-	60	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	39	50	-	60	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	38	50	-	60	ns
Delay Matching: Upper Turn-Off to Lower Turn-On	t_{MON}		1	8	-	-	16	ns
Delay Matching: Lower Turn-Off to Upper Turn-On	t_{MOFF}		1	6	-	-	16	ns
Either Output Rise Time (10% to 90%)	t_{RC}	$C_L = 1nF$	-	9	-	-	-	ns
Either Output Fall Time (90% to 10%)	t_{FC}	$C_L = 1nF$	-	7.5	-	-	-	ns
Either Output Rise Time (3V to 9V)	t_R	$C_L = 0.1\mu F$	-	0.3	0.4	-	0.5	μs
Either Output Fall Time (9V to 3V)	t_F	$C_L = 0.1\mu F$	-	0.19	0.3	-	0.4	μs
Minimum Input Pulse Width that Changes the Output	t_{PW}		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	-	-	ns

NOTE:

10. Parameters with MIN and/or MAX limits are 100% tested at $+25^{\circ}C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Timing Diagrams

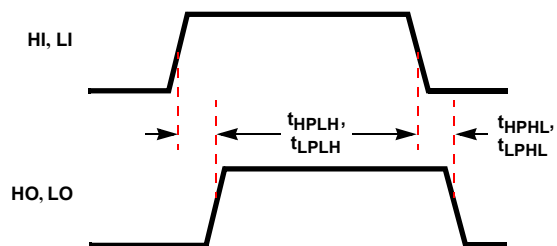


FIGURE 5. PROPAGATION DELAYS

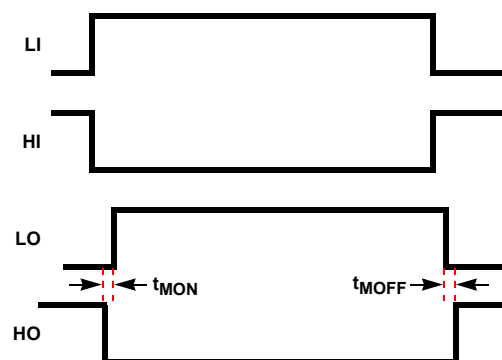


FIGURE 6. DELAY MATCHING

Typical Performance Curves

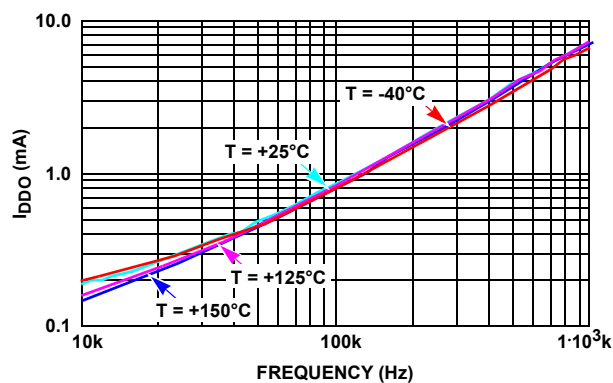
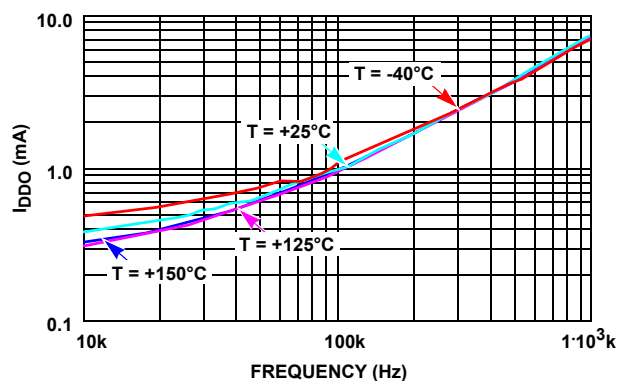
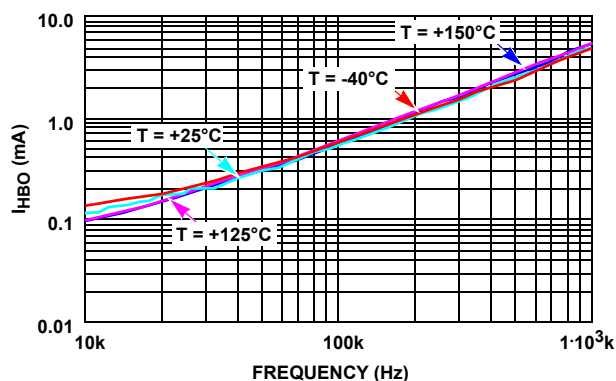
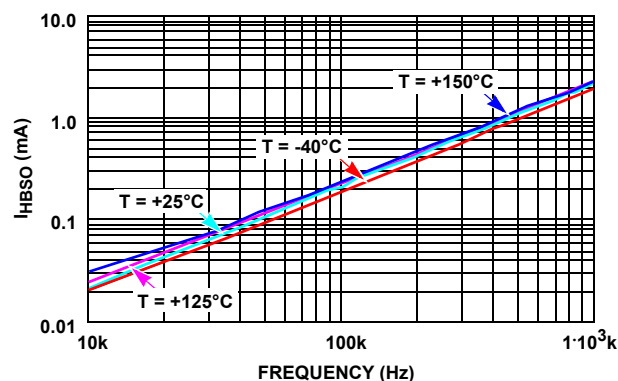
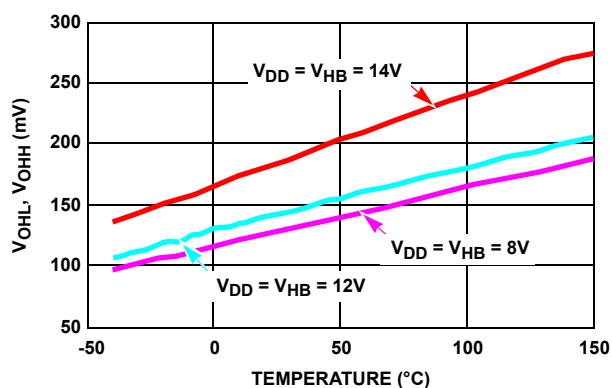
FIGURE 7. ISL2110 I_{DD} OPERATING CURRENT vs FREQUENCYFIGURE 8. ISL2111 I_{DD} OPERATING CURRENT vs FREQUENCYFIGURE 9. I_{HB} OPERATING CURRENT vs FREQUENCYFIGURE 10. I_{HBS} OPERATING CURRENT vs FREQUENCY

FIGURE 11. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

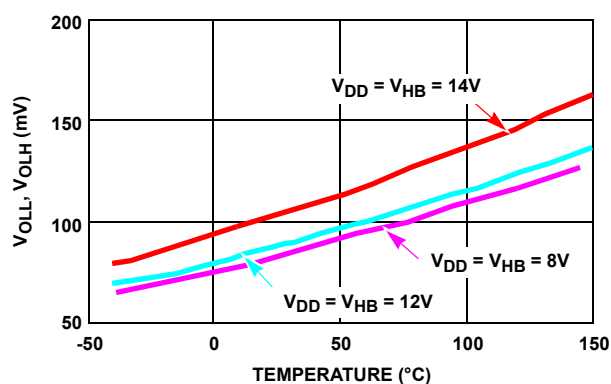


FIGURE 12. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

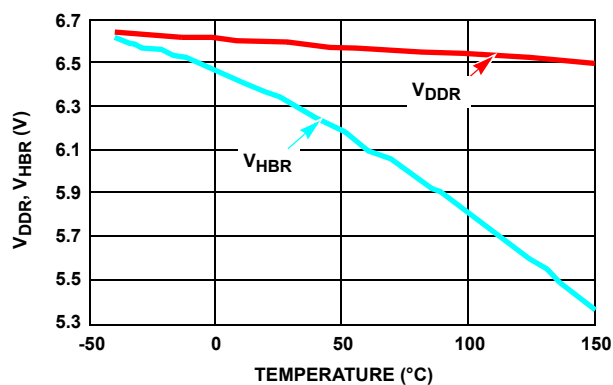


FIGURE 13. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

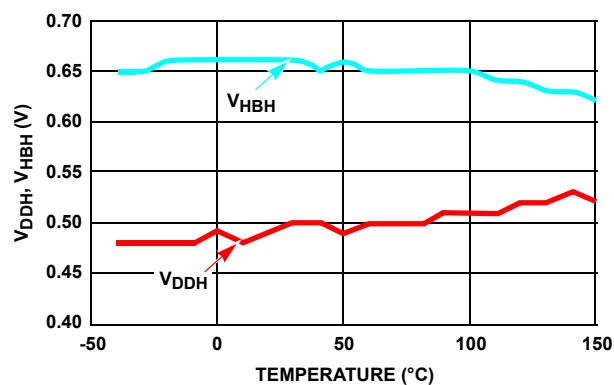


FIGURE 14. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

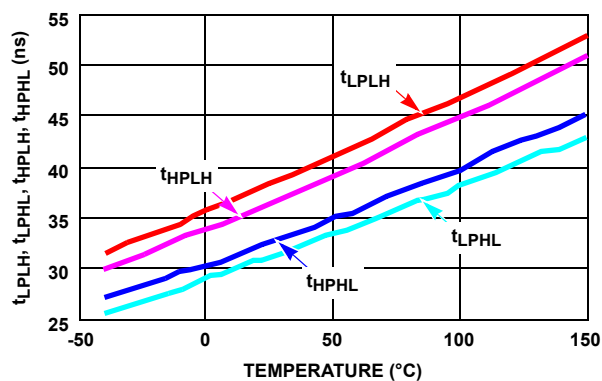


FIGURE 15. ISL2110 PROPAGATION DELAYS vs TEMPERATURE

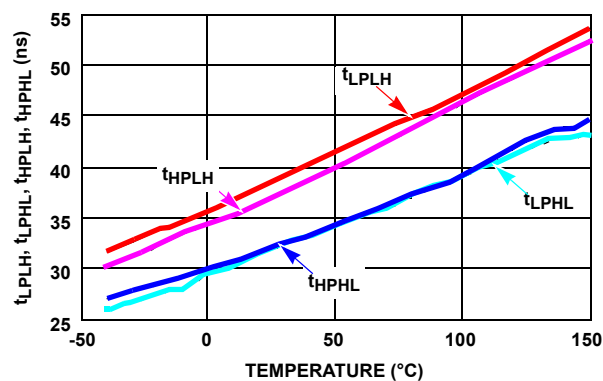


FIGURE 16. ISL2111 PROPAGATION DELAYS vs TEMPERATURE

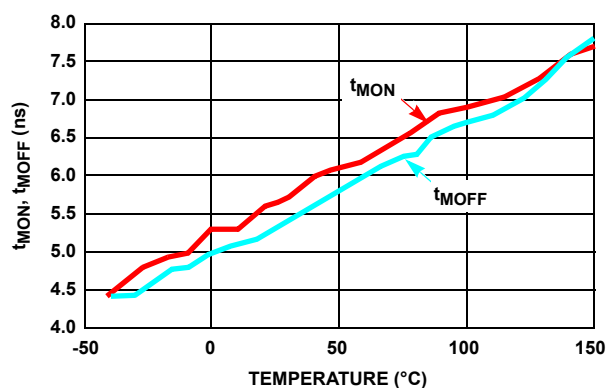


FIGURE 17. ISL2110 DELAY MATCHING vs TEMPERATURE

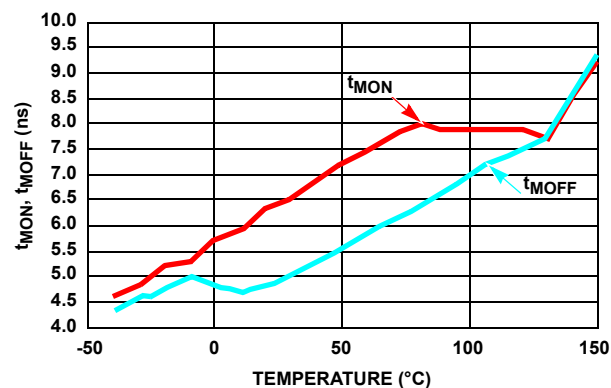


FIGURE 18. ISL2111 DELAY MATCHING vs TEMPERATURE

Typical Performance Curves (Continued)

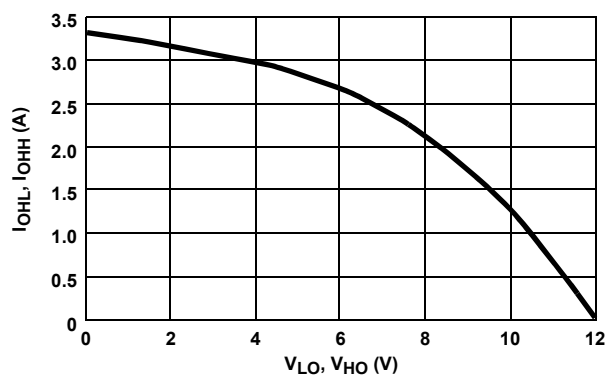


FIGURE 19. PEAK PULL-UP CURRENT vs OUTPUT VOLTAGE

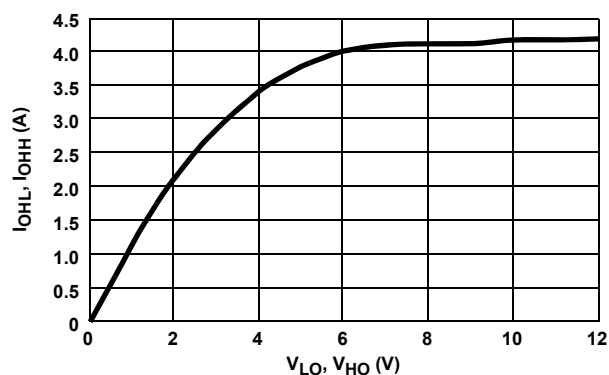


FIGURE 20. PEAK PULL-DOWN CURRENT vs OUTPUT VOLTAGE

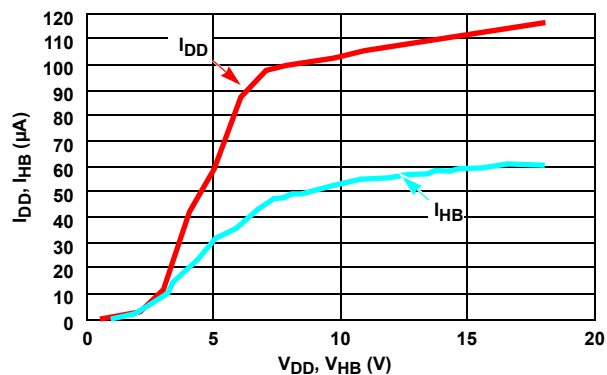


FIGURE 21. ISL2110 QUIESCENT CURRENT vs VOLTAGE

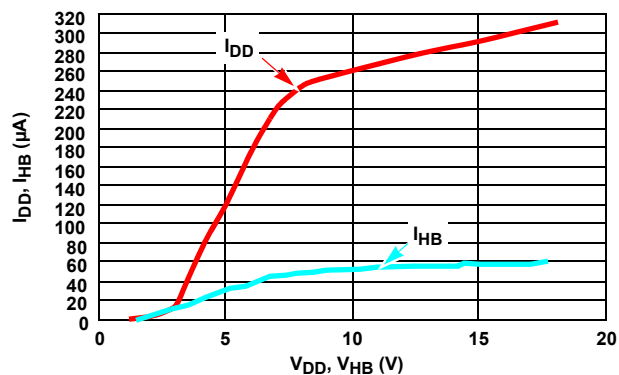


FIGURE 22. ISL2111 QUIESCENT CURRENT vs VOLTAGE

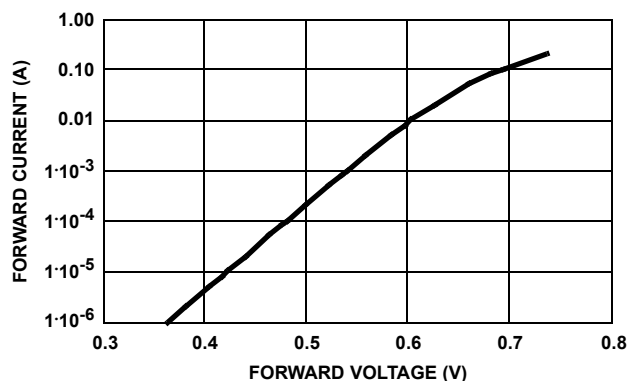
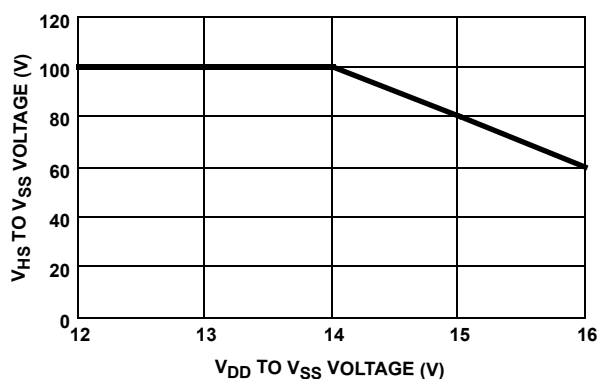


FIGURE 23. BOOTSTRAP DIODE I-V CHARACTERISTICS

FIGURE 24. V_{HS} VOLTAGE vs V_{DD} VOLTAGE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Oct 2, 2023	8.01	Updated M8.15 POD to the latest revision (corrected typo).
April 18, 2022	8.0	Updated the Ordering information table to comply with the new standard, updated notes. In Absolute Maximum Ratings, added Voltage on HO relative to HS and Voltage on LO relative to GND. Updated POD M8.15 to the latest version: "Added the coplanarity spec into the drawing." Removed Related Literature and About Intersil sections.
Mar 16, 2017	7.0	Corrected the branding of FG ISL2111BR4Z in the order information table from "211 1BR4A" to "211 1BR4Z". Added Revision History table and About Intersil information. Updated L10.4x4 Package Outline Drawing from Rev 1 to Rev 2. Change since Rev 1 is: "Tiebar note update from 'Tiebar shown (if present) is a non-functional feature' to 'Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends)'". Updated L12.4x4A Package Outline Drawing from Rev 1 to Rev 3. Changes since Rev 1 are: "Tiebar note update from 'Tiebar shown (if present) is a non-functional feature' to 'Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends)'"; "Bottom View changed from '3.2 REF' TO '2.5 REF'"; "Typical Recommended Land Pattern changed from '3.80' to '3.75'"; "Updated to new POD format by removing table listing dimensions and moving dimensions onto drawing", and "Added typical recommended land pattern". Updated M8.15 Package Outline Drawing from Rev 3 to Rev 4. Change since Rev 3 is: "Changed Note 1 from 1982 to 1994". Updated L8.4x4 Package Outline Drawing from Rev 0 to Rev 1. Change since Rev 0 is: "Tiebar note update from 'Tiebar shown (if present) is a non-functional feature' to 'Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends)'".

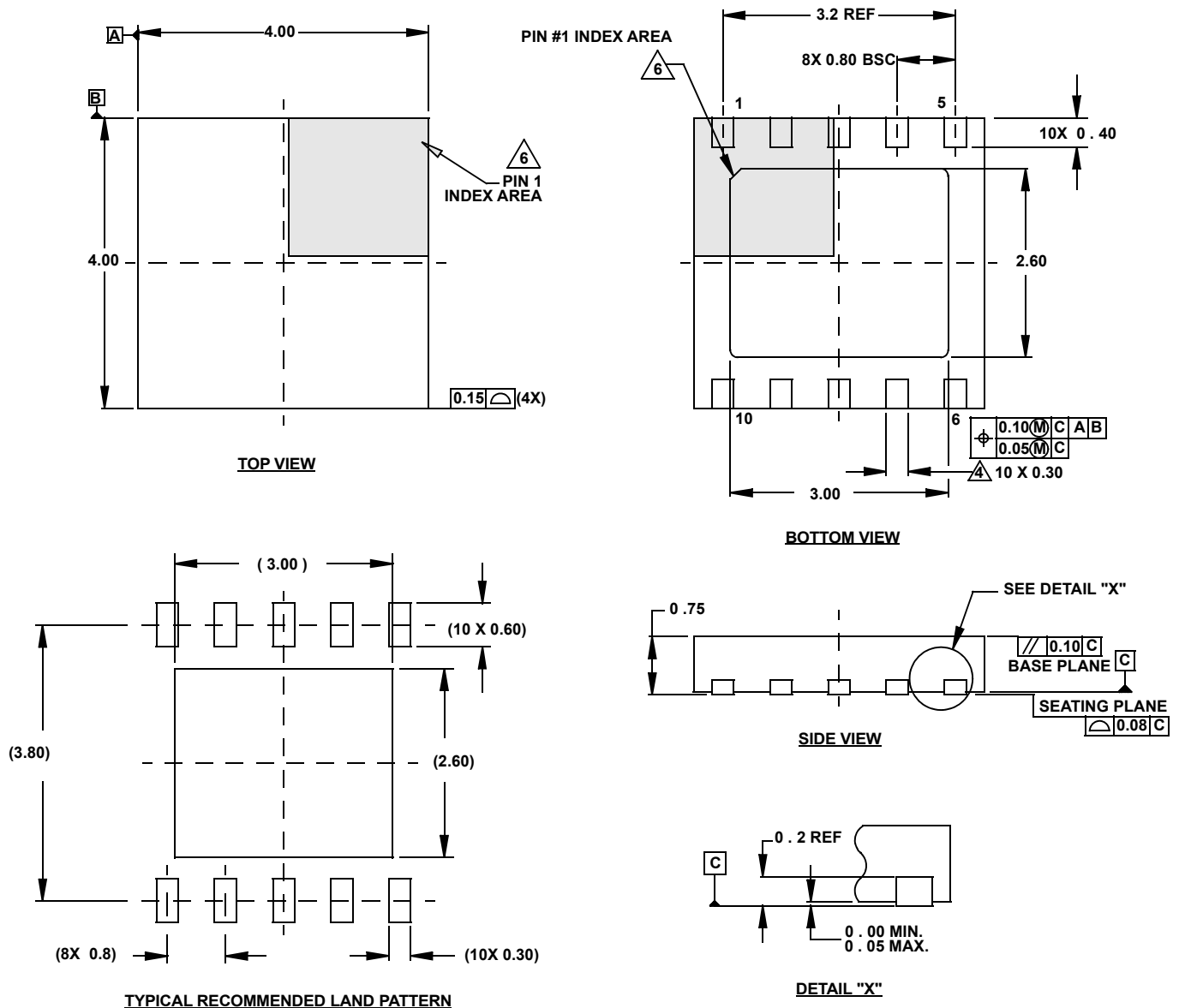
Package Outline Drawings

For the most recent package outline drawing, see [L10.4x4](#).

L10.4x4

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

Rev 2, 4/15



NOTES:

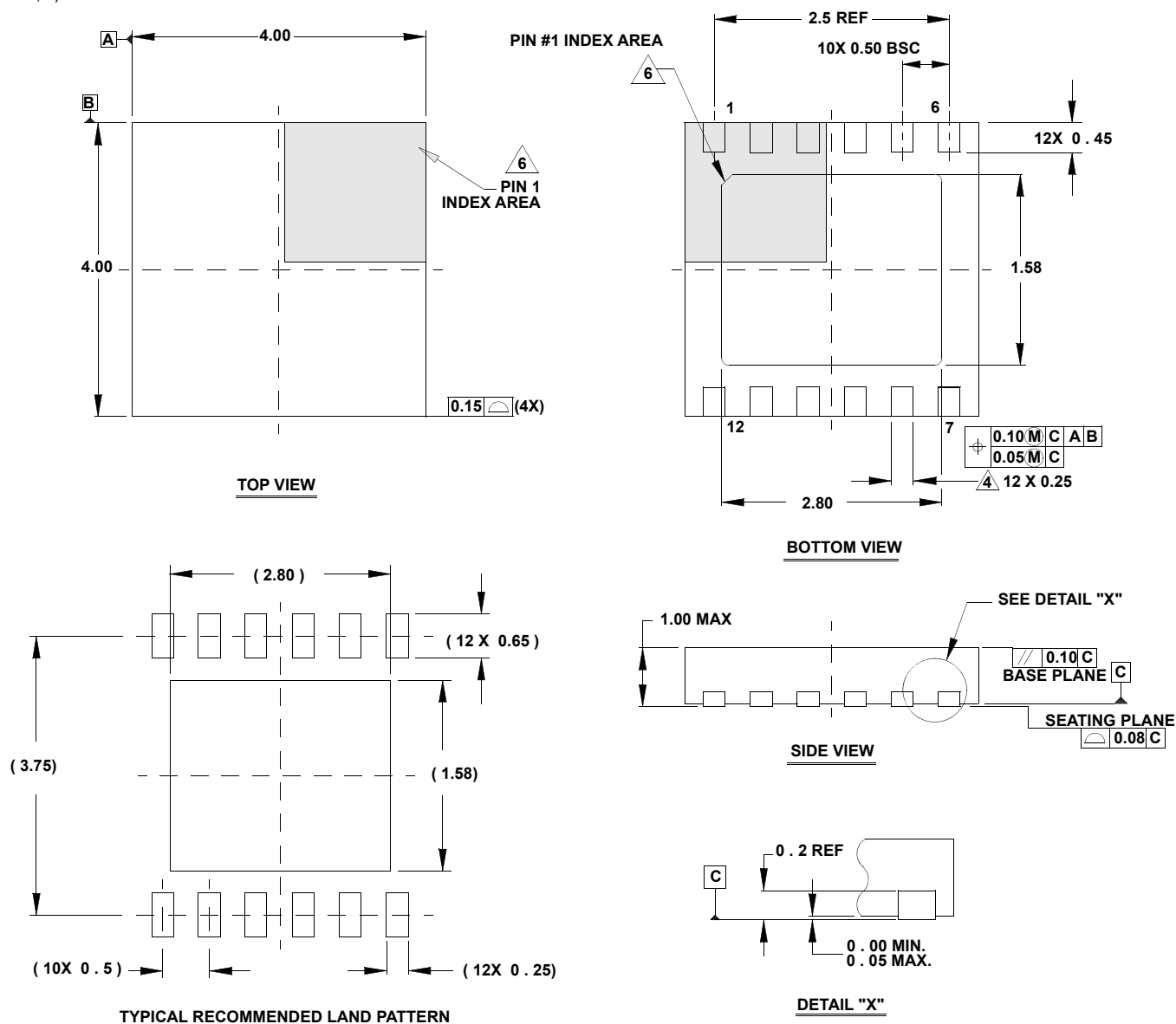
1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

For the most recent package outline drawing, see [L12.4x4A](#).

L12.4x4A

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

Rev 3, 3/15



NOTES:

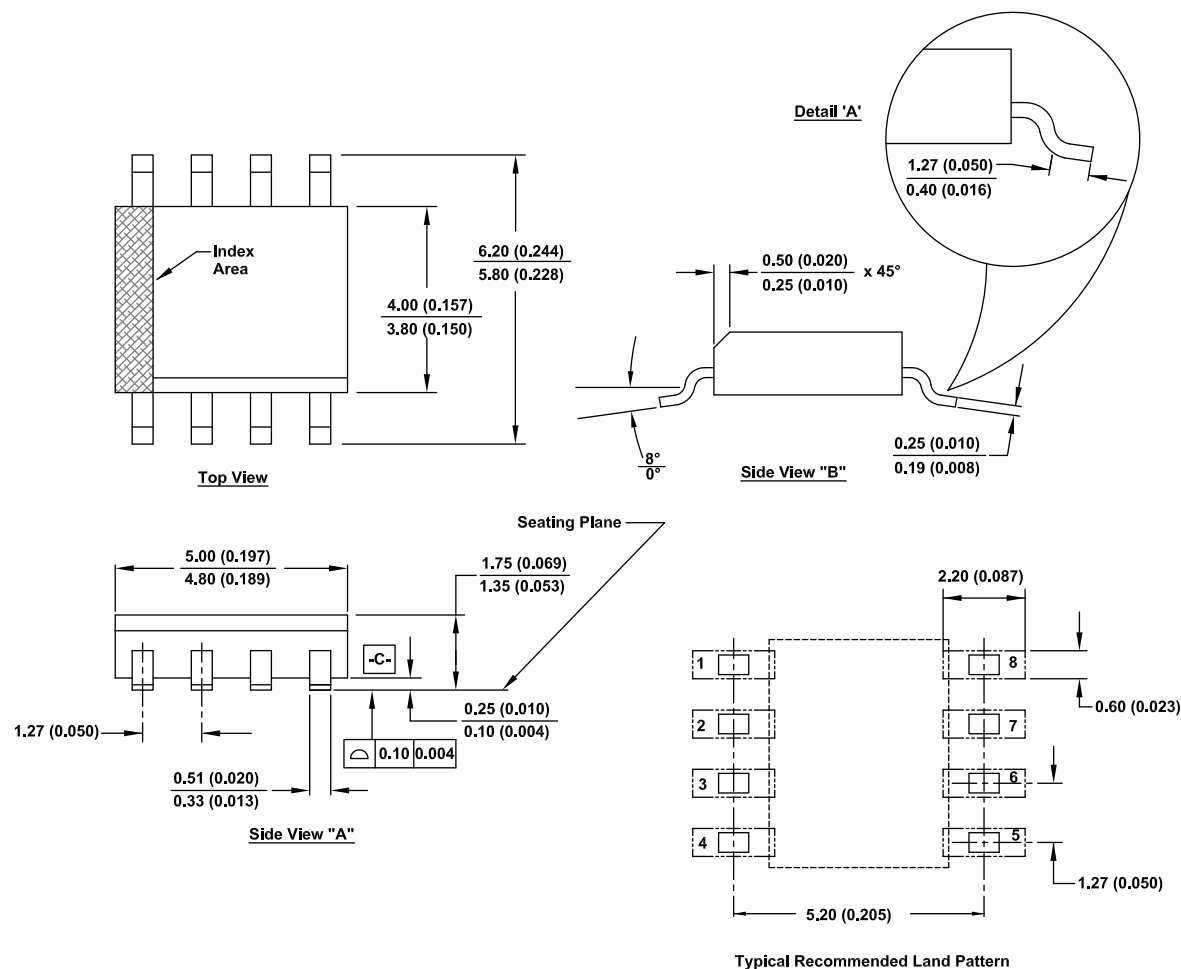
1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

For the most recent package outline drawing, see [M8.15](#).

M8.15

8 Lead Narrow Body Small Outline Plastic Package

Rev 7, 9/2023



Notes:

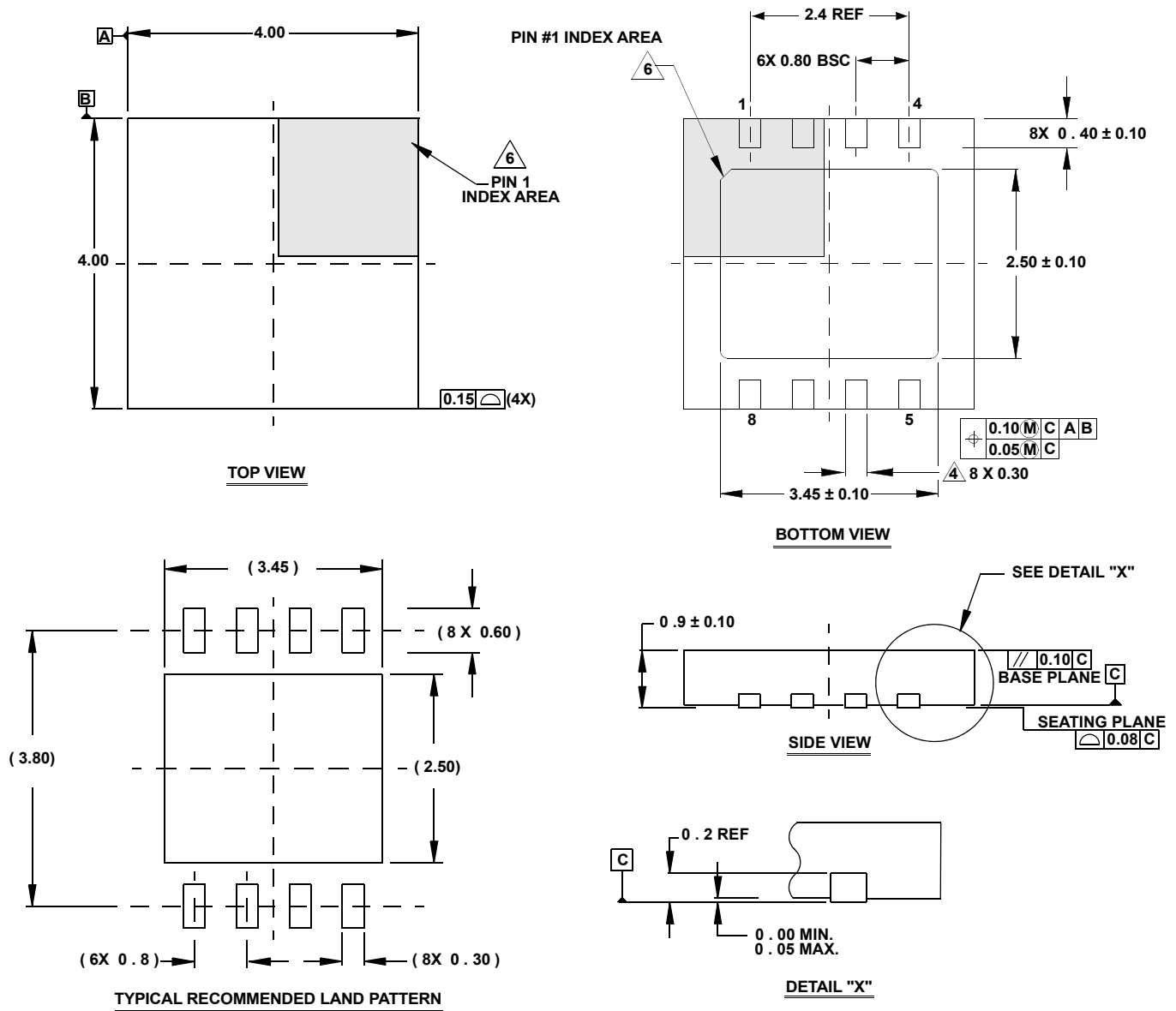
1. Dimension long and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

For the most recent package outline drawing, see [L8.4x4](#).

L8.4x4

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

Rev 1, 03/15



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.