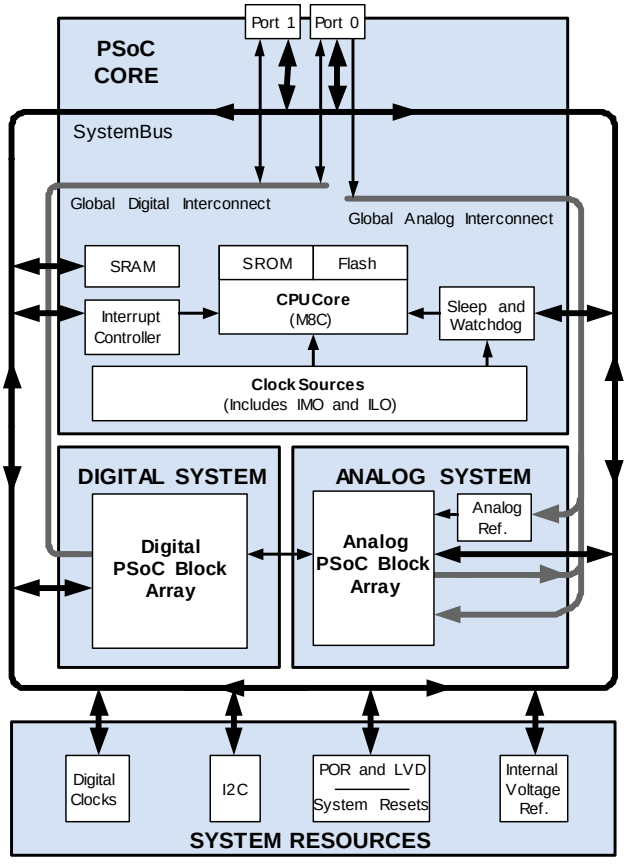
# FAN Controller
# CG6457AM and CG6462AM

## Features

- **Excellent for Fan Control Applications**
- **Powerful Harvard Architecture Processor**
  - M8C Processor Speeds to 12 MHz
  - Low Power at High Speed
  - 4.75V to 5.25V Operating Voltage
  - Extended Temperature Range: -40°C to +125°C
- **Advanced Peripherals (PSoC Blocks)**
  - 4 Analog Type "E" PSoC Blocks Provide:
    - 2 Comparators with DAC Refs
    - Single or Dual 8-Bit 8:1 ADC
  - 4 Digital PSoC Blocks Provide:
    - 8- to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Full-Duplex UART, SPI™ Master or Slave
    - Connectable to All GPIO Pins
  - Complex Peripherals by Combining Blocks
- **Flexible On-Chip Memory**
  - 4K Flash Program Storage
  - 256 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP™)
  - Partial Flash Updates
  - Flexible Protection Modes
- **Complete Development Tools**
  - Free Development Software (PSoC™ Designer)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128 Bytes Trace Memory
- **Precision, Programmable Clocking**
  - Internal ±3.5% 24 MHz Oscillator
  - Internal Oscillator for Watchdog and Sleep
- **Programmable Pin Configurations**
  - 25 mA Drive on All GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on All GPIO
  - Up to 8 Analog Inputs on GPIO
  - Configurable Interrupt on All GPIO
- **Additional System Resources**
  - $I^2C$™ Master, Slave and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference




## PSoC™ Functional Overview

The PSoC™ family consists of many *Mixed-Signal Array with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, as well as programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: the Core, the System Resources, the Digital System, and the Analog System. Configurable global bus resources allow all the device resources to be combined into a complete custom system. Each PSoC device includes four digital blocks. Depending on the PSoC package, up to two analog comparators and up to 16 general purpose IO (GPIO) are also included. The GPIO provide access to the global digital and analog interconnects.

### The PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The

CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two MIPS 8-bit Harvard architecture microprocessor.

System Resources provide additional capability, such as digital clocks to increase the flexibility of the PSoC mixed-signal arrays, I2C functionality for implementing an I2C master, slave, multi-master, an internal voltage reference that provides an absolute value of 1.3V to a number of PSoC subsystems, and various system resets supported by the M8C.

The Digital System is composed of an array of digital PSoC blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global busses that can route any signal to any pin. Freeing designs from the constraints of a fixed peripheral controller.

The Analog System is composed of four analog PSoC blocks, supporting comparators and analog-to-digital conversion up to 8 bits in precision.

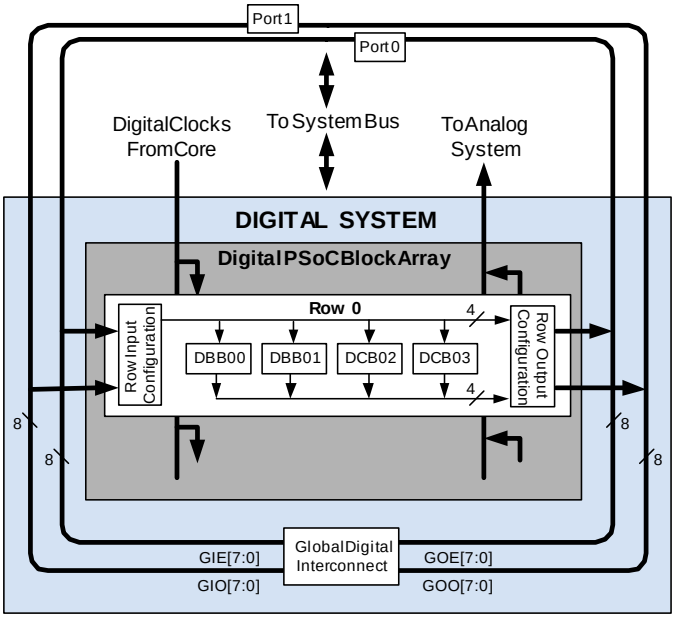
## The Digital System

The Digital System is composed of 4 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave, master, multi-master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 4)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global busses that can route any signal to any pin. The busses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled “PSoC Device Characteristics” on page 3.




**Digital System Block Diagram**

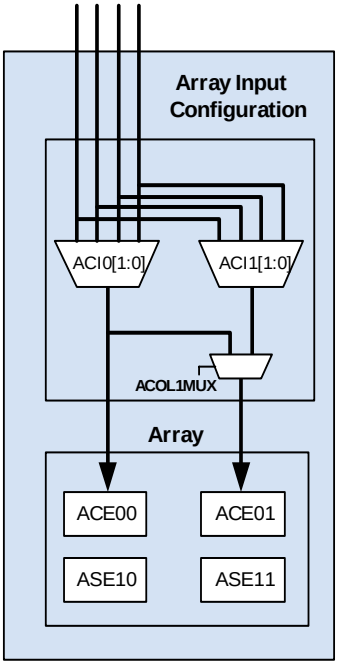
## The Analog System

The Analog System is composed of 4 configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (single or dual, with 10-bit resolution)
- Pin-to-pin comparators (1)
- Single-ended comparators (up to 2) with absolute (1.3V) reference
- 1.3V reference (as a System Resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The CG64xxAM devices provide limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

The number of blocks is on the device family which is detailed in the table titled “PSoC Device Characteristics” on page 3.




**Analog System Block Diagram**

## Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted below.

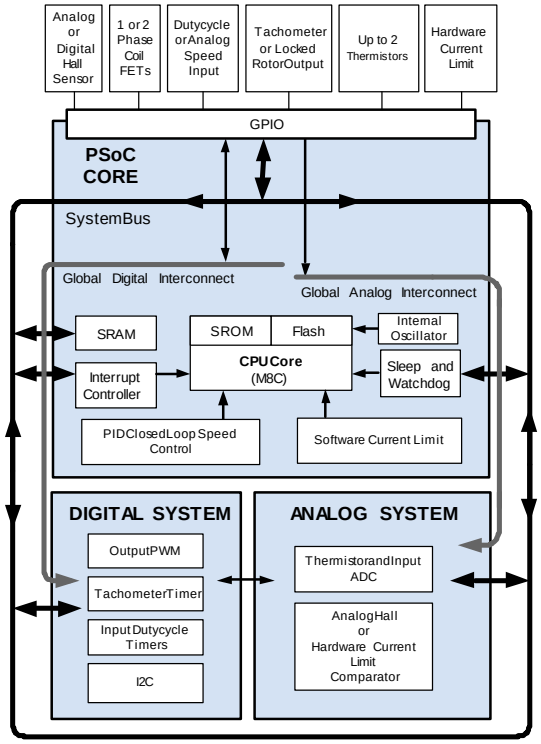
**PSoC Device Characteristics**

| PSoC Device Group | Digital IO | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | Amount of SRAM | Amount of Flash |
|---|---|---|---|---|---|---|---|---|---|
| CY8C29x66 | 64 | 4 | 16 | 12 | 4 | 4 | 12 | 2K | 32K |
| CY8C27x43 | 44 | 2 | 8 | 12 | 4 | 4 | 12 | 256 Bytes | 16K |
| CY8C24794 | 56 | 1 | 4 | 48 | 2 | 2 | 6 | 1K | 16K |
| CY8C24x23A | 24 | 1 | 4 | 12 | 2 | 2 | 6 | 256 Bytes | 4K |
| CY8C24x23 | 24 | 1 | 4 | 12 | 2 | 2 | 6 | 256 Bytes | 4K |
| CY8C21x34 | 28 | 1 | 4 | 28 | 0 | 2 | 4[a] | 512 Bytes | 8K |
| **CY8C21x23** | **16** | **1** | **4** | **8** | **0** | **2** | **4[a]** | **256 Bytes** | **4K** |

a. Limited analog functionality.

## Example Application

To develop an application for CG6462, use the CY8C21123 in the development tools. To develop an application for CG6457, use the CY8C21323 in the development tools. Following is a high-level diagram of an ideal application using this device.




**Fan Controller Block Diagram**

# Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC Mixed-Signal Array Technical Reference Manual*, which can be found on http://www.cypress.com/psoc.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at http://www.cypress.com.

## Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

## Technical Training

Free PSoC technical training is available for beginners and is taught by a marketing or application engineer over the phone. PSoC training classes cover designing, debugging, advanced analog, as well as application-specific classes covering topics such as PSoC and the LIN bus. Go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select Technical Training for more details.

## Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

## Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

## Application Notes

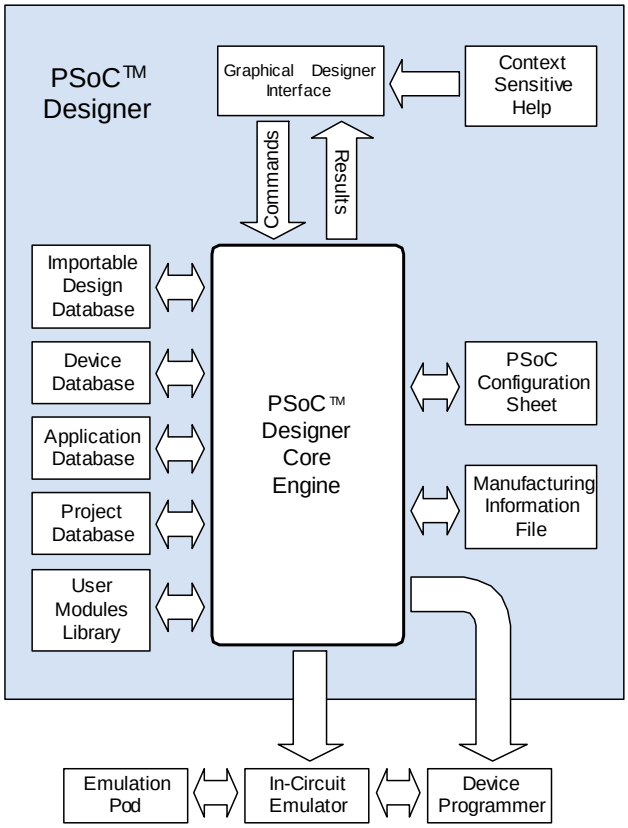
A long list of application notes will assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are sorted by date by default.

# Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.




**PSoC Designer Subsystems**

## PSoC Designer Software Subsystems

### *Device Editor*

The device editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

### *Design Browser*

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

### *Application Editor*

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

**Assembler.** The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compiler.** A C language compiler is available that supports PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

### *Debugger*

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read the program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

### *Online Help System*

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

## PSoC Express Software

PSoC Express is the first visual embedded system design tool that allows a user to create an entire PSoC Project, generate a schematic, BOM, and data sheet without writing a single line of code. System designers are finally free from the low-level implementation details of "micro-coding" to work directly with application objects such as LEDs, switches, sensors, and fans. Because the details of the actual firmware are left to the PSoC Express firmware generation engine, and hidden from the user, not only are design cycles reduced from weeks and months to a few hours, but the generated, fully-tested 'C' code is completely standardized, considerably increasing overall design quality and maintainability. Go to http://www.cypress.com/psocexpress for free downloads and more information.

## Hardware Tools

### *In-Circuit Emulator*

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation

# Designing with User Modules

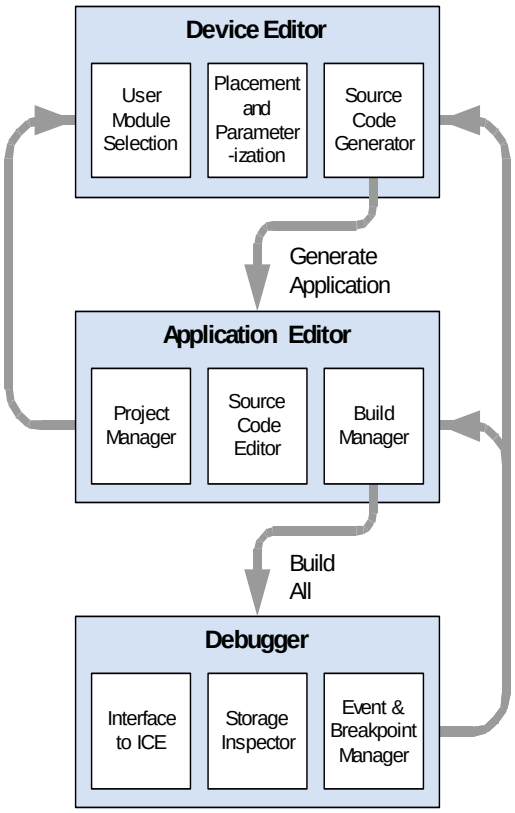
The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, busses and to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 common peripherals such as ADCs, DACs Timers, Counters, UARTs, and other not-so common peripherals such as DTMF Generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.




**User Module and Source Code Development Flows**

The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

# Document Conventions

## Acronyms Used

The following table lists the acronyms that are used in this document.

| Acronym | Description |
|---|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CPU | central processing unit |
| CT | continuous time |
| DAC | digital-to-analog converter |
| DC | direct current |
| FSR | full scale range |
| GPIO | general purpose IO |
| IO | input/output |
| IPOR | imprecise power on reset |
| LSb | least-significant bit |
| LVD | low voltage detect |
| MSb | most-significant bit |
| PC | program counter |
| POR | power on reset |
| PPOR | precision power on reset |
| PSoC™ | Programmable System-on-Chip |
| PWM | pulse width modulator |
| ROM | read only memory |
| SC | switched capacitor |
| SRAM | static random access memory |

## Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 3-1 on page 13 lists all the abbreviations used to measure the PSoC devices.

## Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexidecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

# Table of Contents

For an in depth discussion and more information on your PSoC device, obtain the *PSoC Mixed-Signal Array Technical Reference Manual* on http://www.cypress.com. This data sheet encompasses and is organized into the following chapters and sections.

# 1. Pin Information

This chapter describes, lists, and illustrates the CG64xxAM PSoC device pins and pinout configurations.

## 1.1 Pinouts

The CG6462AM and CG6457AM PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, and XRES are not capable of Digital IO.

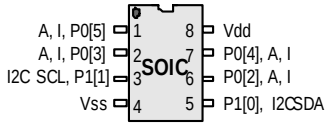
### 1.1.1 8-Pin Part Pinout

**Table 1-1. 8-Pin Part Pinout (SOIC)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I | P0[5] | Analog column mux input. |
| 2 | IO | I | P0[3] | Analog column mux input. |
| 3 | IO | | P1[1] | I2C Serial Clock (SCL), ISSP-SCLK. |
| 4 | Power | | Vss | Ground connection. |
| 5 | IO | | P1[0] | I2C Serial Data (SDA), ISSP-SDATA. |
| 6 | IO | I | P0[2] | Analog column mux input. |
| 7 | IO | I | P0[4] | Analog column mux input. |
| 8 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.

**CG6462AM 8-Pin PSoC Device**



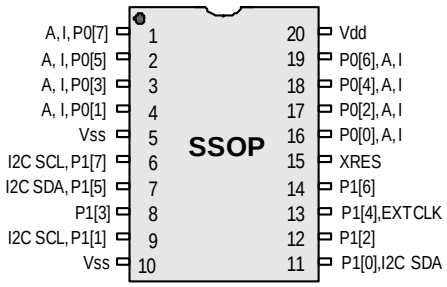
## 1.1.2 20-Pin Part Pinout

**Table 1-2. 20-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | I | P0[5] | Analog column mux input. |
| 3 | IO | I | P0[3] | Analog column mux input. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | Power | | Vss | Ground connection. |
| 6 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 7 | IO | | P1[5] | I2C Serial Data (SDA). |
| 8 | IO | | P1[3] | |
| 9 | IO | | P1[1] | I2C Serial Clock (SCL), ISSP-SCLK. |
| 10 | Power | | Vss | Ground connection. |
| 11 | IO | | P1[0] | I2C Serial Data (SDA), ISSP-SDATA. |
| 12 | IO | | P1[2] | |
| 13 | IO | | P1[4] | Optional External Clock Input (EXT-CLK). |
| 14 | IO | | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull down. |
| 16 | IO | I | P0[0] | Analog column mux input. |
| 17 | IO | I | P0[2] | Analog column mux input. |
| 18 | IO | I | P0[4] | Analog column mux input. |
| 19 | IO | I | P0[6] | Analog column mux input. |
| 20 | Power | | Vdd | Supply voltage. |

**LEGEND** A = Analog, I = Input, and O = Output.

**CG6457AM 20-Pin PSoC Device**



# 2. Register Reference

This chapter lists the registers of the CG64xxAM PSoC device. For detailed register information, reference the *PSoC™ Mixed-Signal Array Technical Reference Manual*.

## 2.1 Register Conventions

The register conventions specific to this section are listed in the following table.

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## 2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and should not be accessed.

## Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| | 08 | | | 48 | | | 88 | | | C8 | |
| | 09 | | | 49 | | | 89 | | | C9 | |
| | 0A | | | 4A | | | 8A | | | CA | |
| | 0B | | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | | D0 | |
| | 11 | | | 51 | | | 91 | | | D1 | |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | | D3 | |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | | 97 | | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | | 63 | | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | E4 | |
| DBB01DR1 | 25 | W | | 65 | | | A5 | | | E5 | |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | | E8 | |
| DCB02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | | E9 | |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| DCB02CR0 | 2B | # | | 6B | | | AB | | | EB | |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed. # Access is bit specific.

## Register Map Bank 1 Table: Configuration Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | | 87 | | | C7 | |
| | 08 | | | 48 | | | 88 | | | C8 | |
| | 09 | | | 49 | | | 89 | | | C9 | |
| | 0A | | | 4A | | | 8A | | | CA | |
| | 0B | | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | | 91 | | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | | D6 | |
| | 17 | | | 57 | | | 97 | | | D7 | |
| | 18 | | | 58 | | | 98 | | | D8 | |
| | 19 | | | 59 | | | 99 | | | D9 | |
| | 1A | | | 5A | | | 9A | | | DA | |
| | 1B | | | 5B | | | 9B | | | DB | |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | ADC0_TR | E5 | RW |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | ADC1_TR | E6 | RW |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | CLK_CR3 | 6B | RW | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | FLS_PR1 | FA | RW |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed. # Access is bit specific.

# 3. Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CG64xxAM PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ $T_A$ ≤ 85°C and $T_J$ ≤ 100°C, except where noted.

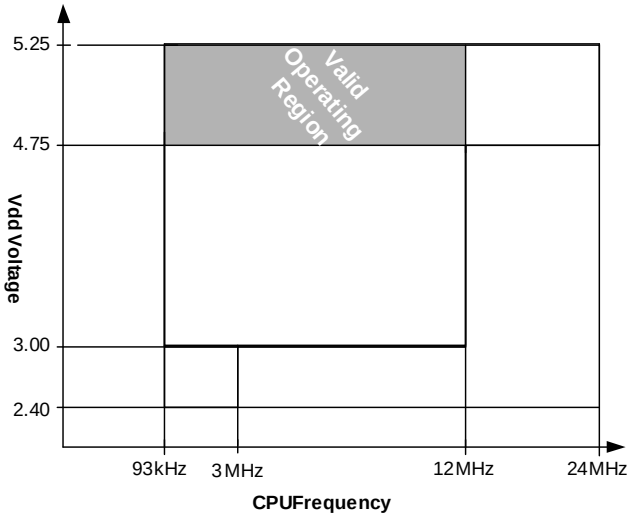



**Figure 3-1. Vdd Voltage versus CPU Frequency**

The following table lists the units of measure that are used in this chapter.

**Table 3-1: Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | µW | microwatts |
| dB | decibels | mA | milli-ampere |
| fF | femto farad | ms | milli-second |
| Hz | hertz | mV | milli-volts |
| KB | 1024 bytes | nA | nanoampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolts |
| kΩ | kilohm | Ω | ohm |
| MHz | megahertz | pA | picoampere |
| MΩ | megaohm | pF | picofarad |
| µA | microampere | pp | peak-to-peak |
| µF | microfarad | ppm | parts per million |
| µH | microhenry | ps | picosecond |
| µs | microsecond | sps | samples per second |
| µV | microvolts | σ | sigma: one standard deviation |
| µVrms | microvolts root-mean-square | V | volts |

# 3.1 Absolute Maximum Ratings

**Table 3-2. Absolute Maximum Ratings**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -40 | – | +100 | °C | Higher storage temperatures will reduce data retention time. |
| $T_A$ | Ambient Temperature with Power Applied | -40 | – | +125 | °C | |
| Vdd | Supply Voltage on Vdd Relative to Vss | -0.5 | – | +6.0 | V | |
| $V_{IO}$ | DC Input Voltage | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $V_{IOZ}$ | DC Voltage Applied to Tri-state | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $I_{MIO}$ | Maximum Current into any Port Pin | -25 | – | +50 | mA | |
| ESD | Electro Static Discharge Voltage | 2000 | – | – | V | Human Body Model ESD. |
| LU | Latch-up Current | – | – | 200 | mA | |

# 3.2 Operating Temperature

**Table 3-3. Operating Temperature**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature | -40 | – | +85 | °C | |
| $T_J$ | Junction Temperature at $T_A \le 85^oC$ | -40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See “Thermal Impedances” on page 23. The user must limit the power consumption to comply with this requirement. |
| $TA_{PEAK}$ | Peak Ambient Temperature | – | – | +125 | °C | Not to exceed 5000 hours at $T_A > 85^oC$. |

# 3.3 DC Electrical Characteristics

## 3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-4. DC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply Voltage | 4.75 | – | 5.25 | V | See DC POR and LVD specifications, Table 3-7 on page 16. |
| $I_{DD}$ | Supply Current, IMO = 24 MHz | – | 3 | 8 | mA | Conditions are Vdd = 5.0V, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz. |
| $I_{SB}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. | – | 4 | 8 | µA | Vdd = 5.25V, $-40^oC \le T_A \le 55^oC$. |
| $I_{SBH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. | – | 5 | 100 | µA | Vdd = 5.25V, $55^oC \le T_A \le 125^oC$. |
| $V_{REF}$ | Reference Voltage (Bandgap) | 1.28 | 1.30 | 1.32 | V | Trimmed for appropriate Vdd. Vdd = 4.75V to 5.25V. |

## 3.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-5. DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull down Resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High Output Level | Vdd - 1.0 | – | – | V | IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget. |
| $V_{OL}$ | Low Output Level | – | – | 0.75 | V | IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget. |
| $V_{IL}$ | Input Low Level | – | – | 0.8 | V | Vdd = 4.75 to 5.25. |
| $V_{IH}$ | Input High Level | 2.1 | – | | V | Vdd = 4.75 to 5.25. |
| $V_H$ | Input Hysteresis | – | 60 | – | mV | |
| $I_{IL}$ | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{IN}$ | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |
| $C_{OUT}$ | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |

## 3.3.3 DC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-6. DC Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) | – | 2.5 | 15 | mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$ | Input Leakage Current (Port 0 Analog Pins) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0.0 | – | Vdd - 1 | V | |
| $G_{OLOA}$ | Open Loop Gain | 80 | – | – | dB | |
| $I_{SOA}$ | Amplifier Supply Current | – | 10 | 30 | µA | |

## 3.3.4 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-7. DC POR and LVD Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{PPOR2}$ | Vdd Value for PPOR Trip<br>PORLEV[1:0] = 10b | – | 4.55 | 4.70 | V | Vdd must be greater than or equal to 4.75V during startup. |
| | Vdd Value for LVD Trip | | | | | |
| $V_{LVD6}$ | VM[2:0] = 110b | 4.62 | 4.73 | 4.83 | V | |
| $V_{LVD7}$ | VM[2:0] = 111b | 4.71 | 4.81 | 4.95 | V | |

## 3.3.5 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-8. DC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $Vdd_{IWRITE}$ | Supply Voltage for Flash Write Operations | 4.25 | – | – | V | |
| $I_{DDP}$ | Supply Current During Programming or Verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input Low Voltage During Programming or Verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input High Voltage During Programming or Verify | 2.2 | – | – | V | |
| $I_{ILP}$ | Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| $I_{IHP}$ | Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| $V_{OLV}$ | Output Low Voltage During Programming or Verify | – | – | Vss + 0.75 | V | |
| $V_{OHV}$ | Output High Voltage During Programming or Verify | Vdd - 1.0 | – | Vdd | V | |
| $Flash_{DR}$ | Flash Data Retention | 15[a] | 100 | – | Years | |

a. Flash data retention is based upon a use condition of ≤ 5000 hours at $T_A$ ≤ 125°C and remaining time at $T_A$ ≤ 60°C.

# 3.4 AC Electrical Characteristics

## 3.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-9. AC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO24}$ | Internal Main Oscillator Frequency for 24 MHz | 23.16 | 24 | 24.84 | MHz | 0°C ≤ $T_A$ ≤ 100°C. |
| $F_{CPU1}$ | CPU Frequency (5V Nominal) | 0.93 | 12 | 12.42 | MHz | |
| $F_{BLK5}$ | Digital PSoC Block Frequency (5V Nominal) | 0 | 24 | 24.84 | MHz | Refer to the AC Digital Block Specifications. |
| $F_{32K1}$ | Internal Low Speed Oscillator Frequency | 15 | 32 | 64 | kHz | |
| Jitter32k | 32 kHz RMS Period Jitter | – | 100 | 200 | ns | |
| Jitter32k | 32 kHz Peak-to-Peak Period Jitter | – | 1400 | – | ns | |
| $T_{XRST}$ | External Reset Pulse Width | 10 | – | – | µs | |
| DC24M | 24 MHz Duty Cycle | 40 | 50 | 60 | % | |
| Step24M | 24 MHz Trim Step Size | – | 50 | – | kHz | |
| Fout48M | 48 MHz Output Frequency | – | – | – | MHz | Doubler. Use not allowed. |
| Jitter24M1 | 24 MHz Peak-to-Peak Period Jitter (IMO) | – | 300 | | ps | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| $T_{RAMP}$ | Supply Ramp Time | 0 | – | – | µs | |

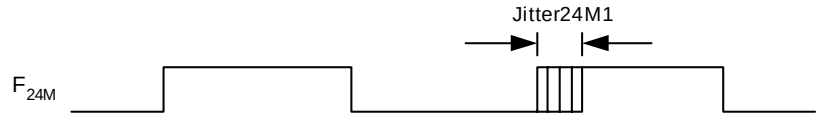



**Figure 3-2. 24 MHz Period Jitter (IMO) Timing Diagram**

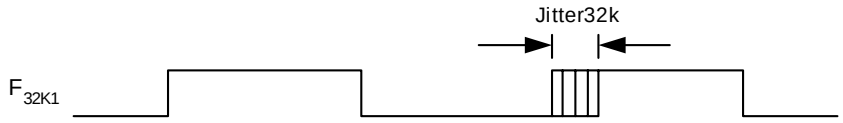



**Figure 3-3. 32 kHz Period Jitter (ILO) Timing Diagram**

## 3.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-10. AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO Operating Frequency | 0 | – | 12 | MHz | Normal Strong Mode |
| TRiseF | Rise Time, Normal Strong Mode, Cload = 50 pF | 3 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| TFallF | Fall Time, Normal Strong Mode, Cload = 50 pF | 2 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| TRiseS | Rise Time, Slow Strong Mode, Cload = 50 pF | 10 | 27 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |
| TFallS | Fall Time, Slow Strong Mode, Cload = 50 pF | 10 | 22 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |

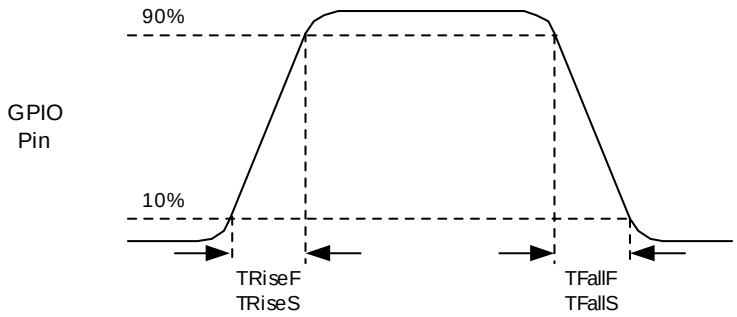



**Figure 3-4. GPIO Timing Diagram**

## 3.4.3 AC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-11. AC Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{COMP1}$ | Comparator Mode Response Time, 50 mVpp Signal Centered on Ref | | | 200 | ns | |

## 3.4.4 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-12. AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| All Functions | Maximum Block Clocking Frequency (> 4.75V) | | | 24.84 | MHz | 4.75V < Vdd < 5.25V. |
| Timer | Capture Pulse Width | 50[a] | – | – | ns | |
| | Maximum Frequency, No Capture | – | – | 24.84 | MHz | 4.75V < Vdd < 5.25V. |
| | Maximum Frequency, With or Without Capture | – | – | 24.84 | MHz | |
| Counter | Enable Pulse Width | 50 | – | – | ns | |
| | Maximum Frequency, No Enable Input | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| | Maximum Frequency, Enable Input | – | – | 24.6 | MHz | |
| Dead Band | Kill Pulse Width: | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50 | – | – | ns | |
| | Disable Mode | 50 | – | – | ns | |
| | Maximum Frequency | – | – | 24.84 | MHz | 4.75V < Vdd < 5.25V. |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency | – | – | 24.84 | MHz | 4.75V < Vdd < 5.25V. |
| CRCPRS (CRC Mode) | Maximum Input Clock Frequency | – | – | 24.84 | MHz | |
| SPIM | Maximum Input Clock Frequency | – | – | 8.2 | MHz | Maximum data rate at 4.1 MHz due to 2 x over clocking. |
| SPIS | Maximum Input Clock Frequency | – | – | 4.1 | MHz | |
| | Width of SS_ Negated Between Transmissions | 50 | – | – | ns | |
| Transmitter | Maximum Input Clock Frequency | – | – | 24.84 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. |
| Receiver | Maximum Input Clock Frequency | – | – | 24.84 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. |

a. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

## 3.4.5 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-13. AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0.093 | – | 24.6 | MHz | |
| – | High Period | 20.6 | – | 5300 | ns | |
| – | Low Period | 20.6 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | µs | |

## 3.4.6 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-14. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{RSCLK}$ | Rise Time of SCLK | 1 | – | 20 | ns | |
| $T_{FSCLK}$ | Fall Time of SCLK | 1 | – | 20 | ns | |
| $T_{SSCLK}$ | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns | |
| $T_{HSCLK}$ | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $T_{ERASEB}$ | Flash Erase Time (Block) | – | 15 | – | ms | |
| $T_{WRITE}$ | Flash Block Write Time | – | 30 | – | ms | |
| $T_{DSCLK5}$ | Data Out Delay from Falling Edge of SCLK | – | – | 50 | ns | |

## 3.4.7 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-15. AC Characteristics of the I²C SDA and SCL Pins for Vcc ≥ 4.75V**

| Symbol | Description | Standard Mode | | Fast Mode | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $F_{SCLI2C}$ | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz | |
| $T_{HDSTAI2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs | |
| $T_{LOWI2C}$ | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | µs | |
| $T_{HIGHI2C}$ | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | µs | |
| $T_{SUSTAI2C}$ | Set-up Time for a Repeated START Condition | 4.7 | – | 0.6 | – | µs | |
| $T_{HDDATI2C}$ | Data Hold Time | 0 | – | 0 | – | µs | |
| $T_{SUDATI2C}$ | Data Set-up Time | 250 | – | 100[a] | – | ns | |
| $T_{SUSTOI2C}$ | Set-up Time for STOP Condition | 4.0 | – | 0.6 | – | µs | |
| $T_{BUFI2C}$ | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | µs | |
| $T_{SPI2C}$ | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | |

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

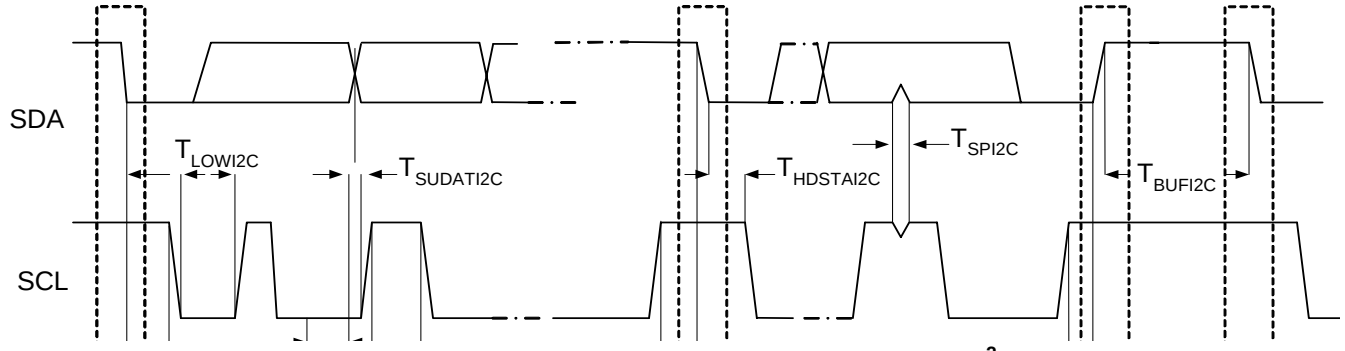



**Figure 3-5. Definition for Timing for Fast/Standard Mode on the I²C Bus**

# 4. Packaging Information

This chapter illustrates the packaging specifications for the CG64xxAM PSoC device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/support/link.cfm?mr=poddim.

## 4.1 Packaging Dimensions

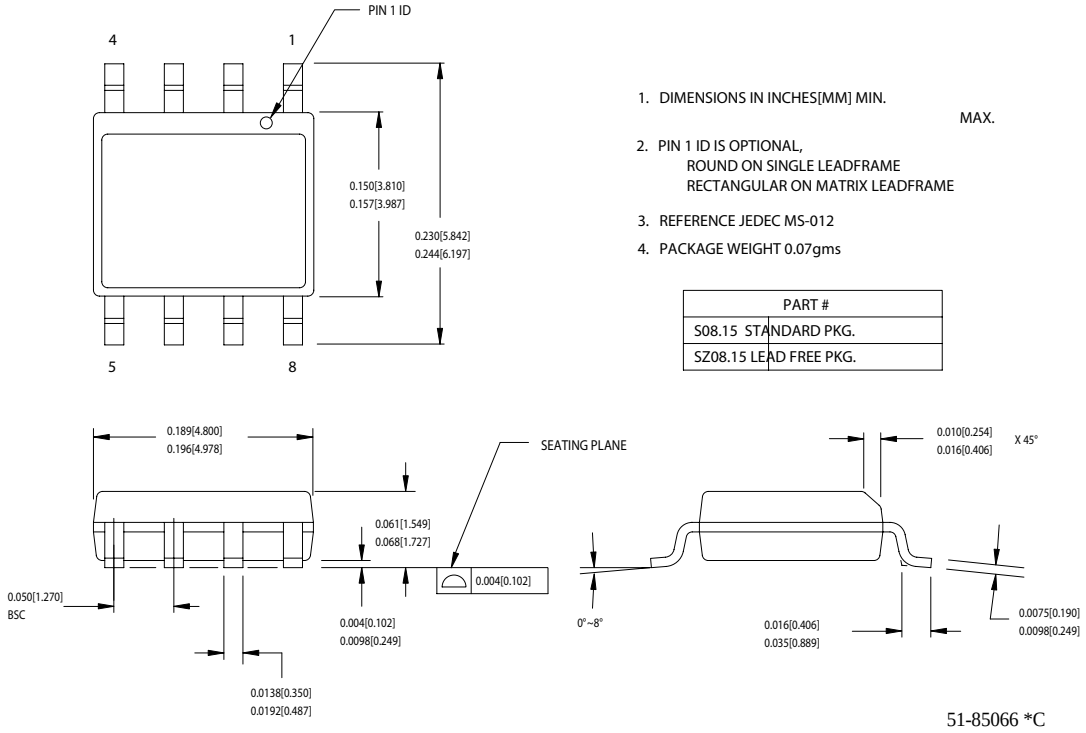



**Figure 4-1. 8-Lead (150-Mil) SOIC**

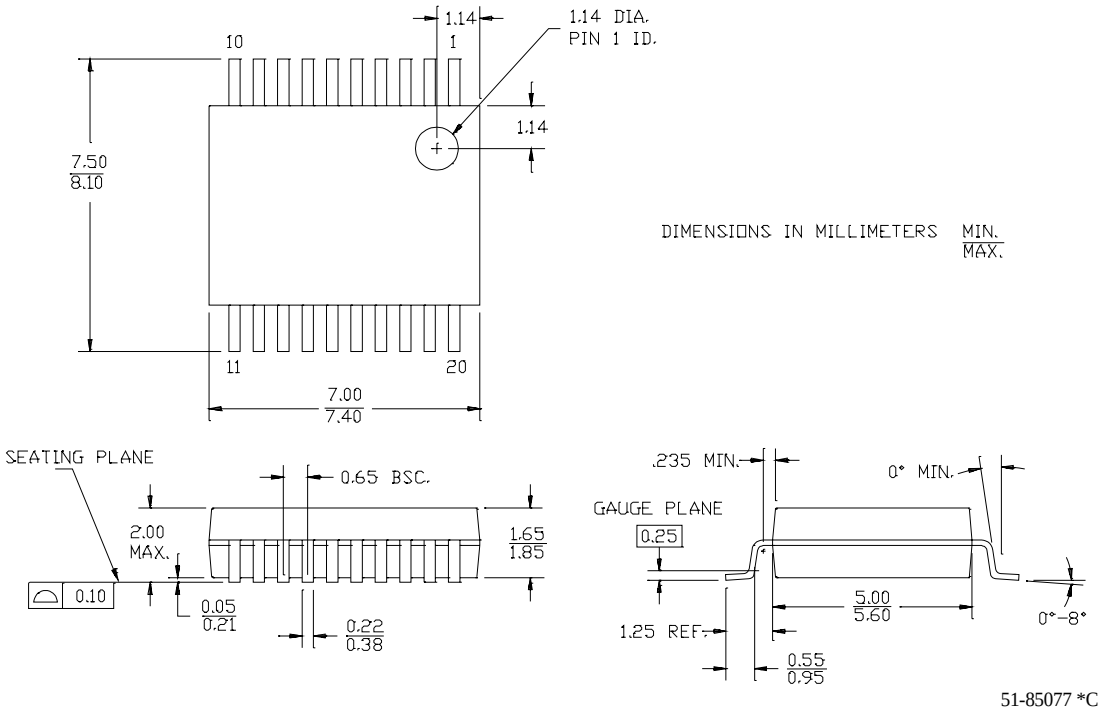



**Figure 4-2. 20-Lead (210-MIL) SSOP**

## 4.2 Thermal Impedances

**Table 4-1. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ * |
|---|---|
| 8 SOIC | 186 °C/W |
| 20 SSOP | 117 °C/W |

* $T_J = T_A + POWER \times \theta_{JA}$

## 4.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

**Table 4-2. Solder Reflow Peak Temperature**

| Package | Minimum Peak Temperature* | Maximum Peak Temperature |
|---|---|---|
| 8 SOIC | 240°C | 260°C |
| 20 SSOP | 240°C | 260°C |

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220+/-5°C with Sn-Pb or 245+/-5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

# 5. Ordering Information

The following table lists the CG64xxAM PSoC device's key package features and ordering codes.

**Table 5-1. CG64xxAM PSoC Device Key Features and Ordering Information**

| Package | Ordering Code | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital PSoC Blocks | Analog Blocks | Digital IO Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 Pin (150-Mil) SOIC[a] | CG6462AM | 4K | 256 | No | -40°C to +125°C | 4 | 4 | 6 | 4 | 0 | No |
| 8 Pin (150-Mil) SOIC (Tape and Reel)[a] | CG6462AMT | 4K | 256 | No | -40°C to +125°C | 4 | 4 | 6 | 4 | 0 | No |
| 20 Pin (210-Mil) SSOP[a] | CG6457AM | 4K | 256 | No | -40°C to +125°C | 4 | 4 | 16 | 8 | 0 | Yes |
| 20 Pin (210-Mil) SSOP (Tape and Reel)[a] | CG6457AMT | 4K | 256 | No | -40°C to +125°C | 4 | 4 | 16 | 8 | 0 | Yes |

a. Lead-free package.

# 6. Sales and Service Information

To obtain information about Cypress Semiconductor or PSoC sales and technical support, reference the following information.

**Cypress Semiconductor**
2700 162nd Street SW, Building D Phone: 800.669.0557
Lynnwood, WA 98037 Facsimile: 425.787.4641

Web Sites: Company Information – http://www.cypress.com
Sales – http://www.cypress.com/aboutus/sales_locations.cfm
Technical Support – http://www.cypress.com/support/login.cfm

## 6.0 Revision History

**Document Title**: Fan Controller CG64xxAM PSoC Mixed-Signal Array Preliminary Data Sheet
**Document Number**: 001-00353

| Revision | ECN # | Issue Date | Origin of Change | Description of Change |
|---|---|---|---|---|
| ** | 366815 | See ECN | HMT | New silicon and document (Revision **). |

**Distribution**: External/Public **Posting**: None

## 6.1 Copyrights and Flash Code Protection



**Flash Code Protection**

Note the following details of the Flash code protection features on Cypress Semiconductor PSoC devices.

Cypress Semiconductor products meet the specifications contained in their particular data sheets. Cypress Semiconductor believes that its PSoC family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress Semiconductor, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress Semiconductor nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress Semiconductor is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress Semiconductor are committed to continuously improving the code protection features of our products.