

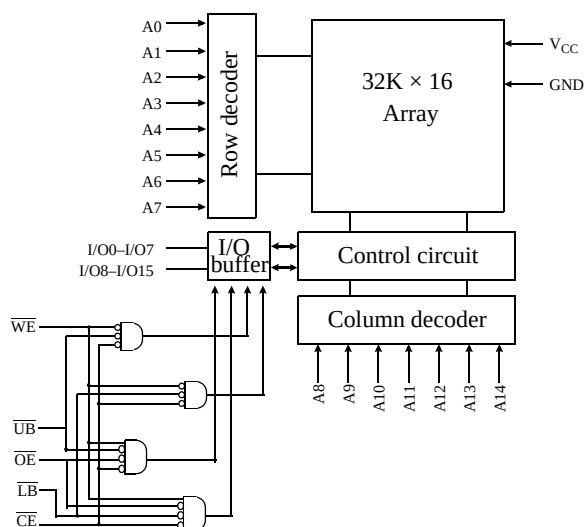


5V 32K×16 CMOS SRAM

Features

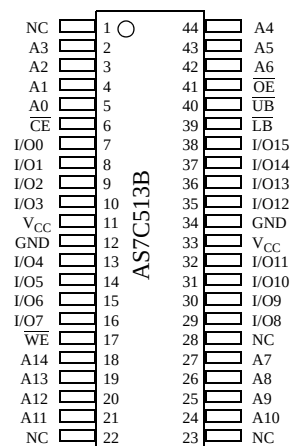
- Industrial and commercial temperature
- Organization: 32,768 words × 16 bits
- Center power and ground pins
- High speed
- 10/12/15/20 ns address access time
- 5, 6, 7, 8 ns output enable access time
- Low power consumption: ACTIVE
- 605mW / max @ 10 ns
- Low power consumption: STANDBY
- 55 mW / max CMOS I/O
- 6T 0.18u CMOS Technology
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- 44-pin JEDEC standard package
- 400 mil SOJ
- 400 mil TSOP 2
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement

44-Pin SOJ, TSOP 2 (400 mil)



Selection guide

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	110	100	90	80	mA
Maximum CMOS standby current	10	10	10	10	mA



Functional description

The AS7C513B is a high performance CMOS 524,288-bit Static Random Access Memory (SRAM) device organized as 32,768 words $\times$ 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5, 6, 7, 8 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high, the device enters standby mode. If inputs are still toggling, the device consumes I_{SB} power. If the bus is static, then the full standby power is reached (I_{SB1}). The AS7C513B is guaranteed not to exceed 55mW power consumption under nominal full standby conditions.

A write cycle is accomplished by asserting write enable ($\overline{WE}$), ($\overline{UB}$) and/or ($\overline{LB}$), and chip enable ($\overline{CE}$). Data on the input pins I/O0 - I/O7, and/or I/O8 - I/O15, is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$), ($\overline{UB}$) and ($\overline{LB}$), and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, or ($\overline{UB}$) and ($\overline{LB}$), output drivers stay in high-impedance mode.

The devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0 - I/O7, and $\overline{UB}$ controls the higher bits, I/O8 - I/O15.

All chip inputs and outputs are TTL-compatible. The AS7C513B is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	-0.50	+7.0	V
Voltage on any pin relative to GND	V_{t2}	-0.50	$V_{CC} + 0.50$	V
Power dissipation	P_D	—	1.0	W
Storage temperature (plastic)	T_{stg}	-65	+150	$^{\circ}\text{C}$
Ambient temperature with V_{CC} applied	T_{bias}	-55	+125	$^{\circ}\text{C}$
DC current into outputs (low)	I_{OUT}	—	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB} , I_{SB1})
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7 (I_{CC})
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15 (I_{CC})
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15 (I_{CC})
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15 (I_{CC})
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7 (I_{CC})
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15 (I_{CC})
L	H	H	X	X	High Z	High Z	Output disable (I_{CC})
L	X	X	H	H	High Z	High Z	

Key: X = Don't care; L = Low; H = High



Recommended operating conditions

Parameter		Symbol	Min	Typical	Max	Unit
Supply voltage		V_{CC}	4.5	5	5.5	V
Input voltage		V_{IH}	2.2	-	$V_{CC} + 0.5$	
		V_{IL}	-0.5	-	0.8	V
Ambient operating temperature	commercial	T_A	0	-	70	°C
	industrial	T_A	-40	-	85	°C

V_{IL} min = -1.0V for pulse width less than 5ns

V_{IH} max = $V_{CC} + 2.0V$ for pulse width less than 5ns.

DC operating characteristics (over the operating range)¹

Parameter	Sym	Test conditions	-10		-12		-15		-20		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND to } V_{CC}$	-	1	-	1	-	1	-	1	μA
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}$ $V_{OUT} = \text{GND to } V_{CC}$	-	1	-	1	-	1	-	1	μA
Operating power supply current	I_{CC}	$V_{CC} = \text{Max}, \overline{CE} \leq V_{IL}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	-	110	-	100	-	90	-	80	mA
Standby power supply current	I_{SB}	$V_{CC} = \text{Max}, \overline{CE} \geq V_{IH}$ $f = f_{\text{Max}}$	-	50	-	45	-	45	-	40	mA
	I_{SB1}	$V_{CC} = \text{Max}, \overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V, f = 0$	-	10	-	10	-	10	-	10	mA
Output voltage	V_{OL}	$I_{OL} = 8\text{ mA}, V_{CC} = \text{Min}$	-	0.4	-	0.4	-	0.4	-	0.4	V
	V_{OH}	$I_{OH} = -4\text{ mA}, V_{CC} = \text{Min}$	2.4	-	2.4	-	2.4	-	2.4	-	V

Capacitance ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$, $V_{CC} = \text{NOMINAL}$)²

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	$V_{in} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out} = 0V$	7	pF

Read cycle (over the operating range)^{3,9}

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	-	12	-	15	-	20	-	ns	
Address access time	t_{AA}	-	10	-	12	-	15	-	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	-	10	-	12	-	15	-	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	-	5	-	6	-	7	-	8	ns	
Output hold from address change	t_{OH}	3	-	3	-	3	-	3	-	ns	5

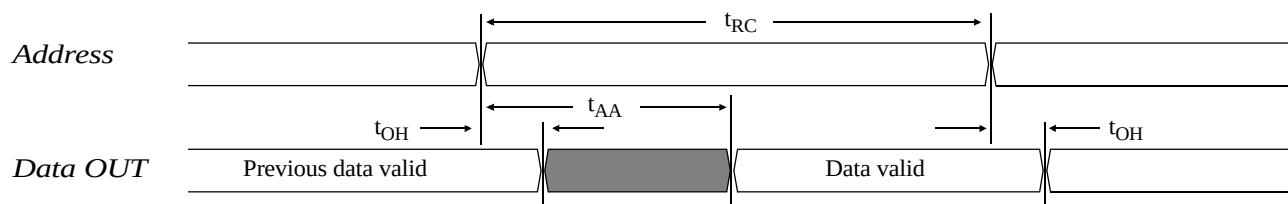


Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CE}$ low to output in low Z	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4, 5
$\overline{CE}$ high to output in high Z	t_{CHZ}	—	4	—	5	—	6	—	7	ns	4, 5
$\overline{OE}$ low to output in low Z	t_{OLZ}	0	—	0	—	0	—	0	—	ns	4, 5
Byte select access time	t_{BA}	—	5	—	6	—	7	—	8	ns	
Byte select Low to low Z	t_{BLZ}	0	—	0	—	0	—	0	—	ns	4, 5
Byte select High to high Z	t_{BHZ}	—	5	—	6	—	6	—	7	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	—	4	—	5	—	6	—	7	ns	4, 5
Power up time	t_{PU}	0	—	0	—	0	—	0	—	ns	4, 5
Power down time	t_{PD}	—	10	—	12	—	15		20	ns	4, 5

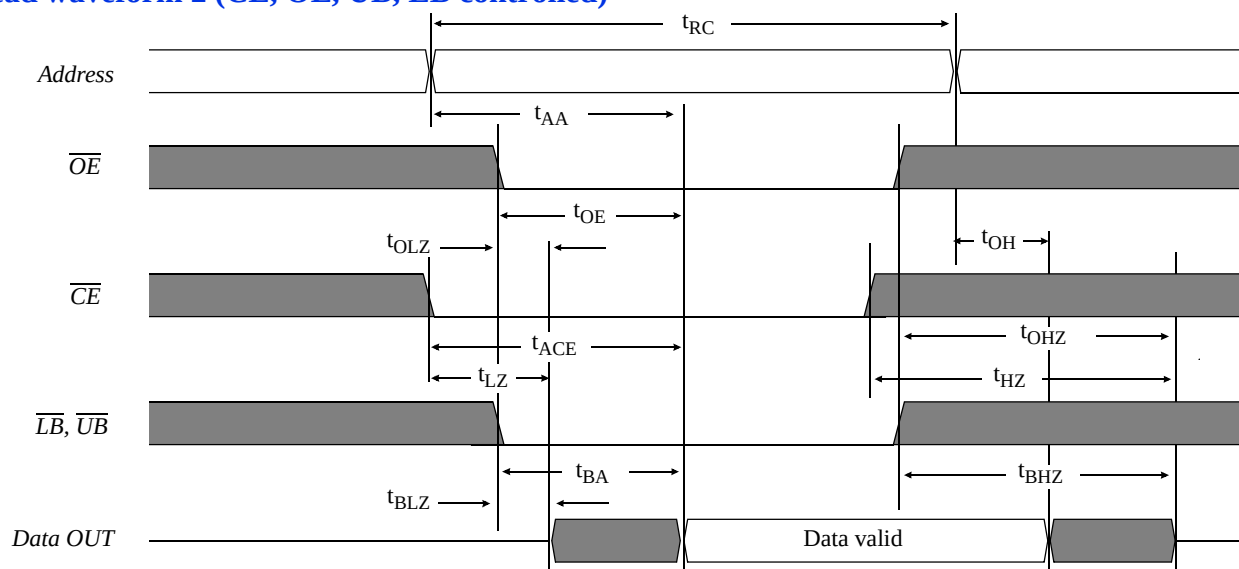
Key to switching waveforms

Rising input
 Falling input
 Undefined output/don't care

Read waveform 1 (address controlled)^{3,6,7,9}



Read waveform 2 ($\overline{CE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ controlled)^{3,6,8,9}



Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t _{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{\text{CE}}$) to write end	t _{CW}	8	–	9	–	10	–	12	–	ns	
Address setup to write end	t _{AW}	8	–	9	–	10	–	12	–	ns	
Address setup time	t _{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t _{WP}	7	–	8	–	9	–	12	–	ns	
Write recovery time	t _{WR}	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	t _{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t _{DW}	5	–	6	–	8	–	10	–	ns	
Data hold time	t _{DH}	0	–	0	–	0	–	0	–	ns	5
Write enable to output in high Z	t _{WZ}	–	5	–	6	–	7	–	8	ns	4, 5
Output active from write end	t _{OW}	1	–	1	–	1	–	2	–	ns	4, 5
Byte select low to end of write	t _{BW}	7	–	8	–	9	–	9	–	ns	

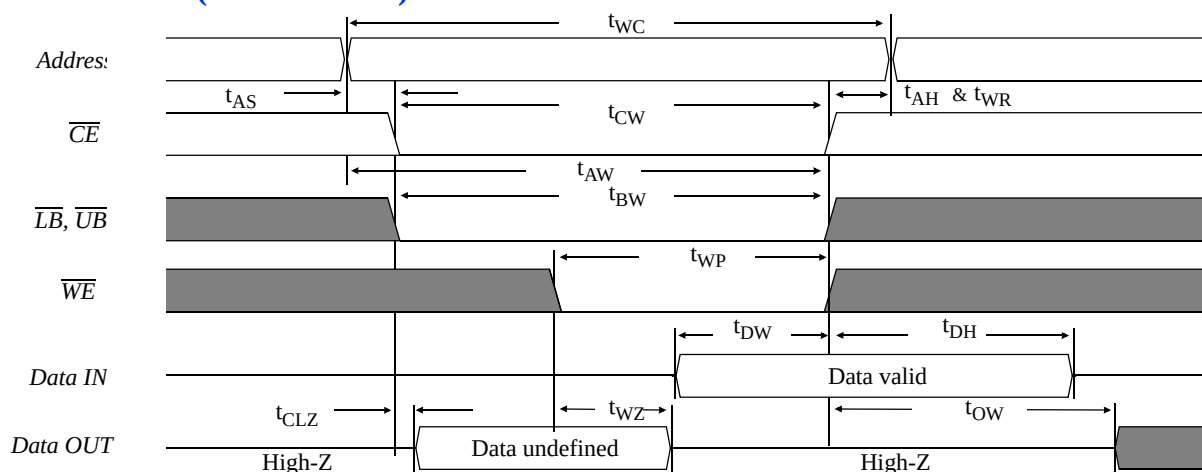
The diagram illustrates the timing relationships for a memory device. The signals shown are Address, $\overline{LB}$, $\overline{UB}$, $\overline{WE}$, Data IN, and Data OUT. The timing parameters are defined as follows:

- t_{WC} : Write Cycle time, from the start of the write operation to the end of the write operation.
- t_{BW} : Burst Width, from the start of the burst to the end of the burst.
- t_{WR} : Write Recovery time, from the end of the write operation to the start of the next read operation.
- t_{AS} : Address Setup time, from the start of the address to the start of the write operation.
- t_{AW} : Address Hold time, from the end of the address to the end of the write operation.
- t_{WP} : Write Pulse time, the duration of the write operation.
- t_{DW} : Data Write time, from the start of the data valid period to the end of the data valid period.
- t_{DH} : Data Hold time, from the end of the data valid period to the start of the next read operation.
- t_{WZ} : Write Z time, from the end of the data valid period to the start of the next read operation.
- t_{OW} : Output Write time, from the start of the data valid period to the end of the data valid period.

The Data IN signal is labeled "Data valid" during the write operation. The Data OUT signal is labeled "Data undefined" during the write operation and "High-Z" when the output is disabled.



Write waveform 2 ($\overline{\text{CE}}$ controlled)¹¹



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.5V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

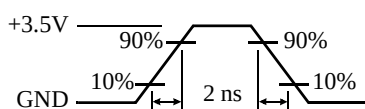


Figure A: Input pulse

Thevenin equivalent:

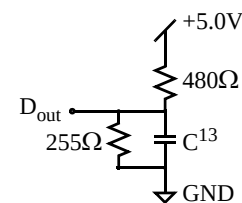
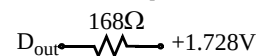


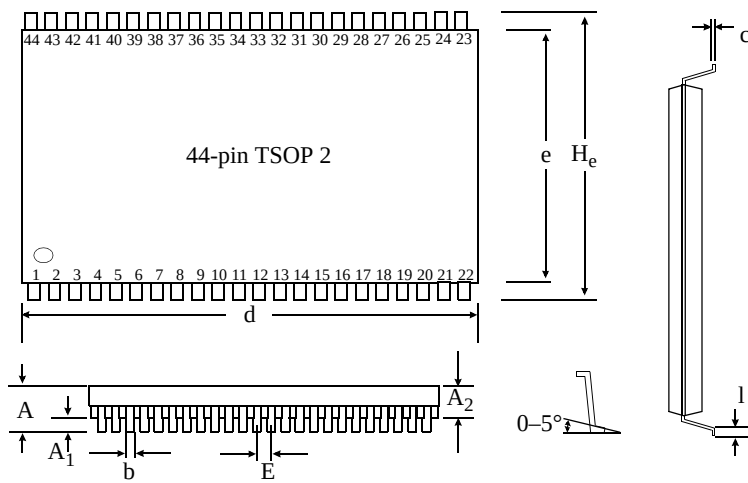
Figure B: 5.0V Output load

Notes

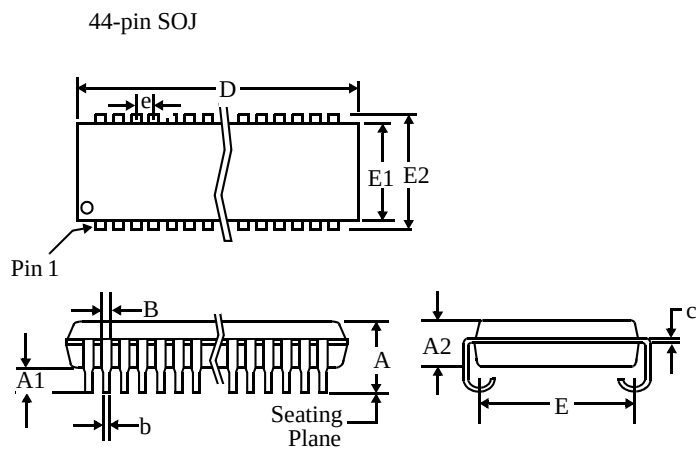
- During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{\text{CE}}$ is required to meet I_{SB} specification.
- This parameter is sampled, but not 100% tested.
- For test conditions, see *AC Test Conditions*, Figures A and B.
- These parameters are specified with $C_L = 5\text{pF}$, as in Figure B. Transition is measured $\pm 500\text{mV}$ from steady-state voltage.
- This parameter is guaranteed, but not 100% tested.
- $\overline{\text{WE}}$ is High for read cycle.
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are Low for read cycle.
- Address valid prior to or coincident with $\overline{\text{CE}}$ transition Low.
- All read cycle timings are referenced from the last valid address to the first transitioning address.
- Not applicable.
- All write cycle timings are referenced from the last valid address to the first transitioning address.
- Not applicable.
- $C = 30\text{pF}$, except on High Z and Low Z parameters, where $C = 5\text{pF}$.



Package dimensions



Symbol	44-pin TSOP 2	
	Min (mm)	Max (mm)
A		1.2
A ₁	0.05	0.15
A ₂	0.95	1.05
b	0.3	0.45
c	0.12	0.21
d	18.31	18.52
e	10.06	10.26
H _e	11.68	11.94
E	0.80 (typical)	
l	0.40	0.60



Symbol	44-pin SOJ 400 mil	
	Min	Max
A	0.128	0.148
A ₁	0.025	-
A ₂	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E ₁	0.395	0.405
E ₂	0.435	0.445
e	0.050 NOM	



Ordering codes

Package\Access time		10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 400 mil	Commercial	AS7C513B-10JC	AS7C513B-12JC	AS7C513B-15JC	AS7C513B-20JC
	Industrial	AS7C513B-10JI	AS7C513B-12JI	AS7C513B-15JI	AS7C513B-20JI
TSOP 2, 18.4×10.2 mm	Commercial	AS7C513B-10TC	AS7C513B-12TC	AS7C513B-15TC	AS7C513B-20TC
	Industrial	AS7C513B-10TI	AS7C513B-12TI	AS7C513B-15TI	AS7C513B-20TI

Part numbering system

AS7C	513B	-XX	X	C
SRAM prefix	Device number	Access time	Package: J = SOJ 400 mil T = TSOP 2 18.4×10.2 mm	Temperature range: C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C



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