

# MOSFET – Power, Single, N-Channel

**40 V, 1.4 mΩ, 200 A**

**NVMJS1D5N04CL**

## Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- LFPK8 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

## MAXIMUM RATINGS ( $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	40	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	200	A
		$T_C = 100\text{ }^{\circ}\text{C}$		140	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25\text{ }^{\circ}\text{C}$	$P_D$	110	W
		$T_C = 100\text{ }^{\circ}\text{C}$		53	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25\text{ }^{\circ}\text{C}$	$I_D$	38	A
		$T_A = 100\text{ }^{\circ}\text{C}$		27	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25\text{ }^{\circ}\text{C}$	$P_D$	3.8	W
		$T_A = 100\text{ }^{\circ}\text{C}$		1.9	
Pulsed Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$ , $t_p = 10\text{ }\mu\text{s}$		$I_{DM}$	900	A
Operating Junction and Storage Temperature			$T_J, T_{stg}$	$-55$ to $+175$	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	120	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 15\text{ A}$ )			$E_{AS}$	493	mJ
Single Pulse Drain-to-Source Voltage ( $t_p = 10\text{ }\mu\text{s}$ )			$V_{DSM}$	48	V
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

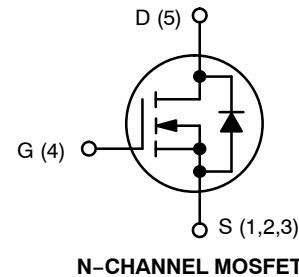
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL RESISTANCE MAXIMUM RATINGS

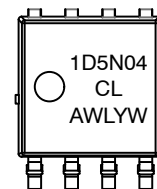
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	1.4	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	36	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	1.4 mΩ @ 10 V	200 A
	2.2 mΩ @ 4.5 V	



## MARKING DIAGRAM



1D5N04CL = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
W = Work Week

## ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

# NVMJS1D5N04CL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			2.0		mV/ $^{\circ}\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25\text{ }^{\circ}\text{C}$		10	$\mu\text{A}$
			$T_J = 125\text{ }^{\circ}\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 130\text{ }\mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.6		mV/ $^{\circ}\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		1.7	2.2	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.2	1.4	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		256		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		4300		pF
Output Capacitance	$C_{OSS}$			1900		
Reverse Transfer Capacitance	$C_{RSS}$			72		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		32		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		70		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		7.0		
Gate-to-Source Charge	$Q_{GS}$			12		
Gate-to-Drain Charge	$Q_{GD}$			9.0		
Plateau Voltage	$V_{GP}$			2.9		V

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}, R_G = 1\text{ }\Omega$		15		ns
Rise Time	$t_r$			140		
Turn-Off Delay Time	$t_{d(OFF)}$			31		
Fall Time	$t_f$			9		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 50\text{ A}$	$T_J = 25\text{ }^{\circ}\text{C}$		0.81	1.2	V
			$T_J = 125\text{ }^{\circ}\text{C}$		0.68		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 50\text{ A}$			61		ns
Charge Time	$t_a$				29		
Discharge Time	$t_b$				32		
Reverse Recovery Charge	$Q_{RR}$				80		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

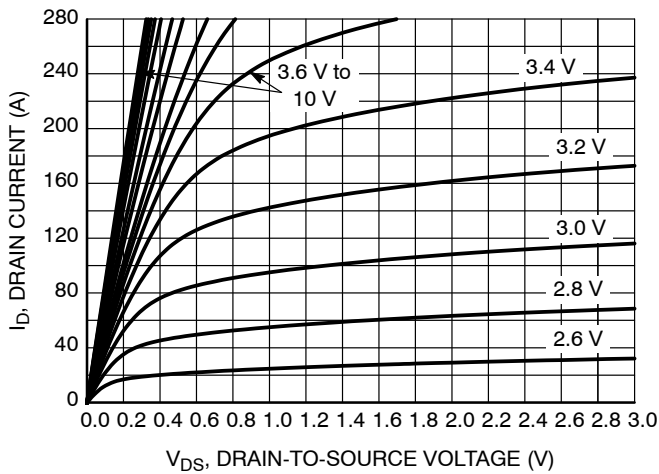


Figure 1. On-Region Characteristics

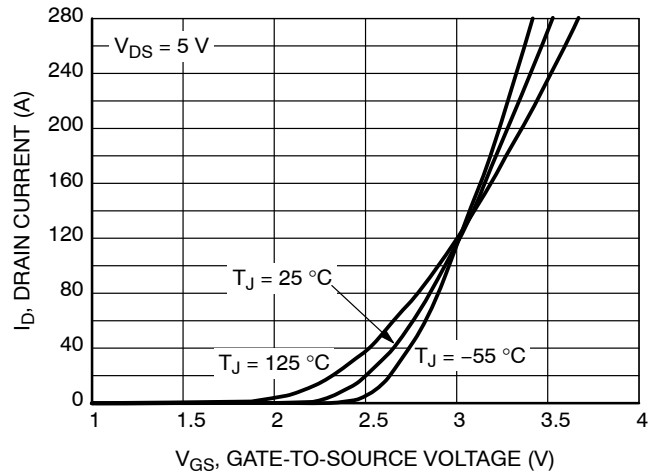


Figure 2. Transfer Characteristics

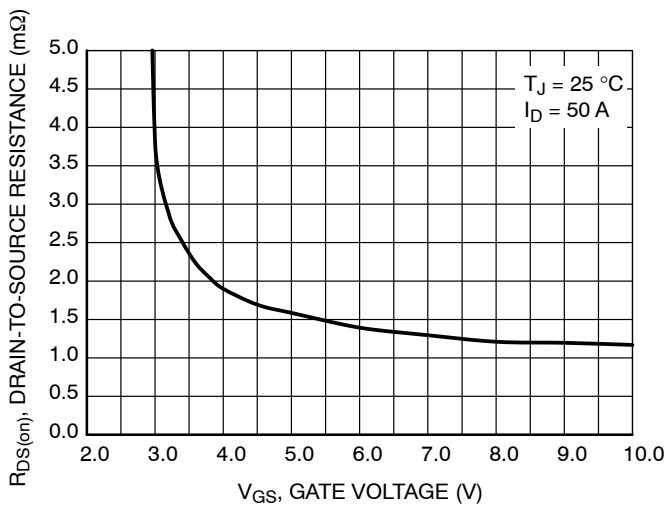


Figure 3. On-Resistance vs. Gate-to-Source Voltage

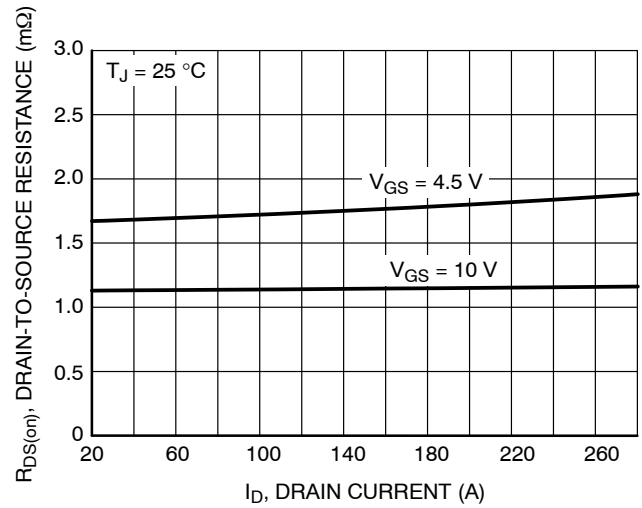


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

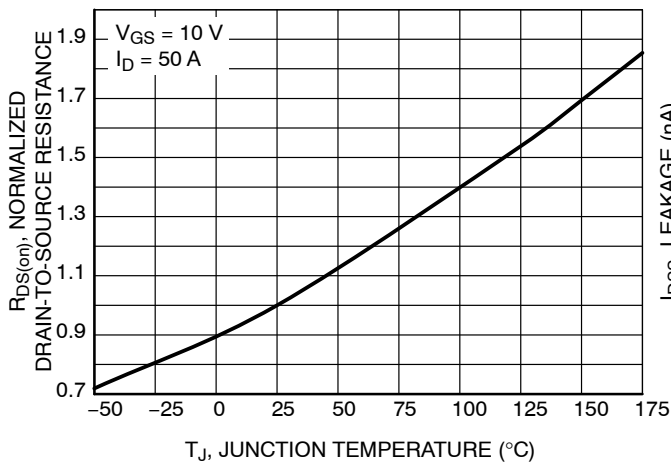


Figure 5. On-Resistance Variation with Temperature

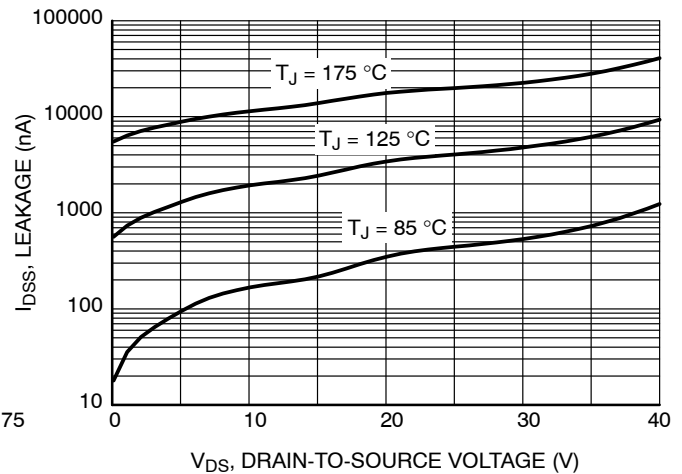


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL CHARACTERISTICS

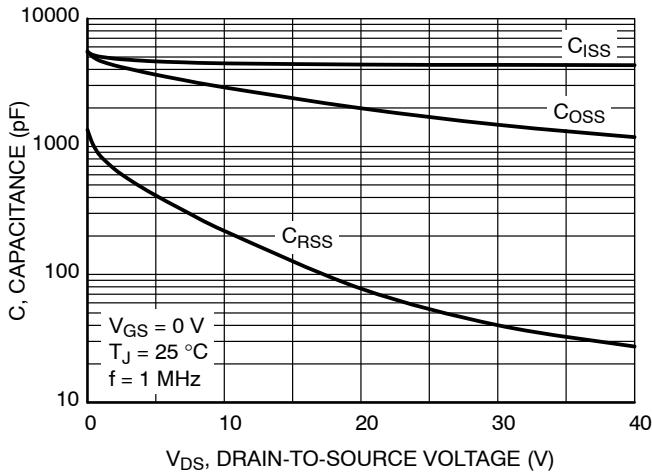


Figure 7. Capacitance Variation

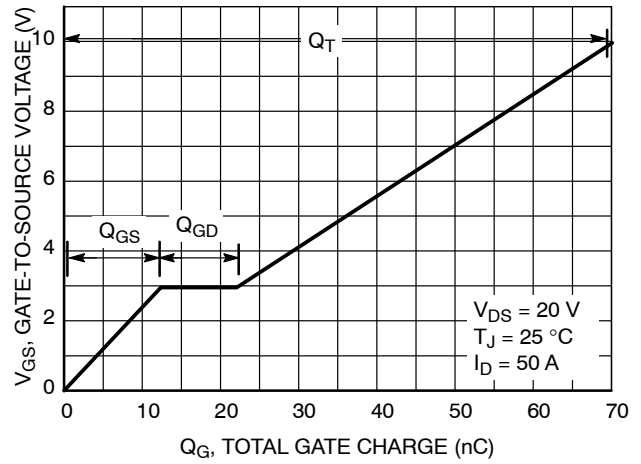


Figure 8. Gate-to-Source Voltage vs. Total Charge

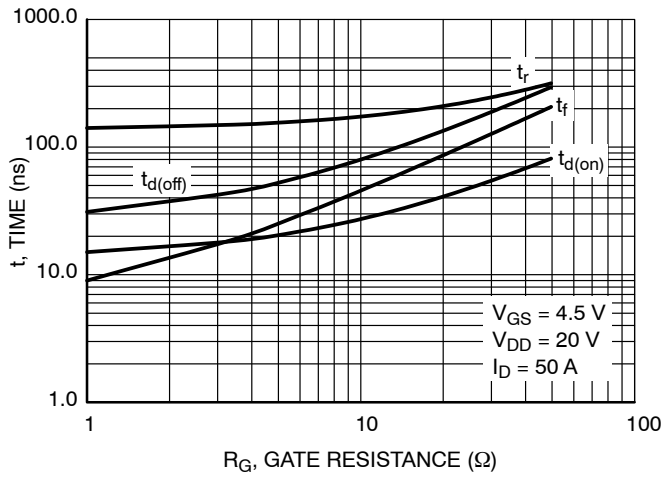


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

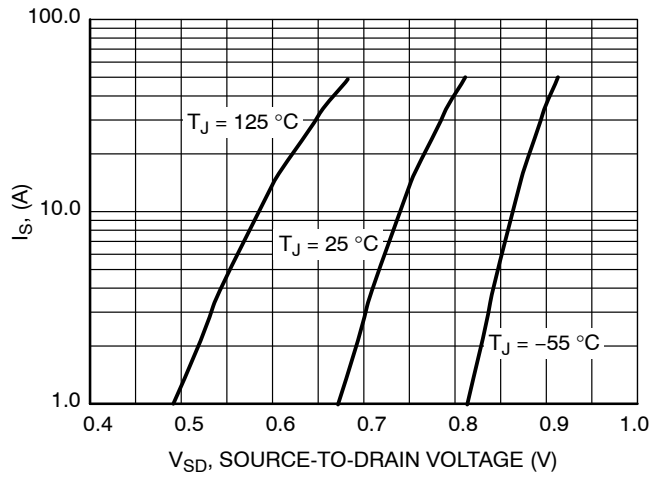


Figure 10. Diode Forward Voltage vs. Current

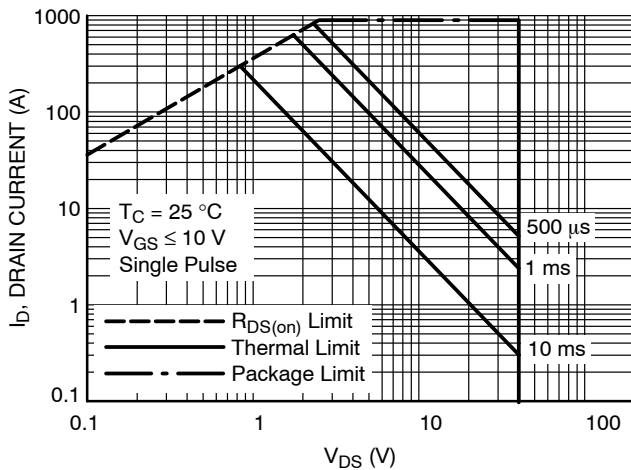


Figure 11. Safe Operating Area

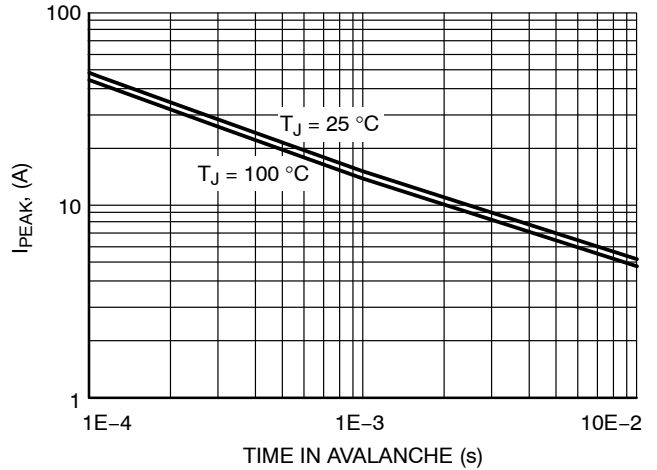


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVMJS1D5N04CL

## TYPICAL CHARACTERISTICS

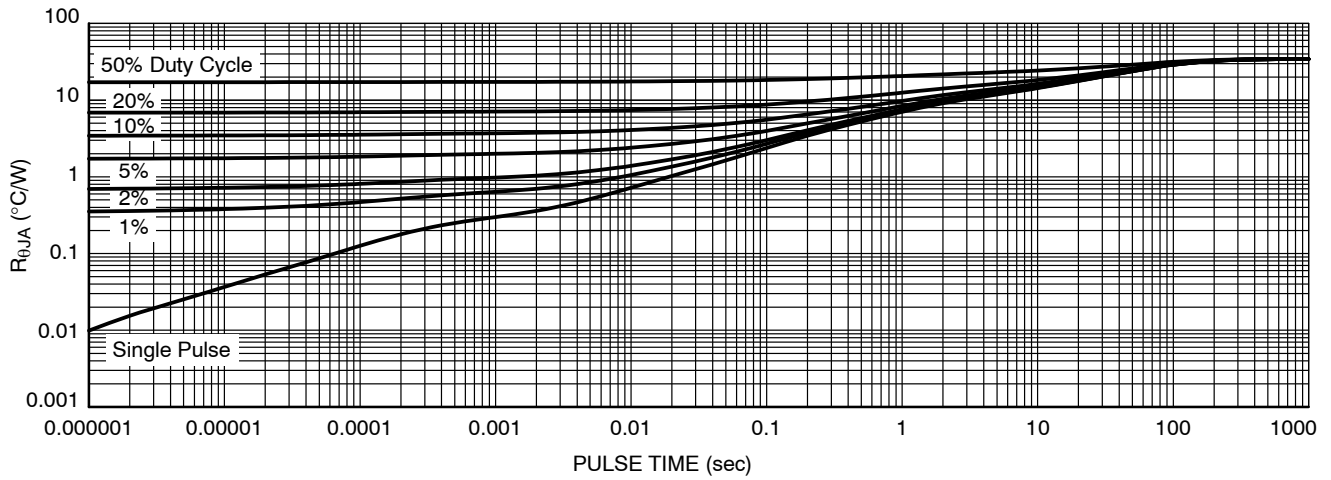


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVMJS1D5N04CLTWG	1D5N04CL	LFPAK8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

## NVMJS1D5N04CL

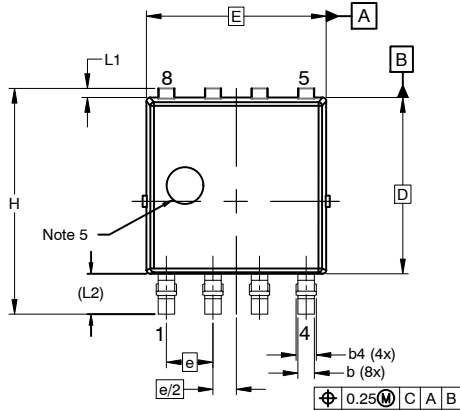
### REVISION HISTORY

Revision	Description of Changes	Date
0	Initial production document version release.	4/1/2019
1	Document rebranded to <b>onsemi</b> format.	11/14/2025

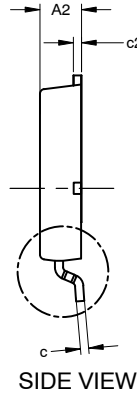


**LPAK8 4.90x4.80x1.12MM, 1.27P**  
CASE 760AA  
ISSUE D

DATE 22 APR 2024



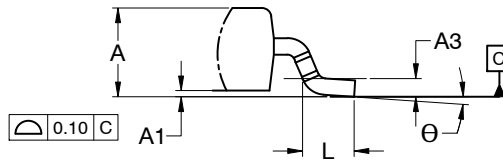
TOP VIEW



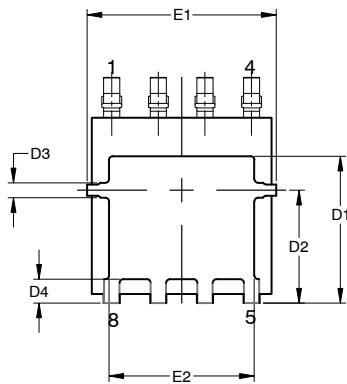
SIDE VIEW

NOTES:

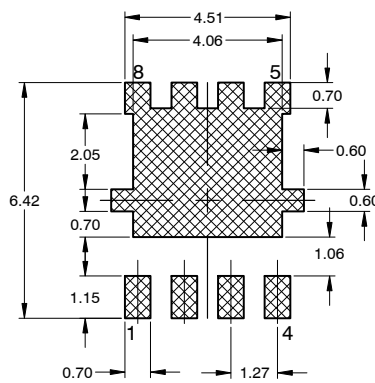
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.



DETAIL 'A'



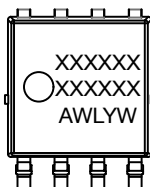
BOTTOM VIEW



RECOMMENDED LAND PAD

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	2.98	3.08	3.18
D3	0.30	0.40	0.50
D4	0.55	0.65	0.75
E	4.80	4.90	5.00
E1	5.05	5.15	5.25
E2	3.91	3.96	4.01
e	1.27 BSC		
e/2	0.635 BSC		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.15	0.25	0.35
L2	1.10 REF		
Θ	0°	4°	8°

**GENERIC  
MARKING DIAGRAM\***



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
W = Work Week

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

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