

Structure	Silicon monolithic Integrated circuit
Product	Clock Generator
Type	BU7346GUL
Feature	To generate clocks for digital still camera system To generate clocks by connecting reference 27.0000MHz SEL pin allowing for the selection of 38.0000MHz or 36.0000MHz Selection of PDB pin enabling Power-Down function

○Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 ~ 4.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Storage Temperature range	Tstg	-55 ~ 125	°C
Power dissipation	PD	460 ^{※1}	mW

※1 A measure value at mounting on 50mm×58mm×1.75mm glass epoxy substrate.

In the case of exceeding Ta=25°C, 4.6mW should be reduced per 1°C.

※ Operation is not guaranteed.

※ The radiation-resistance design is not carried out.

○Operating Conditions (Ta=-5°C~+75°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	2.7	3.3	3.6	V
Input "H" Voltage	VIH	0.8VDD	-	VDD	V
Input "L" Voltage	VIL	0.0	-	0.2VDD	V
Output load	CL	0	-	15	pF

○Electrical Characteristics

(VDD=3.3V, Ta=25°C, Input frequency=27.0000MHz, at No Load, unless otherwise specified)

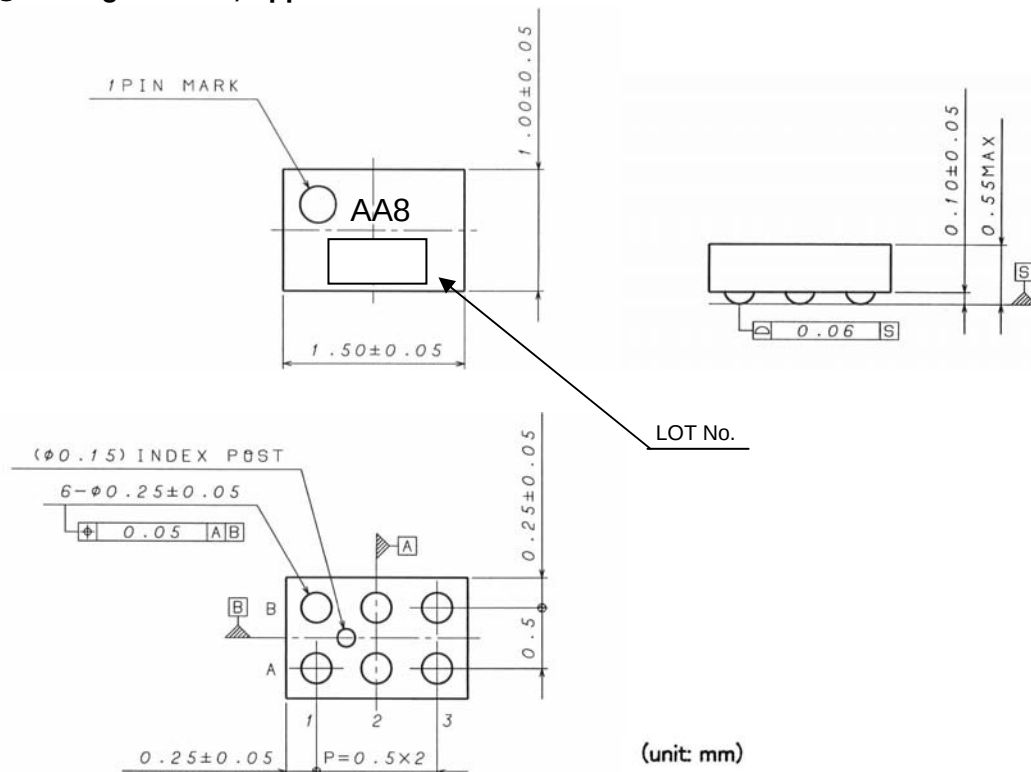
Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Output H voltage	VOH	2.8	-	VDD	V	IOH=-3.0mA
Output L voltage	VOL	0.0	-	0.5	V	IOL=3.0mA
Standby current	IDDst	-	-	1.0	μA	PDB=L
Consumption current1	IDD1	-	3.5	4.6	mA	38.0000MHz Output, SEL=L
Consumption current2	IDD2	-	3.5	4.6	mA	36.0000MHz Output, SEL=H
Pull-down load	Rpd	50	100	200	kΩ	Input PIN pull-down load value

○Output Frequency

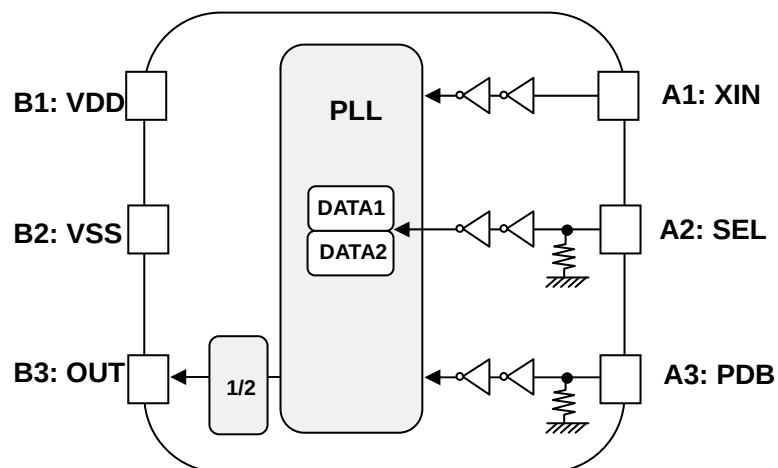
(VDD=3.3V, Ta=25°C, Input frequency=27.0000MHz, unless otherwise specified)

Parameter	Symbol	Output Frequency	Unit	Conditions
OUT1	CLK38	38.0000	MHz	PDB=H, SEL=L XIN×(76/27)/2
OUT2	CLK36	36.0000	MHz	PDB=H, SEL=H XIN×(8/3)/2

○Package outline, Appearance of Marker



○Block diagram, pin function



VDD=3.3V, Ta=25°C, XIN=27.0000MHz
 38.0000MHz output ($OUT = XIN \times (76/27)/2$) as SEL=L
 36.0000MHz output ($OUT = XIN \times (8/3)/2$) as SEL=H

PIN No.	PIN NAME	Function
A1	XIN	Clock input pin (27.0000MHz input)
A2	SEL	SEL pin (L : 38.0000MHz, H : 36.0000MHz), Equipment with pull-down function (Typ.100kΩ)
A3	PDB	Power down (L : disable, H : enable), Equipment with pull-down function (Typ.100kΩ) Output fixed to L at disable
B1	VDD	Power supply
B2	VSS	GND
B3	OUT	Clock output terminal (SEL=L : 38.0000MHz, SEL=H : 36.0000MHz)

●Cautions on use (BU7346GUL)

Basically, mount ICs to the printed circuit board for use. (If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)

Mount 0.1μF capacitors in the vicinity of the IC PINs between B1 PIN(VDD) and B2 PIN(VSS), respectively.

Depending on the conditions of the printed circuit board, mount an additional electrolytic capacitor between the power supply and GND terminal.

For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to BU7346GUL from the printed circuit board or to insert a capacitor (of 1Ω or less), which bypasses high frequency desired, between the power supply and the GND terminal.

When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

●Cautions on use (common)

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies have the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(1 0) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(1 1) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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