

IS41C16100

IS41LV16100

ISSI®

1M x 16 (16-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

April 2003

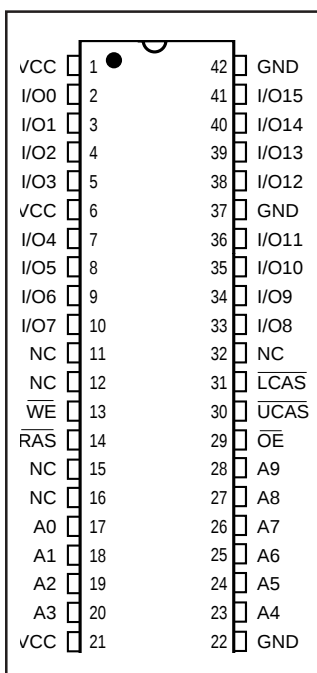
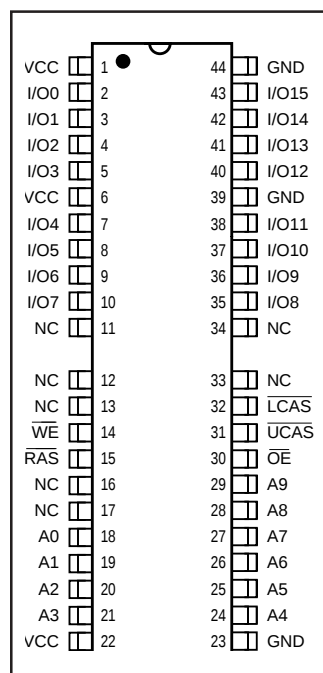
FEATURES

- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval:
 - *Auto refresh Mode*: 1,024 cycles /16 ms
 - *RAS-Only, CAS-before-RAS (CBR), and Hidden*
 - *Self refresh Mode* - 1,024 cycles / 128ms
- JEDEC standard pinout
- Single power supply:
 - 5V $\pm$ 10% (IS41C16100)
 - 3.3V $\pm$ 10% (IS41LV16100)
- Byte Write and Byte Read operation via two $\overline{\text{CAS}}$
- Industrail Temperature Range -40°C to 85°C

PIN CONFIGURATIONS

50(44)-Pin TSOP (Type II)

42-Pin SOJ



DESCRIPTION

The ISSI IS41C16100 and IS41LV16100 are 1,048,576 x 16-bit high-performance CMOS Dynamic Random Access Memories. These devices offer an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 1,024 random accesses within a single row with access cycle time as short as 20 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes the IS41C16100 ideal for use in 16-bit and 32-bit wide data bus systems.

These features make the IS41C16100 and IS41LV16100 ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS41C16100 and IS41LV16100 are packaged in a 42-pin 400-mil SOJ and 400-mil 50- (44-) pin TSOP (Type II). The lead-free 400-mil 50- (44-) option is available too.

KEY TIMING PARAMETERS

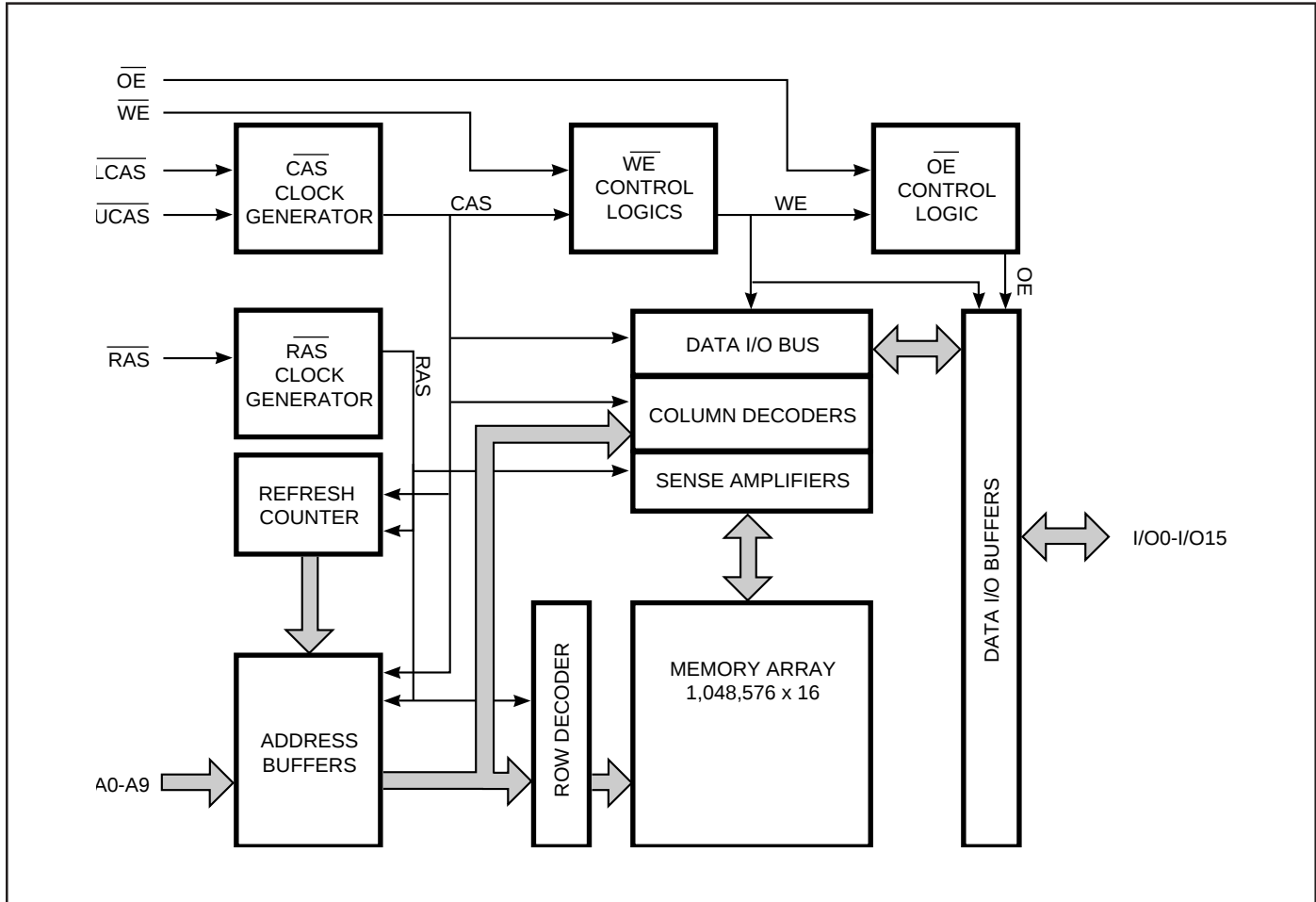
Parameter	-50	-60	Unit
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	50	60	ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	13	15	ns
Max. Column Address Access Time (t_{AA})	25	30	ns
Min. EDO Page Mode Cycle Time (t_{PC})	20	25	ns
Min. Read/Write Cycle Time (t_{RC})	84	104	ns

PIN DESCRIPTIONS

A0-A9	Address Inputs
I/O0-15	Data Inputs/Outputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Upper Column Address Strobe
$\overline{\text{LCAS}}$	Lower Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

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FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function		$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Address t _R /t _C	I/O
Standby		H	H	H	X	X	X	High-Z
Read: Word		L	L	L	H	L	ROW/COL	D _{OUT}
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte, D _{OUT} Upper Byte, High-Z
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, D _{OUT}
Write: Word (Early Write)		L	L	L	L	X	ROW/COL	D _{IN}
Write: Lower Byte (Early Write)		L	L	H	L	X	ROW/COL	Lower Byte, D _{IN} Upper Byte, High-Z
Write: Upper Byte (Early Write)		L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, D _{IN}
Read-Write ^(1,2)		L	L	L	H→L	L→H	ROW/COL	D _{OUT} , D _{IN}
EDO Page-Mode Read ⁽²⁾	1st Cycle:	L	H→L	H→L	H	L	ROW/COL	D _{OUT}
	2nd Cycle:	L	H→L	H→L	H	L	NA/COL	D _{OUT}
	Any Cycle:	L	L→H	L→H	H	L	NA/NA	D _{OUT}
EDO Page-Mode Write ⁽¹⁾	1st Cycle:	L	H→L	H→L	L	X	ROW/COL	D _{IN}
	2nd Cycle:	L	H→L	H→L	L	X	NA/COL	D _{IN}
EDO Page-Mode ^(1,2) Read-Write	1st Cycle:	L	H→L	H→L	H→L	L→H	ROW/COL	D _{OUT} , D _{IN}
	2nd Cycle:	L	H→L	H→L	H→L	L→H	NA/COL	D _{OUT} , D _{IN}
Hidden Refresh	Read ⁽²⁾	L→H→L	L	L	H	L	ROW/COL	D _{OUT}
	Write ^(1,3)	L→H→L	L	L	L	X	ROW/COL	D _{OUT}
RAS-Only Refresh		L	H	H	X	X	ROW/NA	High-Z
CBR Refresh ⁽⁴⁾		H→L	L	L	X	X	X	High-Z

Notes:

1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{\text{CAS}}$ signals must be active ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$).

Functional Description

The IS41C16100 and IS41LV16100 is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits. These are entered ten bits (A0-A9) at a time. The row address is latched by the Row Address Strobe ($\overline{\text{RAS}}$). The column address is latched by the Column Address Strobe ($\overline{\text{CAS}}$). $\overline{\text{RAS}}$ is used to latch the first nine bits and $\overline{\text{CAS}}$ is used to latch the latter nine bits.

The IS41C16100 and IS41LV16100 has two $\overline{\text{CAS}}$ controls, $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$. The $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ inputs internally generate a $\overline{\text{CAS}}$ signal functioning in an identical manner to the single $\overline{\text{CAS}}$ input on the other 1M x 16 DRAMs. The key difference is that each $\overline{\text{CAS}}$ controls its corresponding I/O tristate logic (in conjunction with $\overline{\text{OE}}$ and $\overline{\text{WE}}$ and $\overline{\text{RAS}}$). $\overline{\text{LCAS}}$ controls I/O0 through I/O7 and $\overline{\text{UCAS}}$ controls I/O8 through I/O15.

The IS41C16100 and IS41LV16100 $\overline{\text{CAS}}$ function is determined by the first $\overline{\text{CAS}}$ ($\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$) transitioning LOW and the last transitioning back HIGH. The two $\overline{\text{CAS}}$ controls give the IS41C16100 and IS41LV16100 both BYTE READ and BYTE WRITE cycle capabilities.

Memory Cycle

A memory cycle is initiated by bringing $\overline{\text{RAS}}$ LOW and it is terminated by returning both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH. To ensure proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. A new cycle must not be initiated until the minimum precharge time t_{RP} , t_{CP} has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{OE}}$, whichever occurs last, while holding $\overline{\text{WE}}$ HIGH. The column address must be held for a minimum time specified by t_{AR} . Data Out becomes valid only when t_{RAC} , t_{AA} , t_{CAC} and t_{OEA} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs first.

Auto Refresh Cycle

To retain data, 1,024 refresh cycles are required in each 16 ms period. There are two ways to refresh the memory.

1. By clocking each of the 1,024 row addresses (A0 through A9) with $\overline{\text{RAS}}$ at least once every 128 ms. Any read, write, read-modify-write or $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is activated by the falling edge of $\overline{\text{RAS}}$,

while holding $\overline{\text{CAS}}$ LOW. In $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Self Refresh Cycle

The Self Refresh allows the user a dynamic refresh, data retention mode at the extended refresh period of 128 ms. i.e., 125 μs per row when using distributed CBR refreshes. The feature also allows the user the choice of a fully static, low power data retention mode. The optional Self Refresh feature is initiated by performing a CBR Refresh cycle and holding $\overline{\text{RAS}}$ LOW for the specified t_{RAS} .

The Self Refresh mode is terminated by driving $\overline{\text{RAS}}$ HIGH for a minimum time of t_{RP} . This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{\text{RAS}}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting Self Refresh.

However, if the DRAM controller utilizes a $\overline{\text{RAS}}$ -only or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

Extended Data Out Page Mode

EDO page mode operation permits all 1,024 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next $\overline{\text{CAS}}$ cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the $\overline{\text{CAS}}$ cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{\text{CAS}}$ cycle time becomes shorter.

In EDO page mode, due to the extended data function, the $\overline{\text{CAS}}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one $\overline{\text{RAS}}$ cycle, but the performance is equivalent to that of the fast page mode in that case.

Power-On

After application of the V_{CC} supply, an initial pause of 200 μs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ signal).

During power-on, it is recommended that $\overline{\text{RAS}}$ track with V_{CC} or be held at a valid V_{IH} to avoid current surges.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameters	Rating	Unit
V _T	Voltage on Any Pin Relative to GND	5V 3.3V	–1.0 to +7.0 –0.5 to +4.6 V
V _{CC}	Supply Voltage	5V 3.3V	–1.0 to +7.0 –0.5 to +4.6 V
I _{OUT}	Output Current	50	mA
P _D	Power Dissipation	1	W
T _A	Commercial Operation Temperature Industrial Operating Temperature	0 to +70 –40 to +85	°C °C
T _{STG}	Storage Temperature	–55 to +125	°C

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	5V 3.3V	4.5 3.0	5.0 3.3	5.5 3.6 V
V _{IH}	Input High Voltage	5V 3.3V	2.4 2.0	— —	V _{CC} + 1.0 V _{CC} + 0.3 V
V _{IL}	Input Low Voltage	5V 3.3V	–1.0 –0.3	— —	0.8 0.8 V
T _A	Commercial Ambient Temperature Industrial Ambient Temperature	0 –40	— —	70 85	°C °C

CAPACITANCE^(1,2)

Symbol	Parameter	Max.	Unit
C _{IN1}	Input Capacitance: A0-A9	5	pF
C _{IN2}	Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	7	pF
C _{IO}	Data Input/Output Capacitance: I/O0-I/O15	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

ELECTRICAL CHARACTERISTICS⁽¹⁾

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I _{IL}	Input Leakage Current	Any input $0V \leq V_{IN} \leq V_{CC}$ Other inputs not under test = 0V		-5	5	μA
I _{IO}	Output Leakage Current	Output is disabled (Hi-Z) $0V \leq V_{OUT} \leq V_{CC}$		-5	5	μA
V _{OH}	Output High Voltage Level	I _{OH} = -5.0 mA (5V) I _{OH} = -2.0 mA (3.3V)		2.4	—	V
V _{OL}	Output Low Voltage Level	I _{OL} = 4.2 mA (5V) I _{OL} = 2.0 mA (3.3V)		—	0.4	V
I _{CC1}	Standby Current: TTL	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{IH}$ Commercial	5V	—	3	mA
			3.3V	—	3	
		Industrial	5V	—	4	mA
			3.3V	—	4	
I _{CC2}	Standby Current: CMOS	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{CC} - 0.2V$	5V	—	2	mA
			3.3V	—	2	
I _{CC3}	Operating Current: Random Read/Write ^(2,3,4) Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS}$, Address Cycling, $t_{RC} = t_{RC} \text{ (min.)}$	-50	—	160	mA
			-60	—	145	
I _{CC4}	Operating Current: EDO Page Mode ^(2,3,4) Average Power Supply Current	$\overline{RAS} = V_{IL}, \overline{LCAS}, \overline{UCAS}$, Cycling $t_{PC} = t_{PC} \text{ (min.)}$	-50	—	90	mA
			-60	—	80	
I _{CC5}	Refresh Current: $\overline{RAS}$ -Only ^(2,3) Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{LCAS}, \overline{UCAS} \geq V_{IH}$ $t_{RC} = t_{RC} \text{ (min.)}$	-50	—	160	mA
			-60	—	145	
I _{CC6}	Refresh Current: CBR ^(2,3,5) Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS}$ Cycling $t_{RC} = t_{RC} \text{ (min.)}$	-50	—	160	mA
			-60	—	145	

Notes:

1. An initial pause of 200 μs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS (1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50		-60		Units
		Min.	Max.	Min.	Max.	
t _{RC}	Random READ or WRITE Cycle Time	84	—	104	—	ns
t _{RAC}	Access Time from $\overline{\text{RAS}}$ ^(6, 7)	—	50	—	60	ns
t _{CAC}	Access Time from $\overline{\text{CAS}}$ ^(6, 8, 15)	—	13	—	15	ns
t _{AA}	Access Time from Column-Address ⁽⁶⁾	—	25	—	30	ns
t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	50	10K	60	10K	ns
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	30	—	40	—	ns
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width ⁽²⁶⁾	8	10K	10	10K	ns
t _{CP}	$\overline{\text{CAS}}$ Precharge Time ^(9, 25)	9	—	9	—	ns
t _{CSH}	$\overline{\text{CAS}}$ Hold Time ⁽²¹⁾	38	—	40	—	ns
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time ^(10, 20)	12	37	14	45	ns
t _{ASR}	Row-Address Setup Time	0	—	0	—	ns
t _{RAH}	Row-Address Hold Time	8	—	10	—	ns
t _{ASC}	Column-Address Setup Time ⁽²⁰⁾	0	—	0	—	ns
t _{CAH}	Column-Address Hold Time ⁽²⁰⁾	8	—	10	—	ns
t _{AR}	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$)	30	—	40	—	ns
t _{RAD}	$\overline{\text{RAS}}$ to Column-Address Delay Time ⁽¹¹⁾	10	25	12	30	ns
t _{RAL}	Column-Address to $\overline{\text{RAS}}$ Lead Time	25	—	30	—	ns
t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	5	—	5	—	ns
t _{RSH}	$\overline{\text{RAS}}$ Hold Time ⁽²⁷⁾	8	—	10	—	ns
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	37	—	37	—	ns
t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z ^(15, 29)	0	—	0	—	ns
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time ⁽²¹⁾	5	—	5	—	ns
t _{OD}	Output Disable Time ^(19, 28, 29)	3	15	3	15	ns
t _{OE}	Output Enable Time ^(15, 16)	—	13	—	15	ns
t _{OED}	Output Enable Data Delay (Write)	20	—	20	—	ns
t _{OEHC}	$\overline{\text{OE}}$ HIGH Hold Time from $\overline{\text{CAS}}$ HIGH	5	—	5	—	ns
t _{OEP}	$\overline{\text{OE}}$ HIGH Pulse Width	10	—	10	—	ns
t _{OES}	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	5	—	ns
t _{RCS}	Read Command Setup Time ^(17, 20)	0	—	0	—	ns
t _{RRH}	Read Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹²⁾	0	—	0	—	ns
t _{RCH}	Read Command Hold Time (referenced to $\overline{\text{CAS}}$) ^(12, 17, 21)	0	—	0	—	ns
t _{WCH}	Write Command Hold Time ^(17, 27)	8	—	10	—	ns
t _{WCR}	Write Command Hold Time (referenced to $\overline{\text{RAS}}$) ⁽¹⁷⁾	40	—	50	—	ns

AC CHARACTERISTICS (Continued)^(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50		-60		Units
		Min.	Max.	Min.	Max.	
tWP	Write Command Pulse Width ⁽¹⁷⁾	8	—	10	—	ns
tWPZ	$\overline{WE}$ Pulse Widths to Disable Outputs	10	—	10	—	ns
tRWL	Write Command to $\overline{RAS}$ Lead Time ⁽¹⁷⁾	13	—	15	—	ns
tcWL	Write Command to $\overline{CAS}$ Lead Time ^(17, 21)	8	—	10	—	ns
twCS	Write Command Setup Time ^(14, 17, 20)	0	—	0	—	ns
tDHR	Data-in Hold Time (referenced to $\overline{RAS}$)	39	—	39	—	ns
tACH	Column-Address Setup Time to $\overline{CAS}$ Precharge during WRITE Cycle	15	—	15	—	ns
toEH	$\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle ⁽¹⁸⁾	8	—	10	—	ns
tDS	Data-In Setup Time ^(15, 22)	0	—	0	—	ns
tDH	Data-In Hold Time ^(15, 22)	8	—	10	—	ns
tRWC	READ-MODIFY-WRITE Cycle Time	108	—	133	—	ns
tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle ⁽¹⁴⁾	64	—	77	—	ns
tcWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time ^(14, 20)	26	—	32	—	ns
tAWD	Column-Address to $\overline{WE}$ Delay Time ⁽¹⁴⁾	39	—	47	—	ns
tPC	EDO Page Mode READ or WRITE Cycle Time ⁽²⁴⁾	20	—	25	—	ns
tRASP	$\overline{RAS}$ Pulse Width in EDO Page Mode	50	100K	60	100K	ns
tCPA	Access Time from $\overline{CAS}$ Precharge ⁽¹⁵⁾	—	30	—	35	ns
tPRWC	EDO Page Mode READ-WRITE Cycle Time ⁽²⁴⁾	56	—	68	—	ns
tCOH	Data Output Hold after $\overline{CAS}$ LOW	5	—	5	—	ns
tOFF	Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$ ^(13,15,19, 29)	1.6	12	1.6	15	ns
tWHZ	Output Disable Delay from $\overline{WE}$	3	10	3	10	ns
tCLCH	Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ returning HIGH ⁽²³⁾	10	—	10	—	ns
tCSR	$\overline{CAS}$ Setup Time (CBR REFRESH) ^(30, 20)	5	—	5	—	ns
tCHR	$\overline{CAS}$ Hold Time (CBR REFRESH) ^(30, 21)	8	—	10	—	ns
tORD	$\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle	0	—	0	—	ns
tREF	Auto Refresh Period (1,024 Cycles)	—	16	—	16	ms
tREF	Self Refresh Period (1,024 Cycles)	—	128	—	128	ms
tr	Transition Time (Rise or Fall) ^(2, 3)	1	50	1	50	ns

AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF ($V_{CC} = 5.0V \pm 10\%$)
 One TTL Load and 50 pF ($V_{CC} = 3.3V \pm 10\%$)

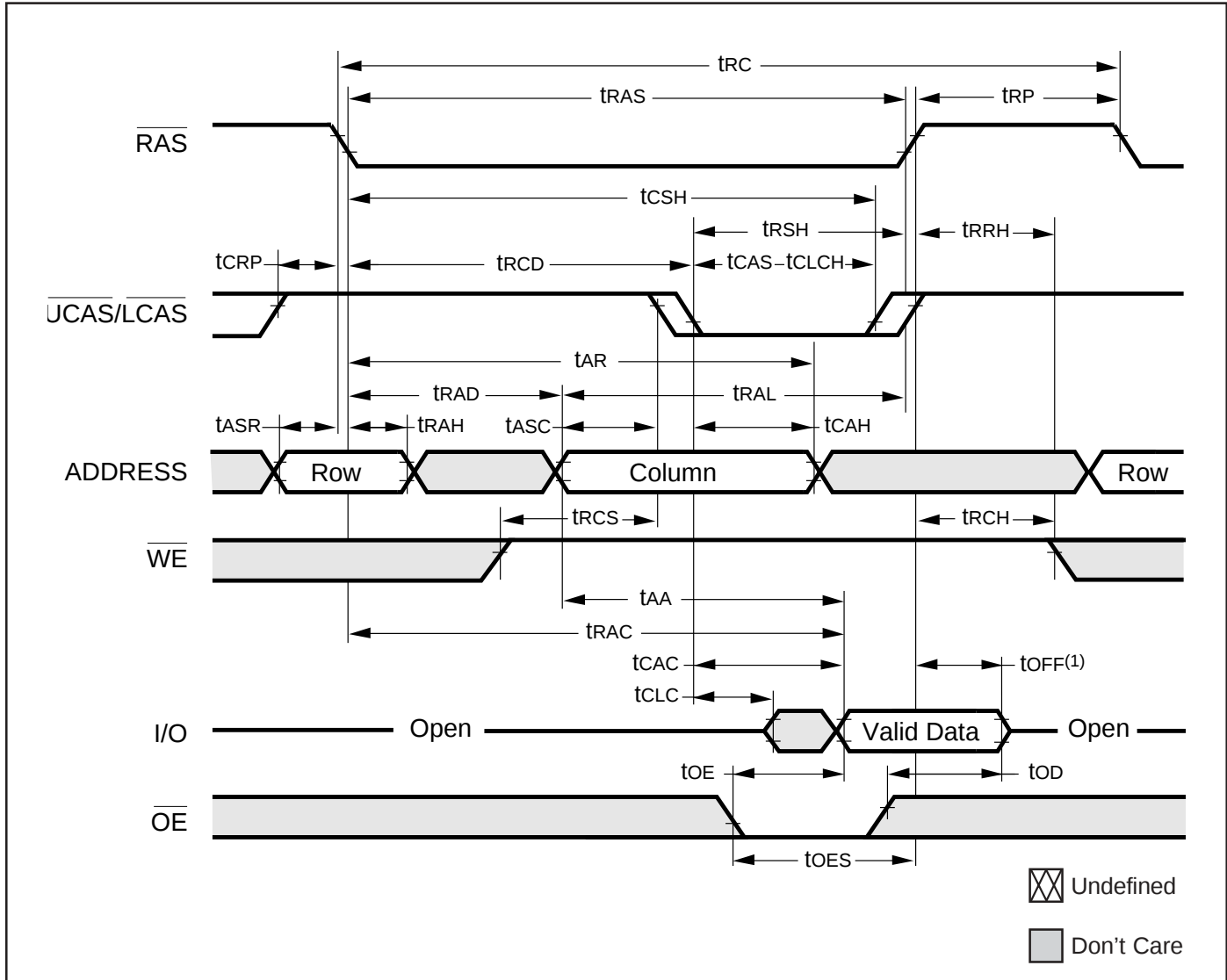
Input timing reference levels: $V_{IH} = 2.4V$, $V_{IL} = 0.8V$ ($V_{CC} = 5.0V \pm 10\%$);
 $V_{IH} = 2.0V$, $V_{IL} = 0.8V$ ($V_{CC} = 3.3V \pm 10\%$)

Output timing reference levels: $V_{OH} = 2.0V$, $V_{OL} = 0.8V$ ($V_{CC} = 5V \pm 10\%$, $3.3V \pm 10\%$)

Notes:

1. An initial pause of 200 μs is required after power-up followed by eight $\overline{RAS}$ refresh cycle ($\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If $\overline{CAS}$ and $\overline{RAS} = V_{IH}$, data output is High-Z.
5. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{RCD} = t_{RCD} (MAX)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{RCD} = t_{RCD} (MAX)$.
9. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed for t_{CP} .
10. Operation with the $t_{RCD} (MAX)$ limit ensures that $t_{RAC} (MAX)$ can be met. $t_{RCD} (MAX)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (MAX)$ limit, access time is controlled exclusively by t_{CAC} .
11. Operation within the $t_{RAD} (MAX)$ limit ensures that $t_{RCD} (MAX)$ can be met. $t_{RAD} (MAX)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} (MAX)$ limit, access time is controlled exclusively by t_{AA} .
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. $t_{OFF} (MAX)$ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} .
14. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} = t_{WCS} (MIN)$, the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{RWD} = t_{RWD} (MIN)$, $t_{AWD} = t_{AWD} (MIN)$ and $t_{CWD} = t_{CWD} (MIN)$, the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$ -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input, I/O0-I/O7 by $\overline{LCAS}$ and I/O8-I/O15 by $\overline{UCAS}$.
16. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, I/O goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{WE}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back to LOW after t_{OE} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. The first $\chi\overline{CAS}$ edge to transition LOW.
21. The last $\chi\overline{CAS}$ edge to transition HIGH.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling $\chi\overline{CAS}$ edge to first rising $\chi\overline{CAS}$ edge.
24. Last rising $\chi\overline{CAS}$ edge to next cycle's last rising $\chi\overline{CAS}$ edge.
25. Last rising $\chi\overline{CAS}$ edge to first falling $\chi\overline{CAS}$ edge.
26. Each $\chi\overline{CAS}$ must meet minimum pulse width.
27. Last $\chi\overline{CAS}$ to go LOW.
28. I/Os controlled, regardless $\overline{UCAS}$ and $\overline{LCAS}$.
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

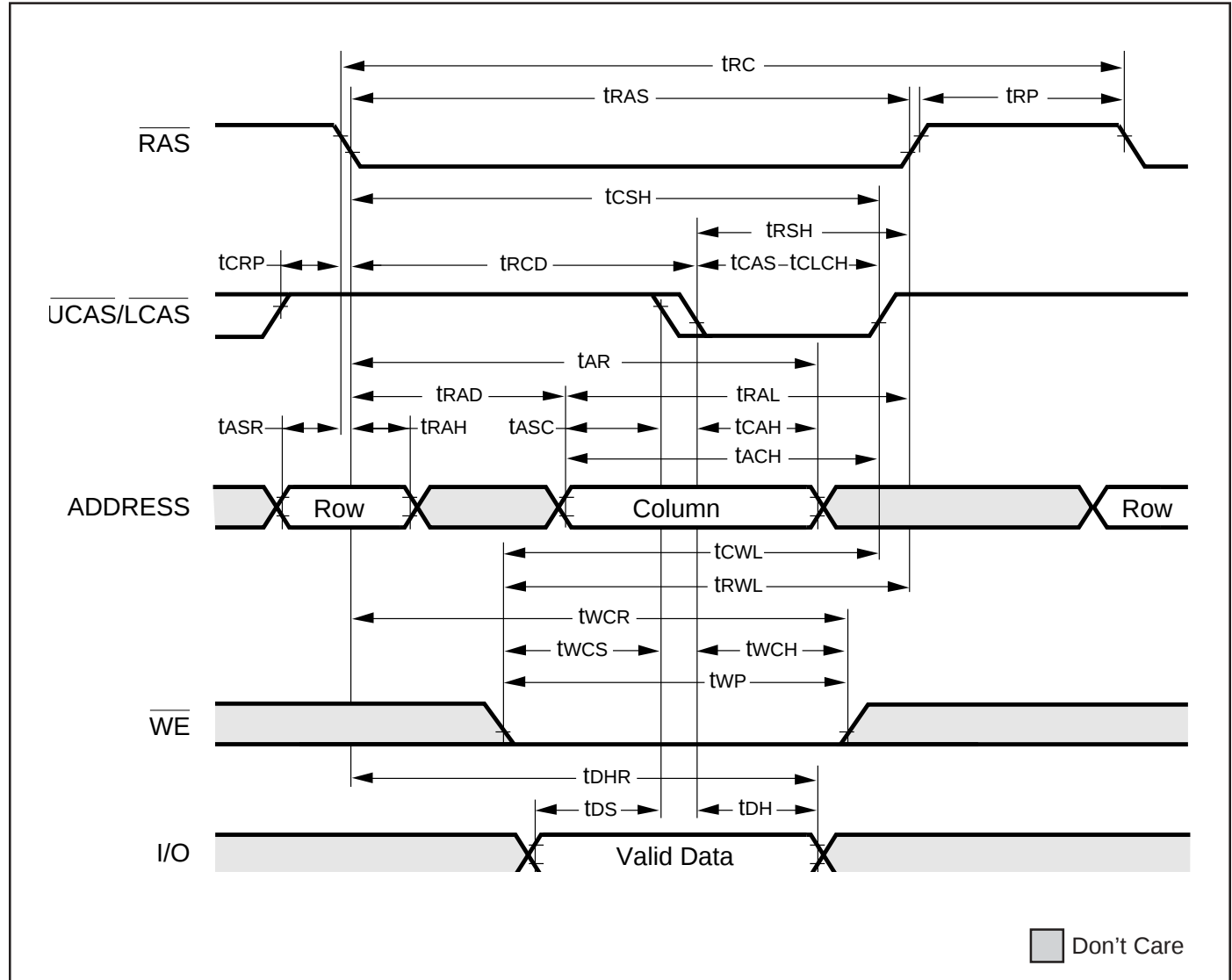
READ CYCLE



Note:

1. t_{OFF} is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



The diagram illustrates the timing relationships for a 2D array memory device. The signals and their associated timing parameters are as follows:

- RAS**: Row Address Strobe. Timing parameters include t_{RWC} (Row to Column delay), t_{RAS} (RAS pulse width), and t_{RP} (RAS return time).
- UCAS/LCAS**: Universal Chip Address Strobe/Latch Address Strobe. Timing parameters include t_{CRP} (UCAS/LCAS to RAS delay), t_{RCD} (RAS to UCAS/LCAS delay), t_{CSH} (UCAS/LCAS to Column delay), t_{RSH} (RAS to UCAS/LCAS delay), and $t_{CAS} - t_{CLCH}$ (UCAS/LCAS to Column delay).
- ADDRESS**: Memory address. It is divided into Row and Column phases. Timing parameters include t_{ASR} (Address Strobe to RAS delay), t_{RAH} (Row Address Hold), t_{ASC} (Address to Column delay), t_{CAH} (Column Address Hold), t_{ACH} (Address to Column delay), t_{RWD} (Row to Column delay), t_{RCS} (Row to Column delay), t_{CWD} (Column to Column delay), t_{AWD} (Address to Column delay), t_{CWL} (Row to Column delay), t_{RWL} (Column to Column delay), and t_{WP} (Write Pulse).
- WE**: Write Enable. Timing parameters include t_{TAA} (Write Enable to Address delay), t_{RAC} (Row Address to Column delay), t_{CAC} (Column Address to Column delay), and t_{CLZ} (Column Address to Column delay).
- I/O**: Data Input/Output. Timing parameters include t_{DS} (Data Setup), t_{DH} (Data Hold), t_{OE} (Output Enable to Data delay), t_{OD} (Output Disable to Data delay), and t_{OEH} (Output Enable Hold).
- OE**: Output Enable. Timing parameters include t_{OE} (Output Enable to Data delay), t_{OD} (Output Disable to Data delay), and t_{OEH} (Output Enable Hold).

Legend:

- Undefined (indicated by a box with an 'X')
- Don't Care (indicated by a shaded box)

The diagram illustrates the timing relationships between several control and data signals during DRAM operations:

- RAS**: Row Address Strobe. Timing parameters include t_{RASP} (pulse width), t_{TRP} (return time), t_{CSH} (setup before CAS), $t_{PC(1)}$ (period between CAS), t_{RSH} (hold after CAS), and t_{CP} (column access time).
- JCAS/LCAS**: Column Address Strobe / Local Column Address Strobe. Timing parameters include t_{CRP} (pulse width), t_{CD} (column delay), $t_{CAS, tCLCH}$ (access time), and t_{TAR} (turnaround time).
- ADDRESS**: Data address bus. It shows sequential accesses for Row, Column, Column, Column, and Row. Parameters include t_{ASR} , t_{ASC} , t_{CAH} , t_{TRAH} , t_{RAD} , t_{RAL} , t_{RRH} , and t_{RCH} .
- WE**: Write Enable. Timing parameters include t_{RCS} (write setup), t_{AAT} (write pulse width), t_{CAC} (write cycle time), t_{COH} (write hold), and t_{TOFF} (output disable time).
- I/O**: Data bus. Shows "Open" state and "Valid Data". Parameters include t_{OE} (output enable pulse width), t_{OES} (output setup), t_{OD} (output delay), t_{TOE} (output enable-to-output delay), and t_{TOEP} (output enable period).
- OE**: Output Enable. Timing parameter includes t_{OEP} (output enable pulse width).

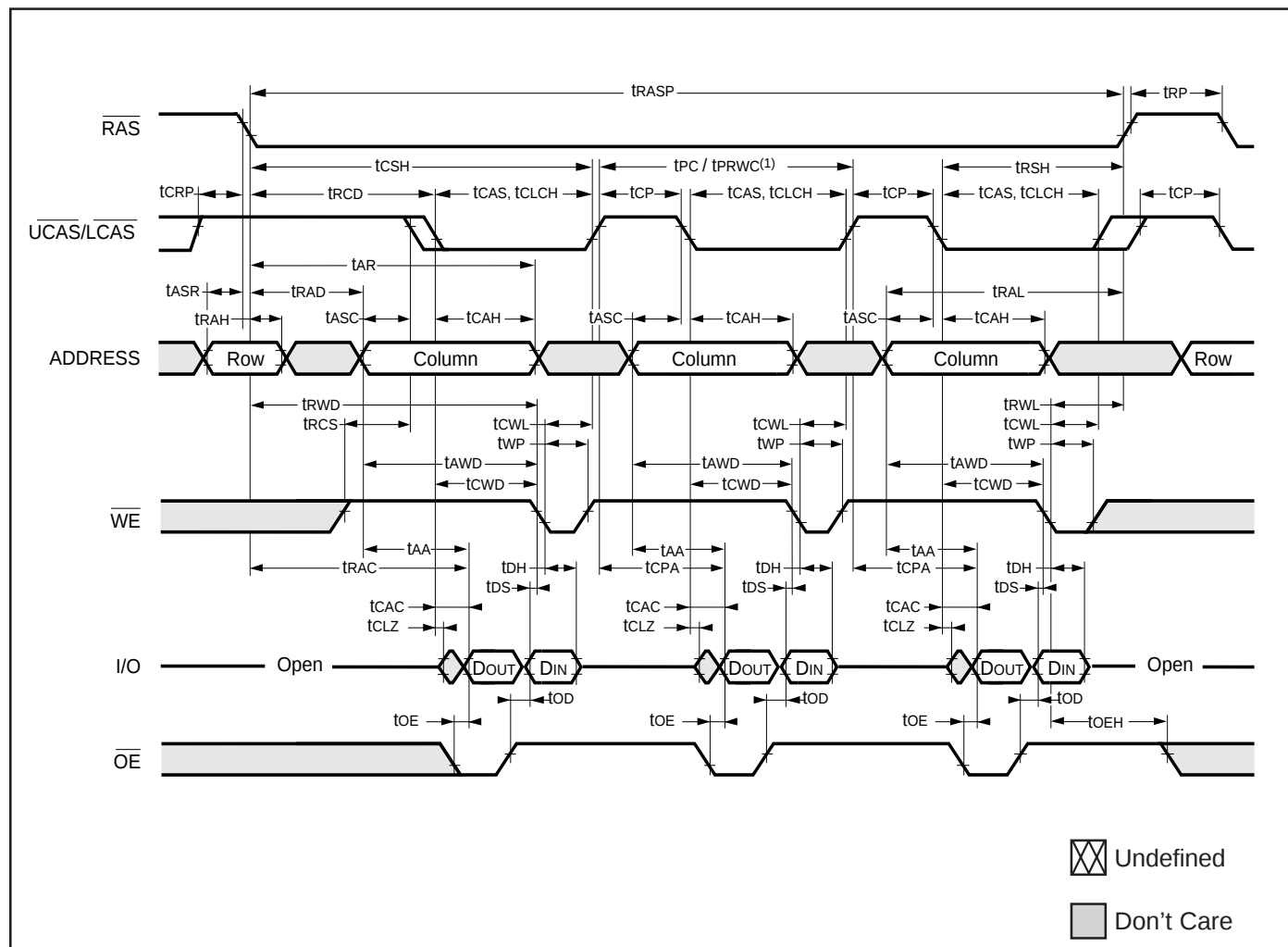
Legend:

- X: Undefined
- Gray box: Don't Care

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[illegible]

EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



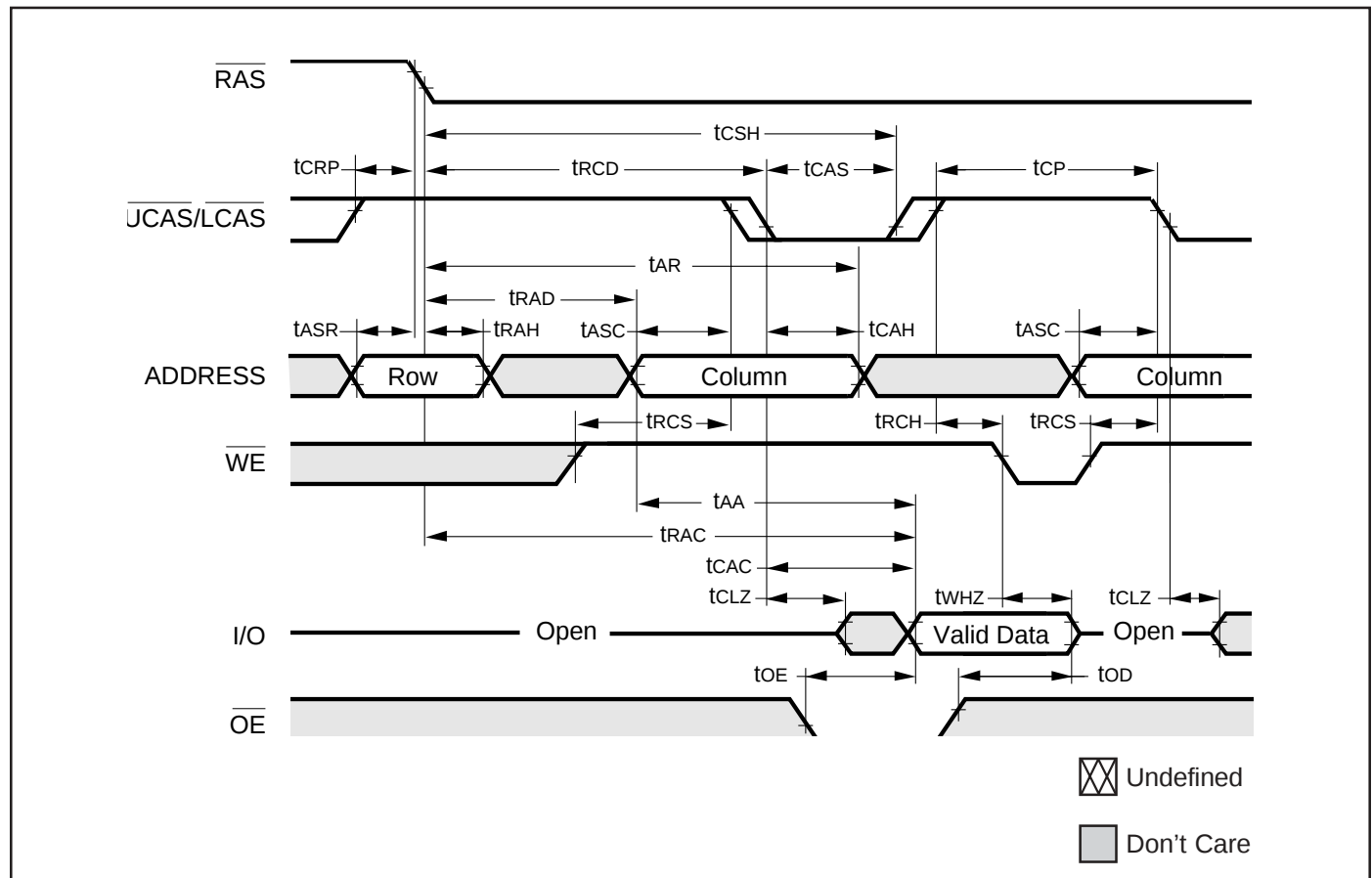
Note:

1. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specifications.

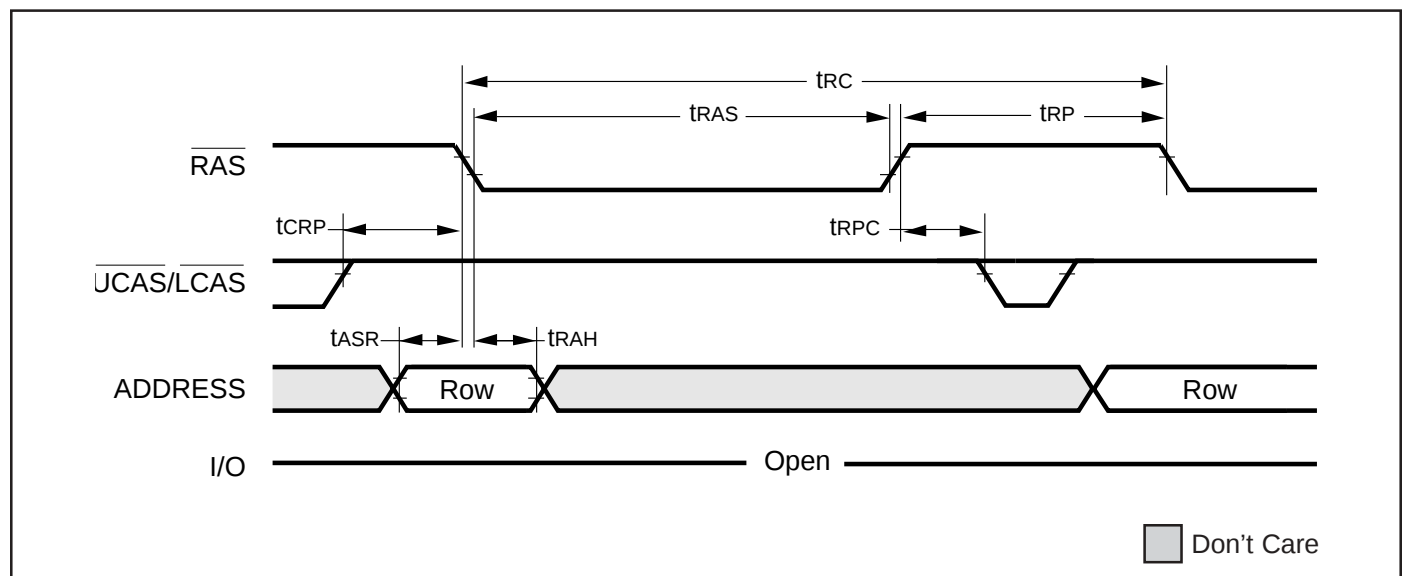
[illegible]

AC WAVEFORMS

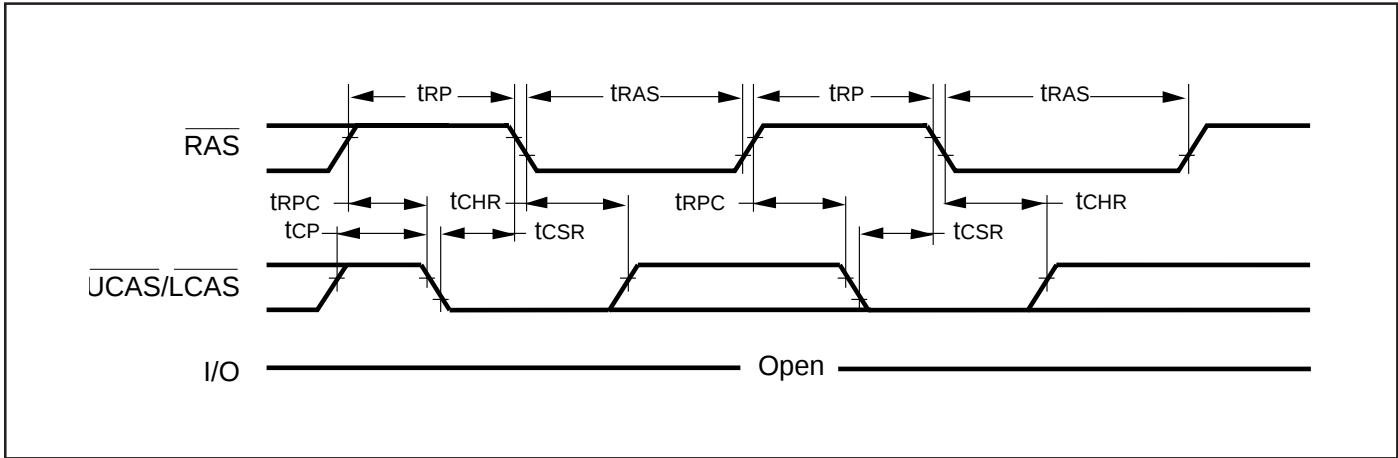
READ CYCLE (With $\overline{WE}$ -Controlled Disable)



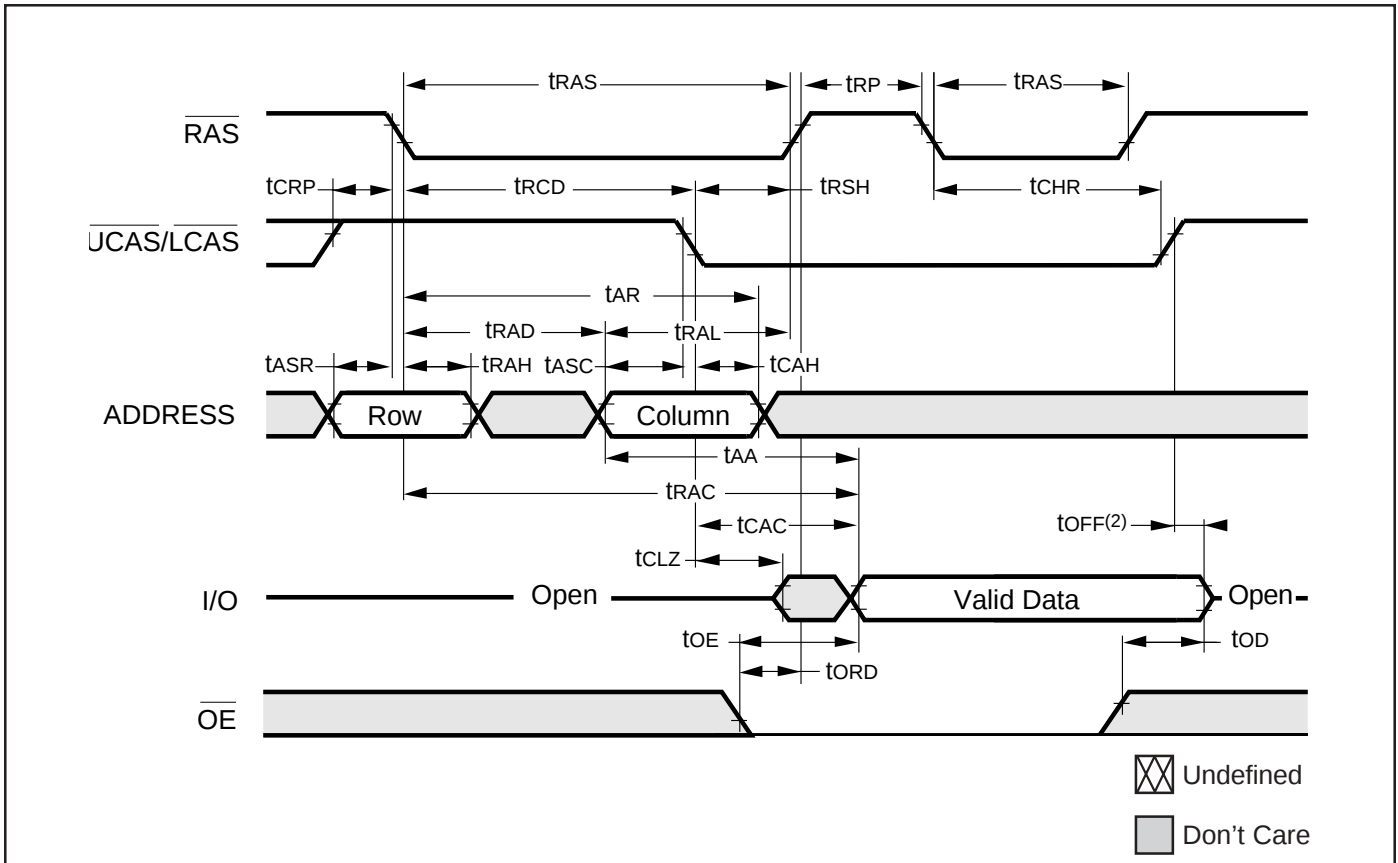
$\overline{RAS}$ -ONLY REFRESH CYCLE ($\overline{OE}$, $\overline{WE}$ = DON'T CARE)



$\overline{\text{CBR}}$ REFRESH CYCLE (Addresses; $\overline{\text{WE}}$, $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE⁽¹⁾ ($\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)



Notes:

1. A Hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
2. t_{OFF} is referenced from rising edge of RAS or CAS, whichever occurs last.

ORDERING INFORMATION : 5V

Commercial Range: 0°C to 70°C

Speed (ns)	Order Part No.	Package
50	IS41C16100-50K	400-mil SOJ
	IS41C16100-50T	400-mil TSOP (Type II)
60	IS41C16100-60K	400-mil SOJ
	IS41C16100-60T	400-mil TSOP (Type II)

Industrial Range: -40°C to 85°C

Speed (ns)	Order Part No.	Package
50	IS41C16100-50KI	400-mil SOJ
	IS41C16100-50TI	400-mil TSOP (Type II)
60	IS41C16100-60KI	400-mil SOJ
	IS41C16100-60TI	400-mil TSOP (Type II)

ORDERING INFORMATION : 3.3V

Commercial Range: 0°C to 70°C

Speed (ns)		Order Part No.	Package
50	IS41LV16100-50K	400-mil SOJ	
	IS41LV16100-50T	400-mil TSOP (Type II)	
	IS41LV16100-50TL	400-mil TSOP (Type II), Lead-free	
60	IS41LV16100-60K	400-mil SOJ	
	IS41LV16100-60T	400-mil TSOP (Type II)	
	IS41LV16100-60TL	400-mil TSOP (Type II), Lead-free	

Industrial Range: -40°C to 85°C

Speed (ns)		Order Part No.	Package
50	IS41LV16100-50KI	400-mil SOJ	
	IS41LV16100-50TI	400-mil TSOP (Type II)	
	IS41LV16100-50TLI	400-mil TSOP (Type II), Lead-free	
60	IS41LV16100-60KI	400-mil SOJ	
	IS41LV16100-60TI	400-mil TSOP (Type II)	
	IS41LV16100-60TLI	400-mil TSOP (Type II), Lead-free	