4-Line BUS-Port ESD-Protection

Features

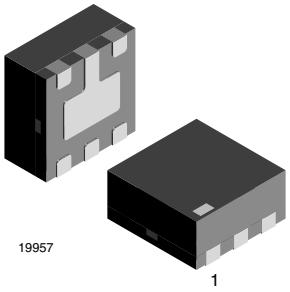
- Ultra compact LLP75-6A package
- 4-line USB ESD-protection
- Low leakage current
- Low load capacitance C_D = 1.2 pF
- ESD-protection acc. IEC 61000-4-2
  - ± 30 kV contact discharge
  - ± 30 kV air discharge
- High surge current acc. IEC61000-4-5 I_{PP} > 11 A
- Lead (Pb)-free component
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC

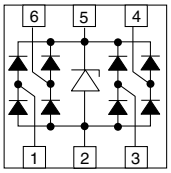
Pb-free

e3

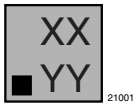
RoHS COMPLIANT

GREEN (5-2008)*





Marking (example only)



Dot = Pin 1 marking
XX = Date code
YY = Type code (see table below)

Ordering Information

Device name	Ordering code	Taped units per reel (8 mm tape on 7" reel)	Minimum order quantity
VBUS054CV-HS3	VBUS054CV-HS3-GS08	3000	15000

Package Data

Device name	Package name	Marking code	Weight	Molding compound flammability rating	Moisture sensitivity level	Soldering conditions
VBUS054CV-HS3	LLP75-6A	U8	5.1 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

Absolute Maximum Ratings

Parameter	Test conditions	Symbol	Value	Unit
Peak pulse current	Pin 1, 3, 4 or 6 to pin 2 acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	I_{PPM}	11	A
	Pin 5 to pin 2 acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	I_{PPM}	13	A
Peak pulse power	Pin 1, 3, 4 or 6 to pin 2 acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	P_{PP}	242	W
	Pin 5 to pin 2 acc. IEC 61000-4-5; t_P = 8/20 µs; single shot	P_{PP}	246	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 30	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 30	kV
Operating temperature	Junction temperature	T_J	- 40 to + 125	°C
Storage temperature		T_{STG}	- 40 to + 150	°C

* Please see document “Vishay Green and Halogen-Free Definitions (5-2008)” http://www.vishay.com/doc?99902

Electrical Characteristics

Ratings at 25 °C, ambient temperature unless otherwise specified

VBUS054CV-HS3

Date line: pin 1 , 3, 4 or 6 to pin 2

Parameter	Test conditions/remarks	Symbol	Min.	Typ.	Max.	Unit
Protection paths	Number of line which can be protected	N_{lines}			4	lines
Reverse working voltage	at I_R = 0.1 µA	V_{RWM}	5			V
Reverse current	at $V_{IN} = V_{RWM}$ = 5 V	I_R		< 0.01	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	7	7.9	8.6	V
Reverse clamping voltage	at I_{PP} = 11 A; acc. IEC 61000-4-5	V_C		18	22	V
Forward clamping voltage	at I_F = 11 A; acc. IEC 61000-4-5	V_F		6.5	8	V
Data line capacitance	V_R (at I/O pin) = 0 V; V_R (at pin 5) = 5 V; f = 1 MHz	C_D		1.2	2.5	pF
Line Symmetry	Difference of the line capacitances	dC_D			0.2	pF

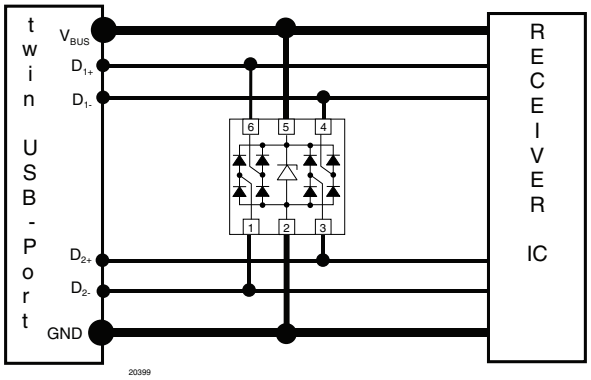
VBUS054CV-HS3

V_{BUS}-line: pin 5 to pin 2

Parameter	Test conditions/remarks	Symbol	Min.	Typ.	Max.	Unit
Reverse working voltage	at I_R = 0.1 µA	V_{RWM}	5	6.6		V
Reverse current	at $V_{IN} = V_{RWM}$ = 5 V	I_R		< 0.01	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	7	7.9	8.6	V
Reverse clamping voltage	at I_{PP} = 13 A; acc. IEC 61000-4-5	V_C		18	22	V
Forward clamping voltage	at I_F = 13 A; acc. IEC 61000-4-5	V_F			7	V
Line capacitance	V_R (at pin 5) = 0 V; f = 1 MHz	C_D		190		pF

Application Note

With the VBUS054CV-HS3 a double, high speed USB-port can be protected against transient voltage signals. Negative transients will be clamped close below the ground level while positive transients will be clamped close above the 5 V working range. An avalanche diode clamps the supply line (V_{BUS} at pin 5) to ground (pin 2). The high speed data lines, D1+, D2+, D1- and D2- , are connected to pin 1, 3, 4 and 6. As long as the signal voltage on the data lines is between the ground- and the V_{BUS} -level, the low capacitance PN-diodes offer a very high isolation to V_{BUS} , ground and to the other data lines. But as soon as any transient signal exceeds this working range, one of the PN-diodes gets in the forward mode and clamps the transient to ground or the avalanche break through voltage level.



Typical Characteristics

T_{amb} = 25 °C, unless otherwise specified

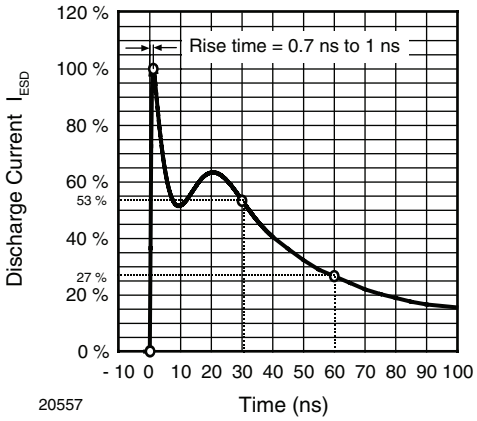


Figure 1. ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω/150 pF)

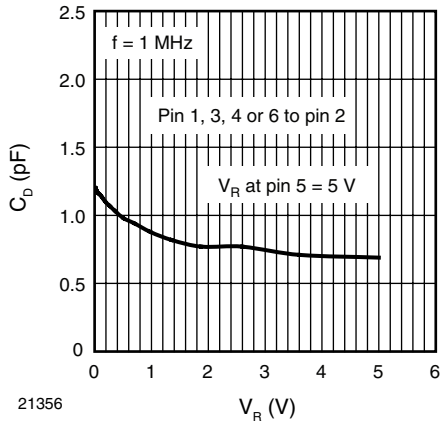


Figure 3. Typical Capacitance C_D vs. Reverse Voltage V_R

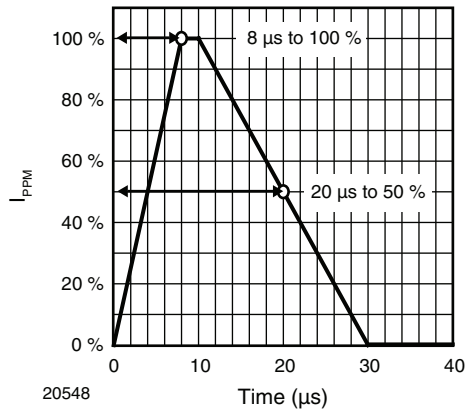


Figure 2. 8/20 µs Peak Pulse Current Wave Form
acc. IEC 61000-4-5

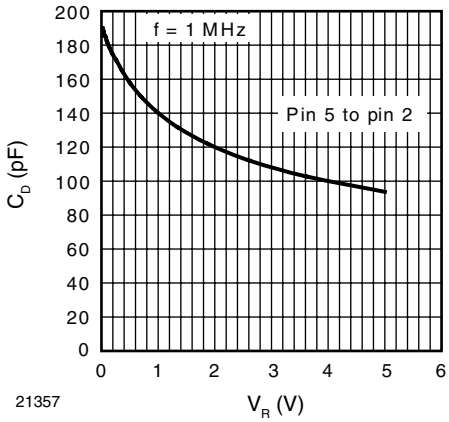


Figure 4. Typical Capacitance C_D vs. Reverse Voltage V_R

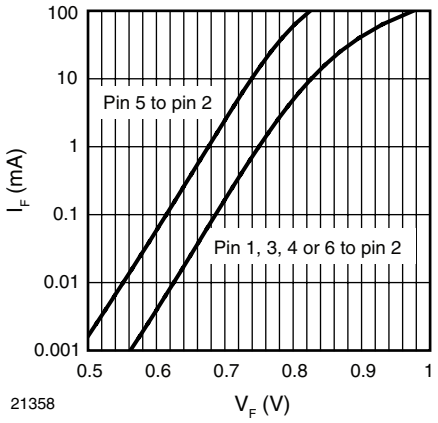


Figure 5. Typical Forward Current I_F vs. Forward Voltage V_F

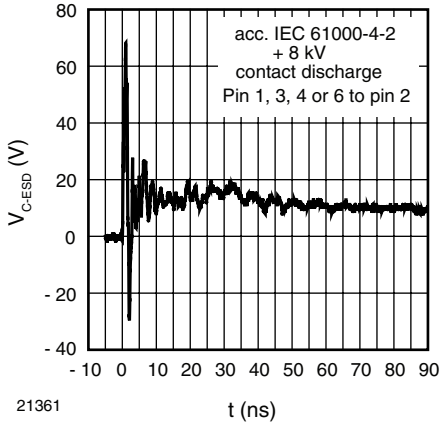


Figure 8. Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

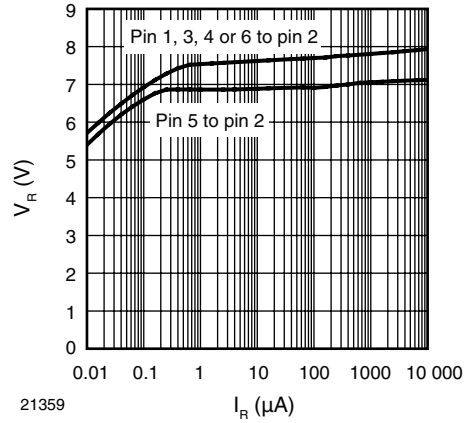


Figure 6. Typical Reverse Voltage V_R vs. Reverse Current I_R

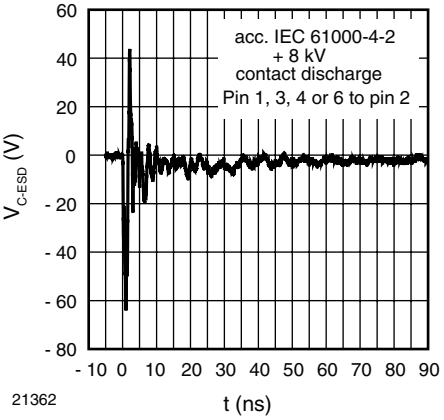


Figure 9. Typical Clamping performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

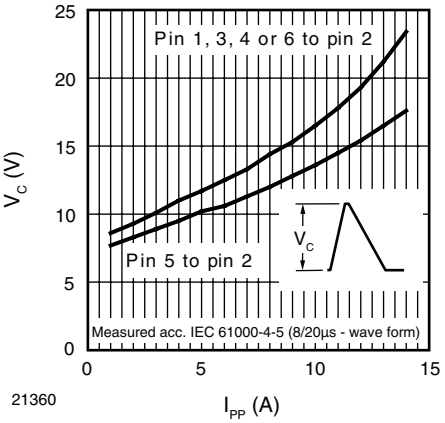


Figure 7. Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

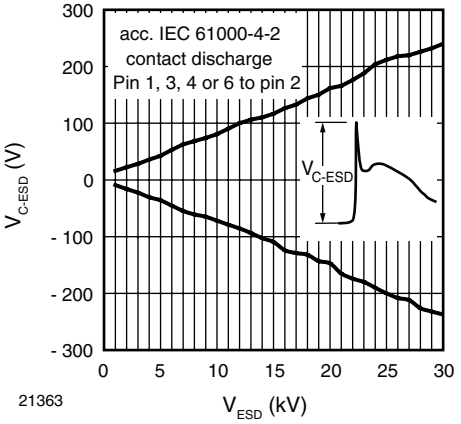
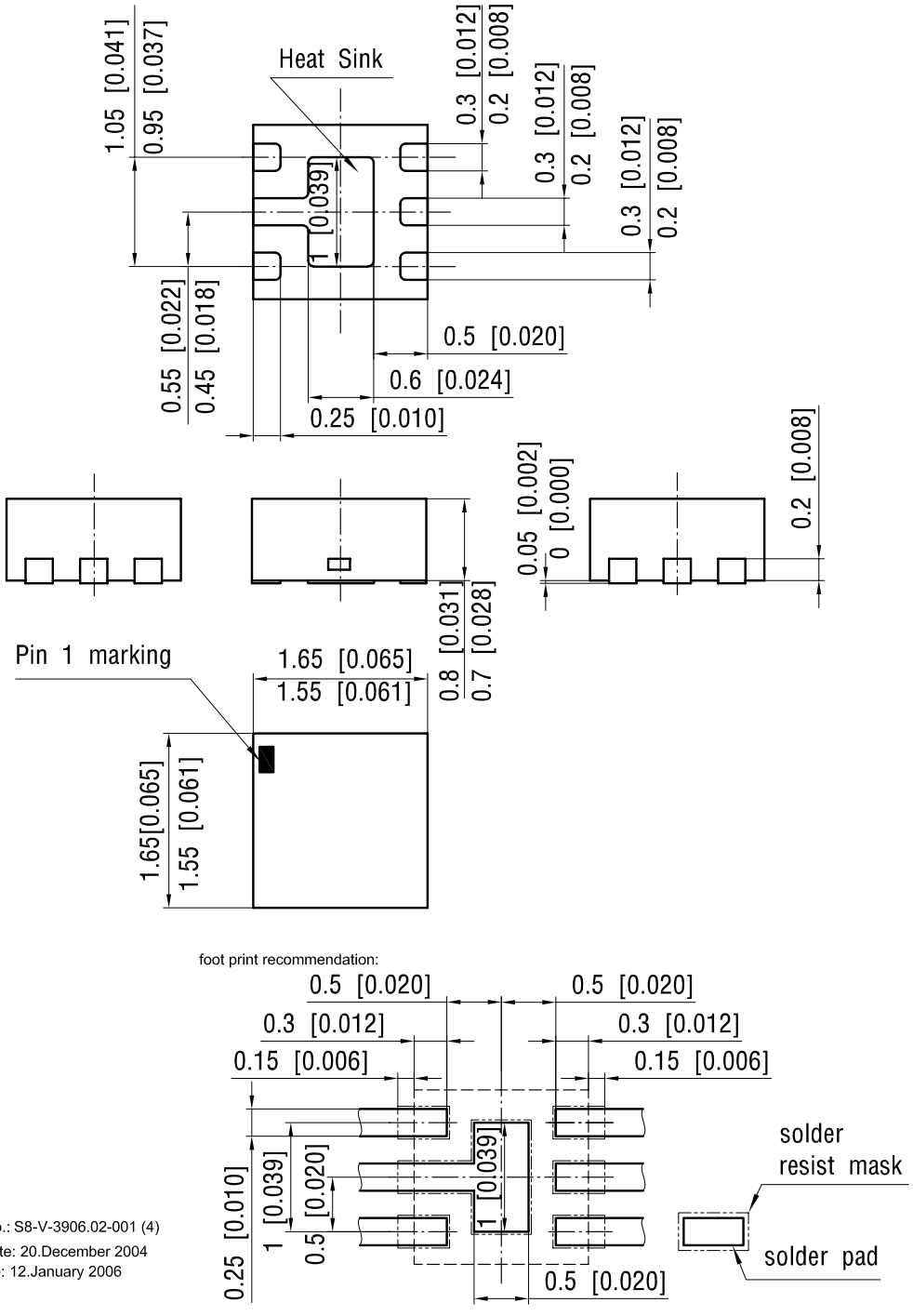


Figure 10. Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

Package Dimensions in millimeters (inches): **LLP75-6A**



foot print recommendation:

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Created - Date: 20.December 2004
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18058

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