



STD3NC60 STD3NC60-1

N-CHANNEL 600V - 1.8Ω - 3.2A DPAK / IPAK
PowerMesh™II MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD3NC60	600V	< 2.2Ω	3.2A
STD3NC60-1	600V	< 2.2Ω	3.2A

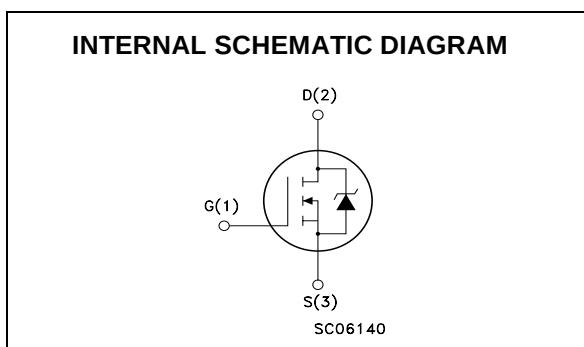
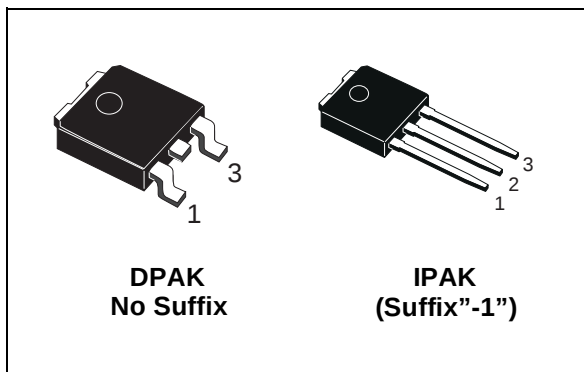
- TYPICAL R_{DS(on)} = 1.8Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL (SMD PACKAGE)

DESCRIPTION

The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600	V
V _{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	3.2	A
I _D	Drain Current (continuous) at T _C = 100°C	2	A
I _{DM} (•)	Drain Current (pulsed)	12.8	A
P _{TOT}	Total Dissipation at T _C = 25°C	50	W
	Derating Factor	0.4	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤ 3.2A, di/dt ≤ 300A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

STD3NC60 - STD3NC60-1

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	2.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	275	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	3.2	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	270	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 1.5 A		1.8	2.2	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 2A		3.7		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		475		pF
C _{oss}	Output Capacitance			72		pF
C _{rss}	Reverse Transfer Capacitance			10		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300V$, $I_D = 2A$		14		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 3)		14		ns
Q_g	Total Gate Charge	$V_{DD} = 480V$, $I_D = 4A$, $V_{GS} = 10V$		16.5	23.1	nC
Q_{gs}	Gate-Source Charge			2.5		nC
Q_{gd}	Gate-Drain Charge			9		nC

SWITCHING OFF

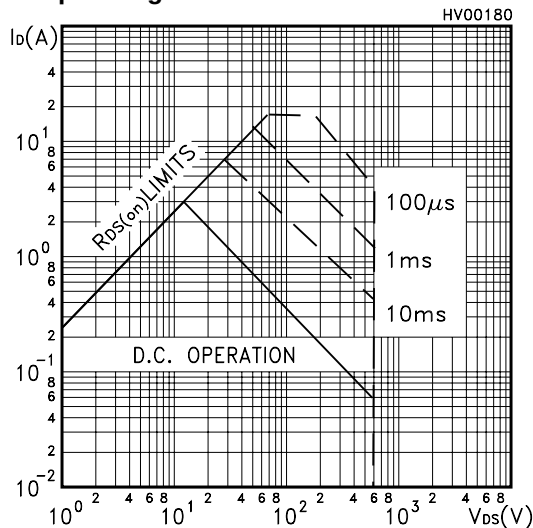
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 480V$, $I_D = 4A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$		15		ns
t_f	Fall Time	(see test circuit, Figure 5)		19		ns
t_c	Cross-over Time			24		ns

SOURCE DRAIN DIODE

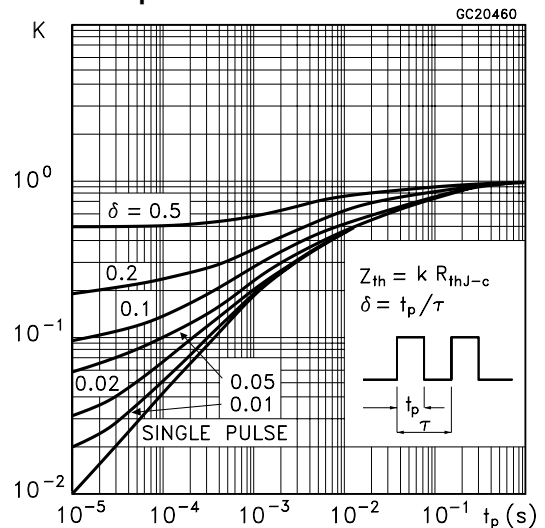
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3.2	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				12.8	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 3.2A$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4A$, $di/dt = 100A/\mu s$, $V_{DD} = 100V$, $T_j = 150^\circ C$		600		ns
Q_{rr}	Reverse Recovery Charge	(see test circuit, Figure 5)		2.7		μC
I_{RRM}	Reverse Recovery Current			9		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

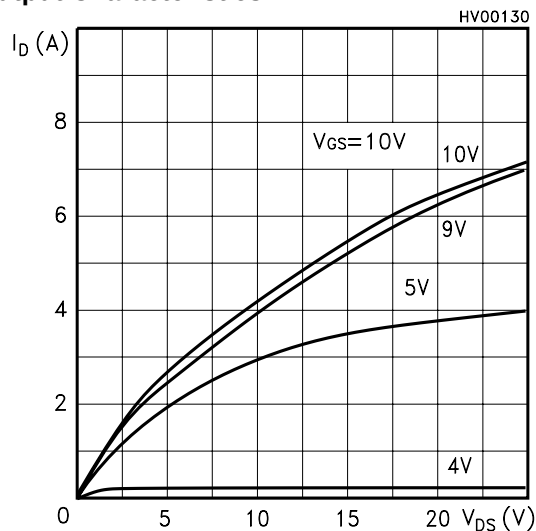
Safe Operating Area



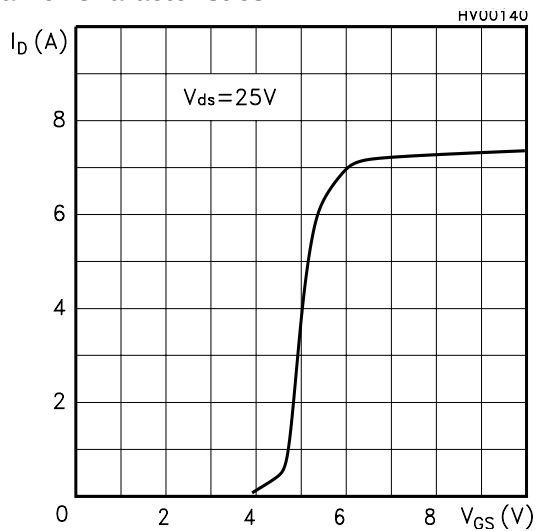
Thermal Impedance



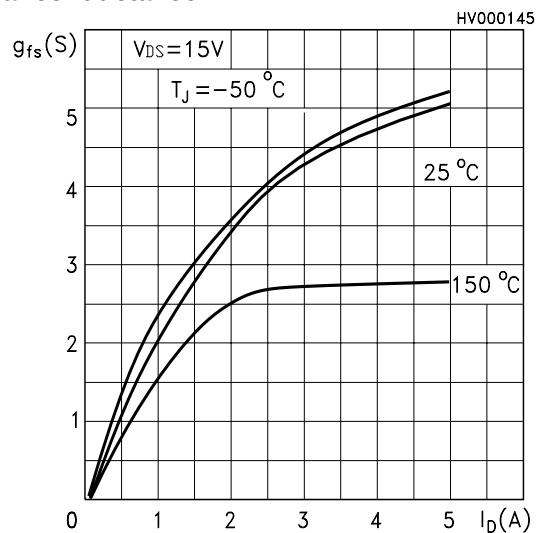
Output Characteristics



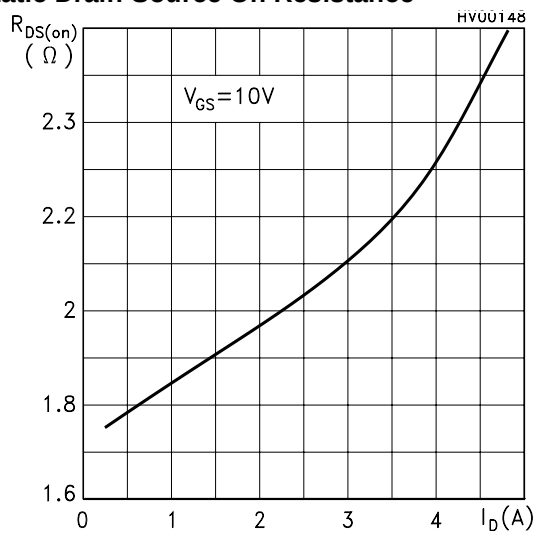
Transfer Characteristics



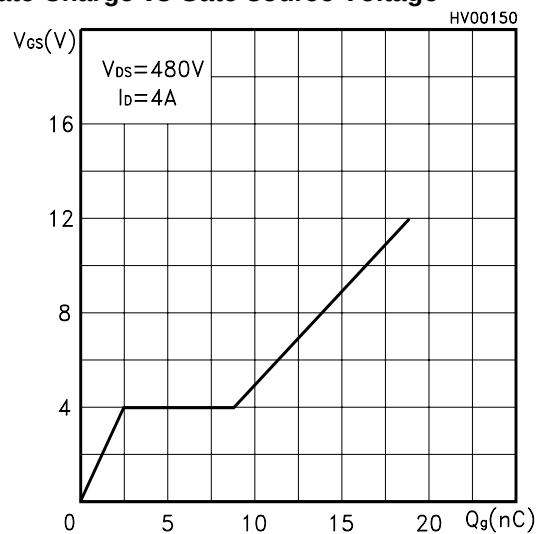
Transconductance



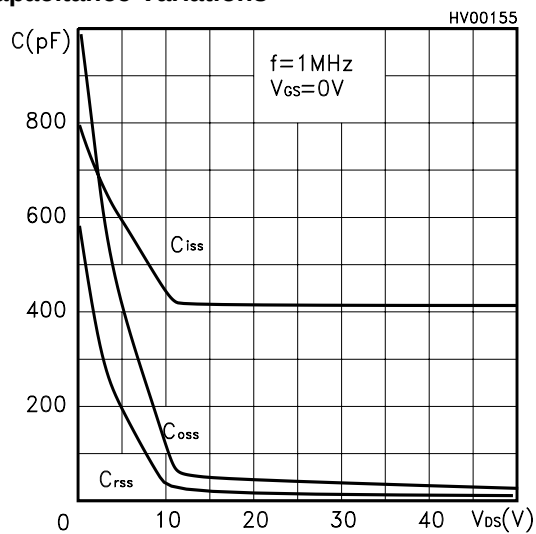
Static Drain-Source On Resistance



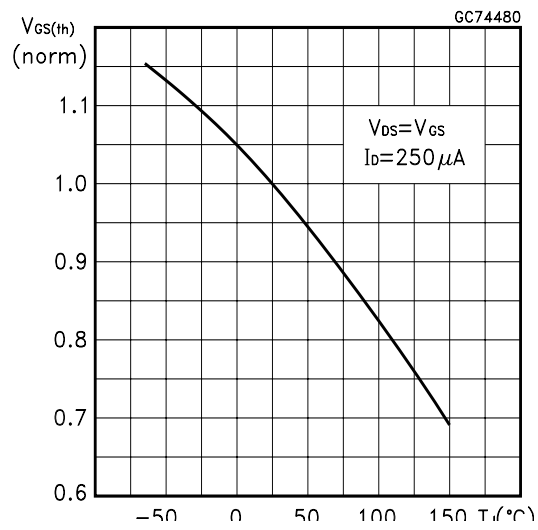
Gate Charge vs Gate-source Voltage



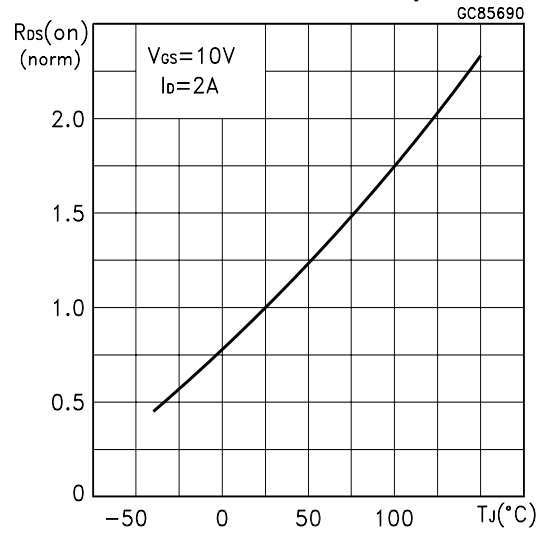
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

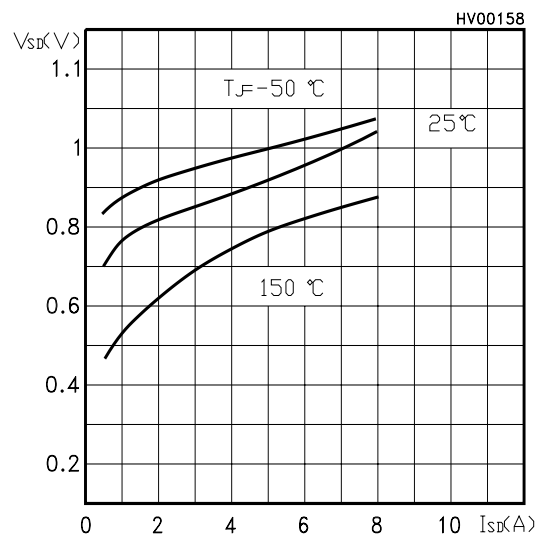


Fig. 1: Unclamped Inductive Load Test Circuit

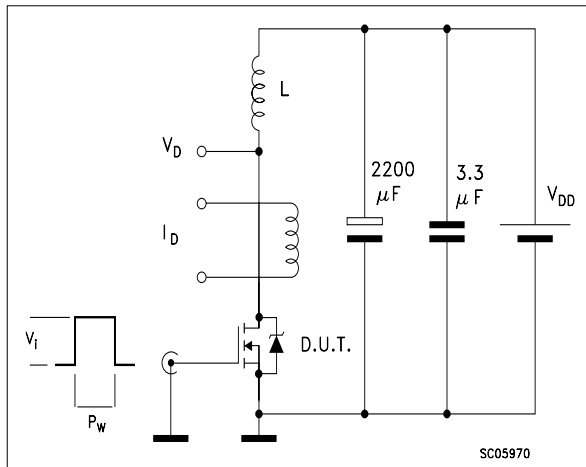


Fig. 2: Unclamped Inductive Waveform

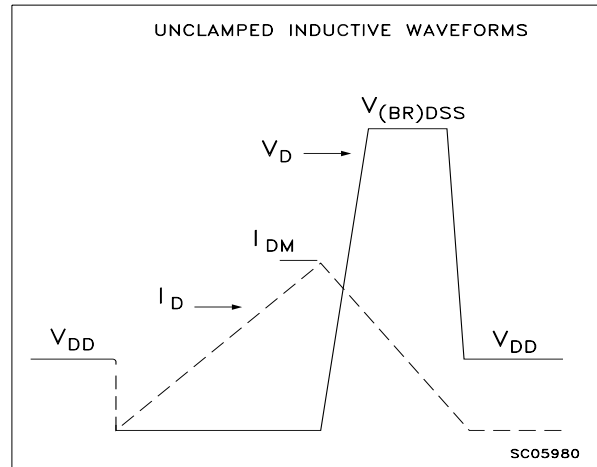


Fig. 3: Switching Times Test Circuits For Resistive Load

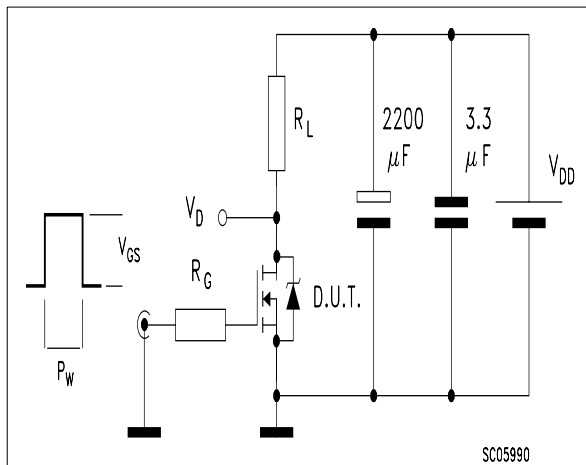


Fig. 4: Gate Charge test Circuit

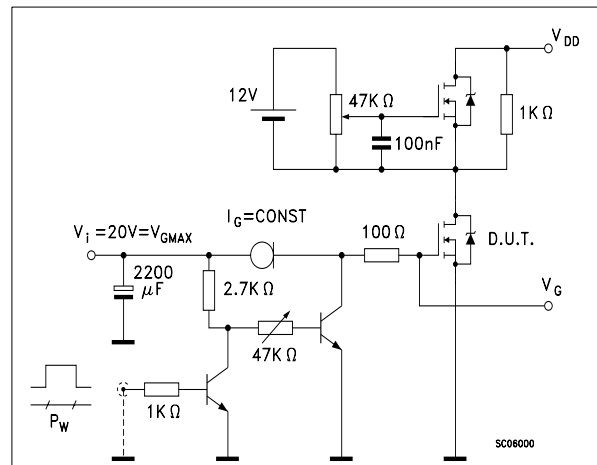
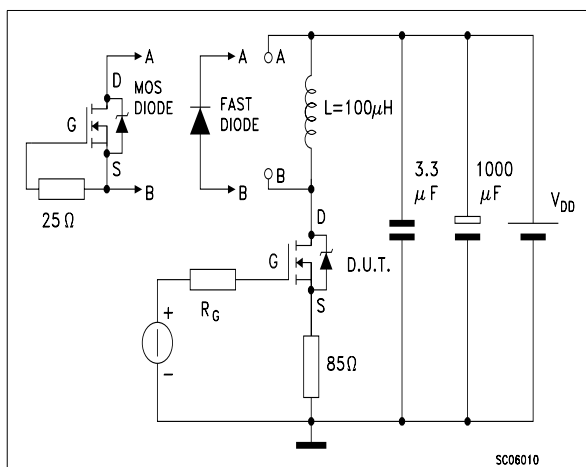
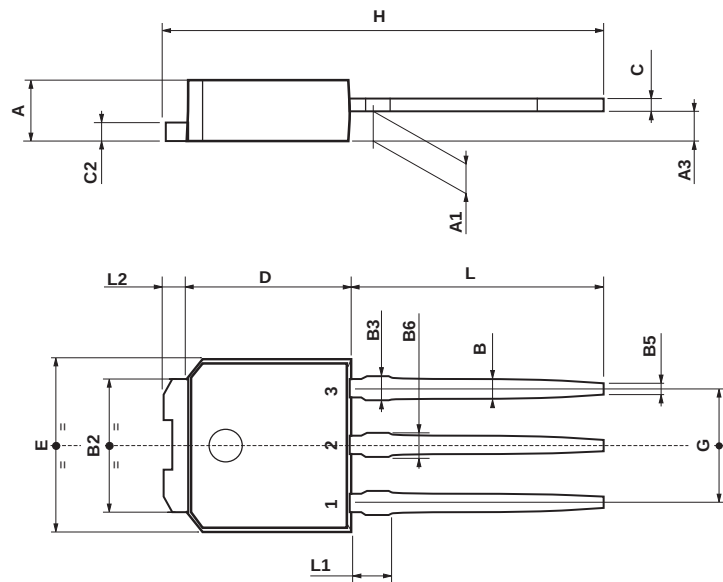


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-251 (IPAK) MECHANICAL DATA

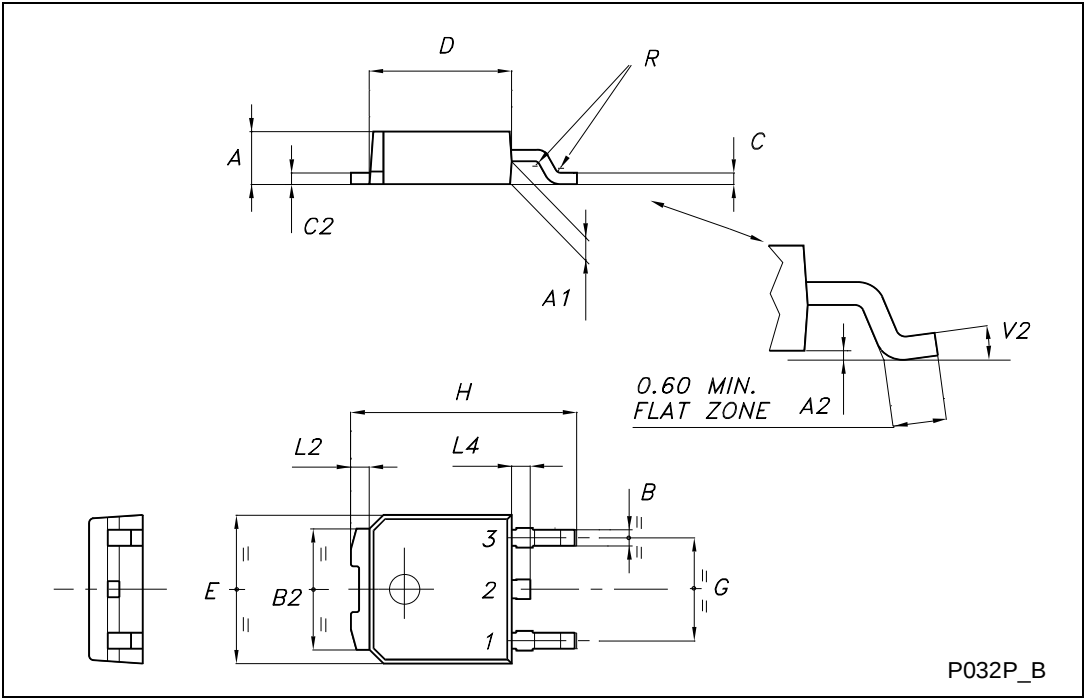
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



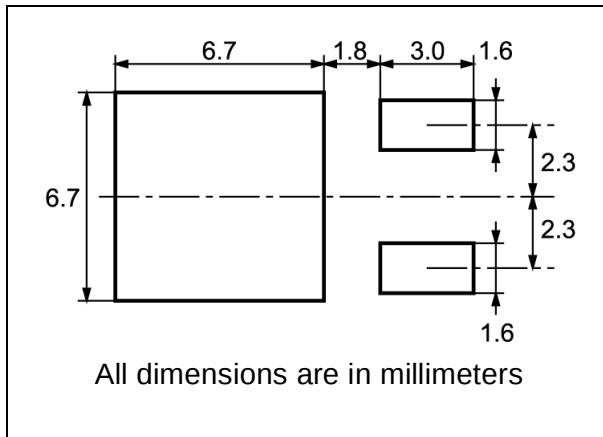
0068771-E

TO-252 (DPAK) MECHANICAL DATA

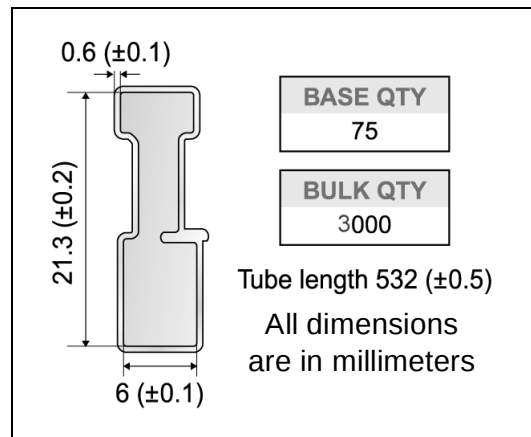
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



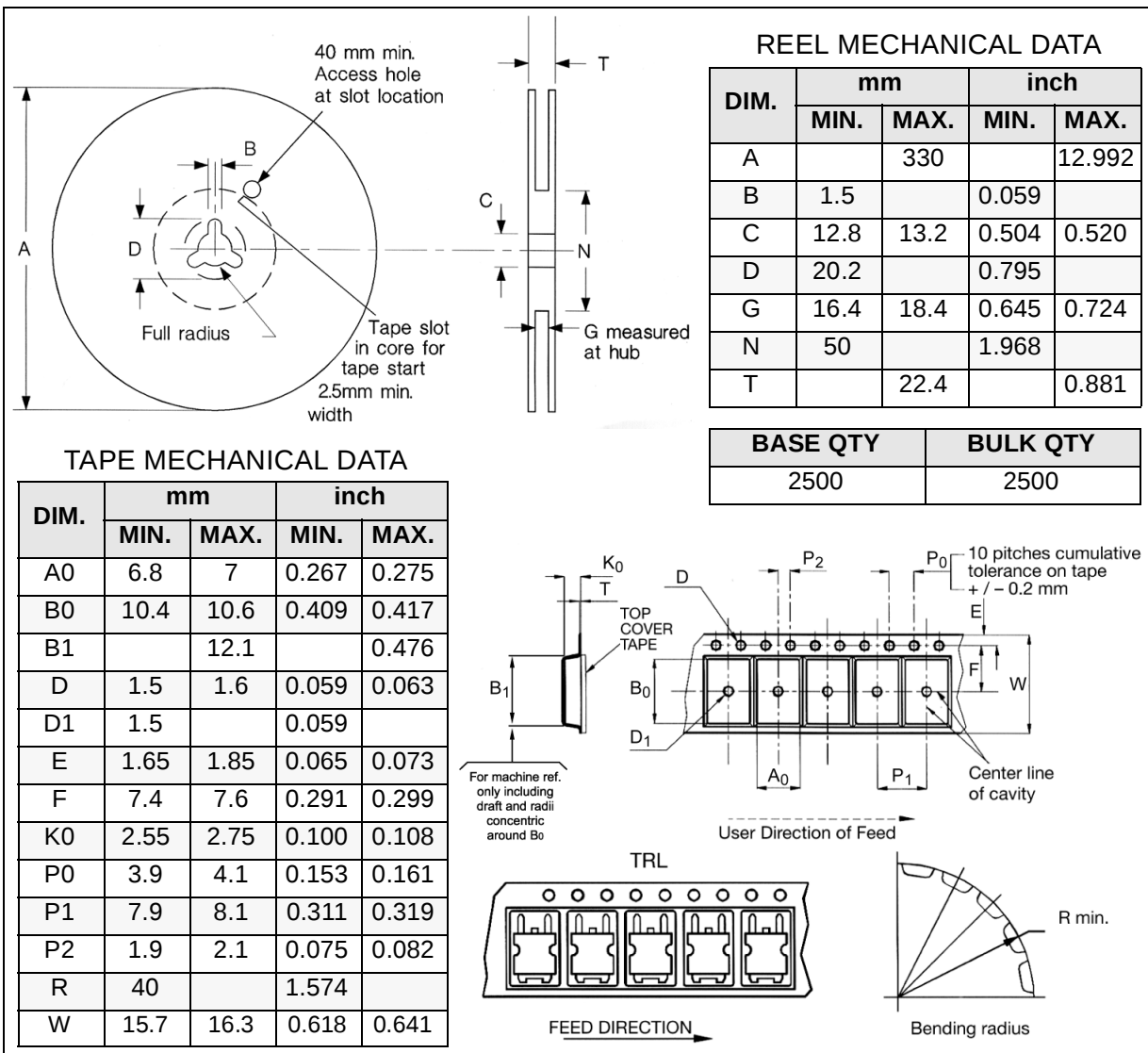
DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



* on sales type



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>