

- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

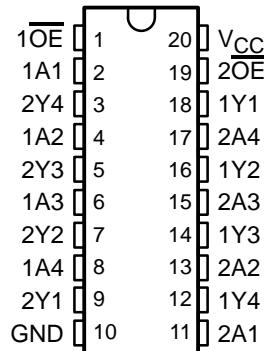
### description/ordering information

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

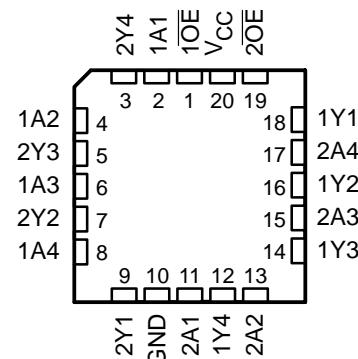
The 'AHCT240 devices are organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHCT240 . . . J OR W PACKAGE  
SN74AHCT240 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT240 . . . FK PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AHCT240N	SN74AHCT240N
	SOIC – DW	Tube	SN74AHCT240DW	AHCT240
		Tape and reel	SN74AHCT240DWR	
	SOP – NS	Tape and reel	SN74AHCT240NSR	AHCT240
	SSOP – DB	Tape and reel	SN74AHCT240DBR	HB240
	TSSOP – PW	Tube	SN74AHCT240PW	HB240
		Tape and reel	SN74AHCT240PWR	
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCT240DGVR	HB240
	CDIP – J	Tube	SNJ54AHCT240J	SNJ54AHCT240J
	CFP – W	Tube	SNJ54AHCT240W	SNJ54AHCT240W
	LCCC – FK	Tube	SNJ54AHCT240FK	SNJ54AHCT240FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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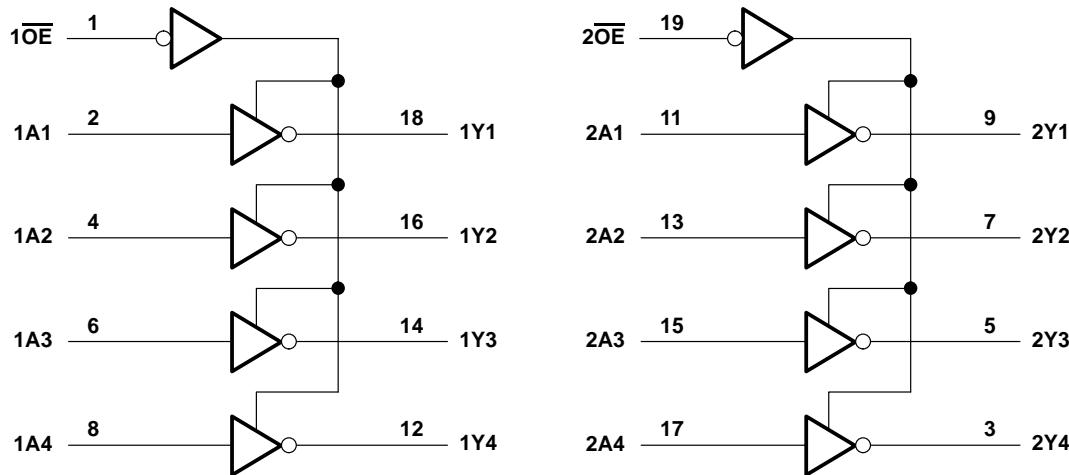
# SN54AHCT240, SN74AHCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS252K – OCTOBER 1995 – REVISED JULY 2003

## FUNCTION TABLE (each 4-bit buffer/driver)

INPUTS		OUTPUT
<u>OE</u>	A	Y
L	H	L
L	L	H
H	X	Z

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package .....	70°C/W
DGV package .....	92°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
PW package .....	83°C/W
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		SN54AHCT240		SN74AHCT240		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8		-8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT240	SN74AHCT240	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	4.5 V	4.4	4.5		4.4	4.4	V
	I <sub>OH</sub> = -8 mA		3.94			3.8	3.8	
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V		0.1		0.1	0.1	V
	I <sub>OL</sub> = 8 mA			0.36		0.44	0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±0.25		±2.5	±2.5	µA
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±0.1		±1*	±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4		40	40	µA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V		1.35		1.5	1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	2.5	10			10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	3					pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

**SN54AHCT240, SN74AHCT240  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

SCLS252K – OCTOBER 1995 – REVISED JULY 2003

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT240	SN74AHCT240	UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	5.4*	7.4*	1*	8.5*	1	8.5
$t_{PHL}$				5.4*	7.4*	1*	8.5*	1	8.5
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	7.7*	10.4*	1*	12*	1	12
$t_{PZL}$				7.7*	10.4*	1*	12*	1	12
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	8.3*	10.4*	1*	12*	1	12
$t_{PLZ}$				8.3*	10.4*	1*	12*	1	12
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	5.9	8.4	1	9.5	1	9.5
$t_{PHL}$				5.9	8.4	1	9.5	1	9.5
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	8.2	11.4	1	13	1	13
$t_{PZL}$				8.2	11.4	1	13	1	13
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	8.8	11.4	1	13	1	13
$t_{PLZ}$				8.8	11.4	1	13	1	13
$t_{sk(o)}$			$C_L = 50 \text{ pF}$	1**				1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

**noise characteristics,  $V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)**

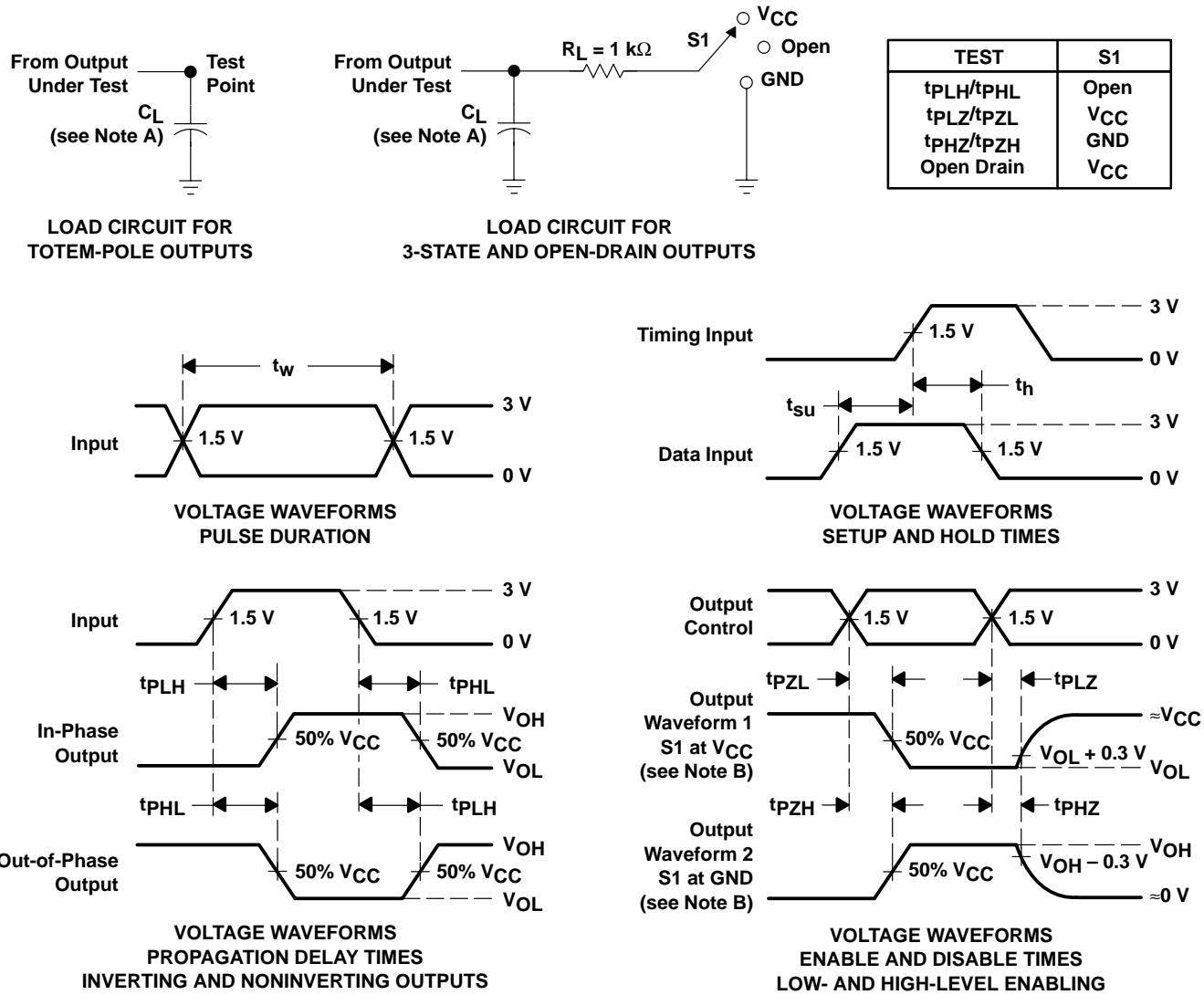
PARAMETER	SN74AHCT240			UNIT
	MIN	TYP	MAX	
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$			4.1	V
$V_{IH(D)}$ High-level dynamic input voltage		2		V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

**operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	10	pF

PARAMETER MEASUREMENT INFORMATION



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9680601Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9680601QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9680601QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN74AHCT240DBLE	OBsolete	SSOP	DB	20		TBD	Call TI	Call TI
SN74AHCT240DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74AHCT240DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/Level-1-235C-UNLIM
SN74AHCT240DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/Level-1-235C-UNLIM
SN74AHCT240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AHCT240NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74AHCT240PW	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHCT240PWLE	OBsolete	TSSOP	PW	20		TBD	Call TI	Call TI
SN74AHCT240PWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SNJ54AHCT240FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AHCT240J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AHCT240W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

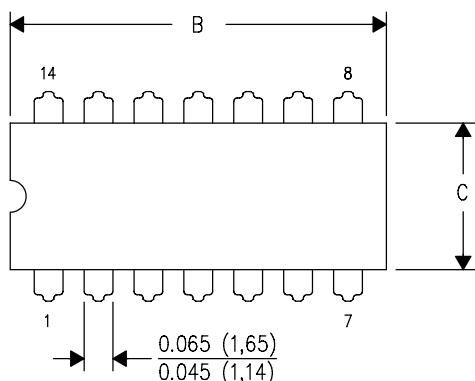
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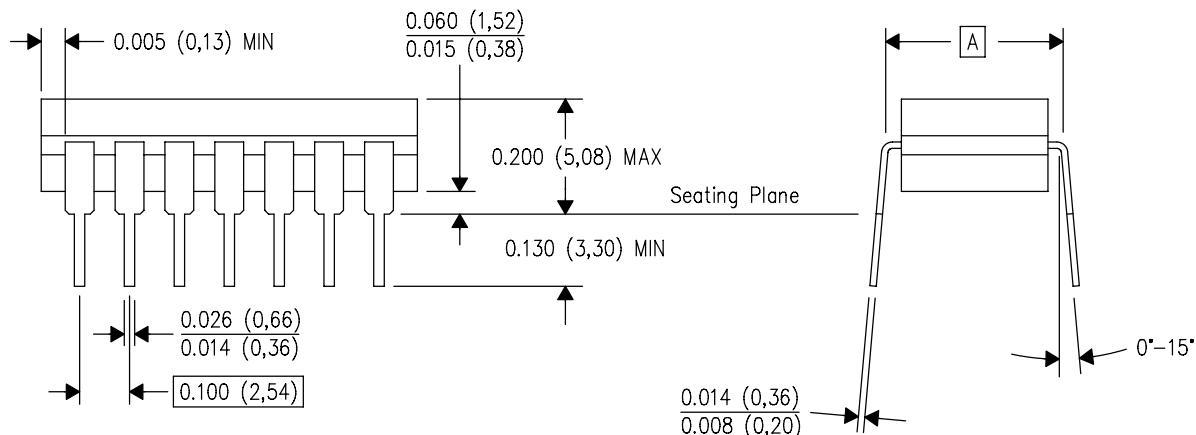
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

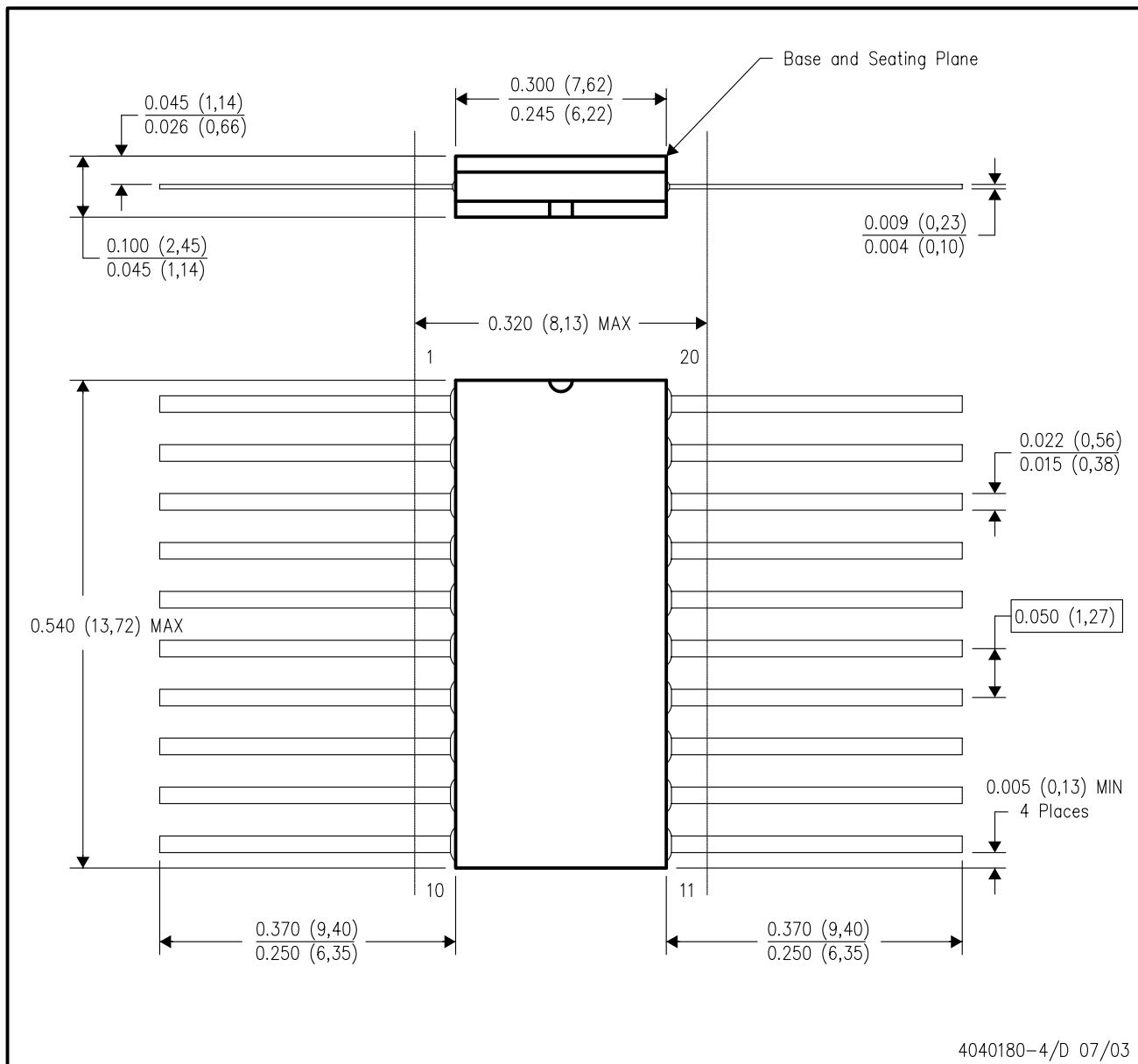


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NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



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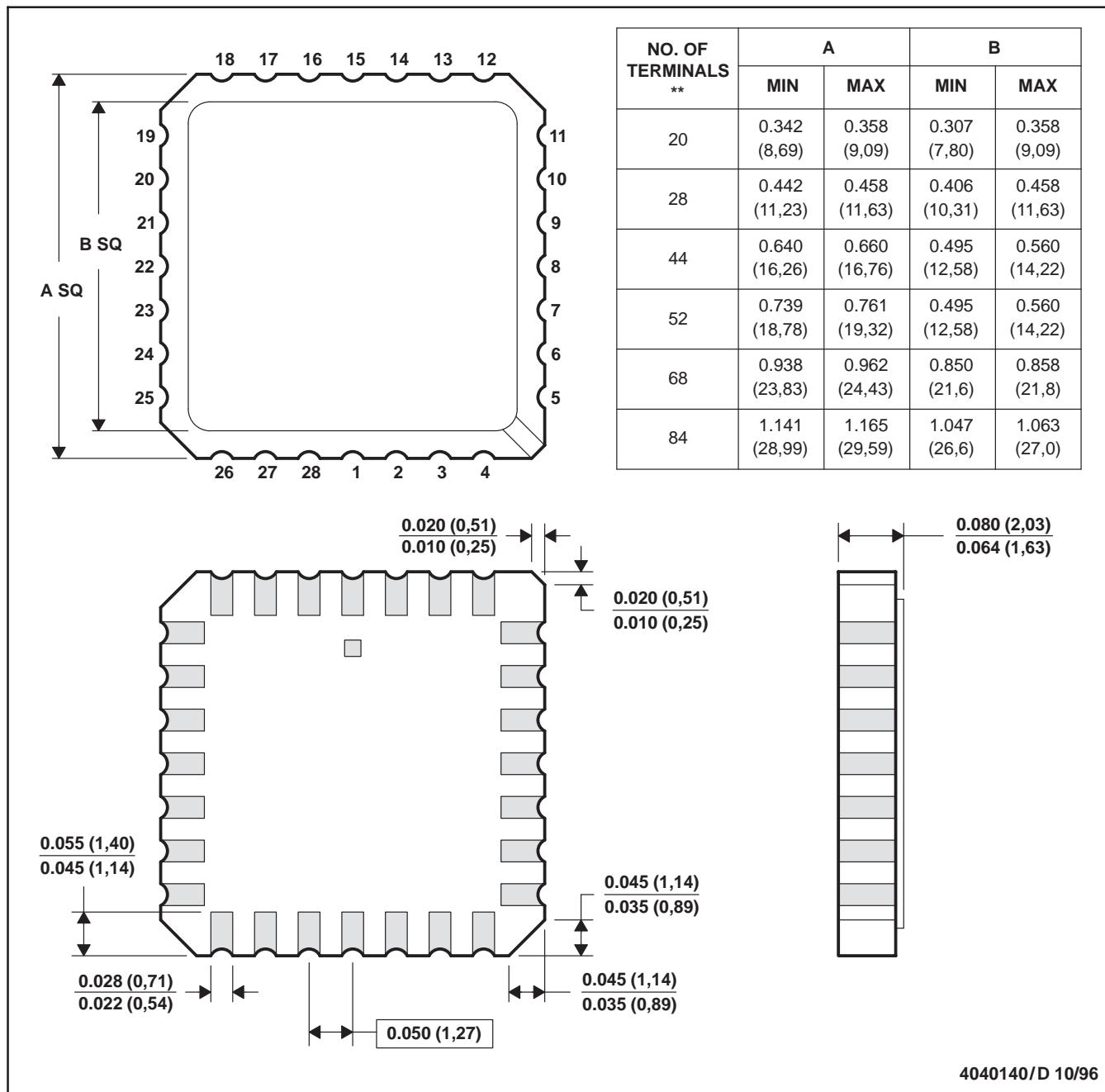
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

## 28 TERMINAL SHOWN



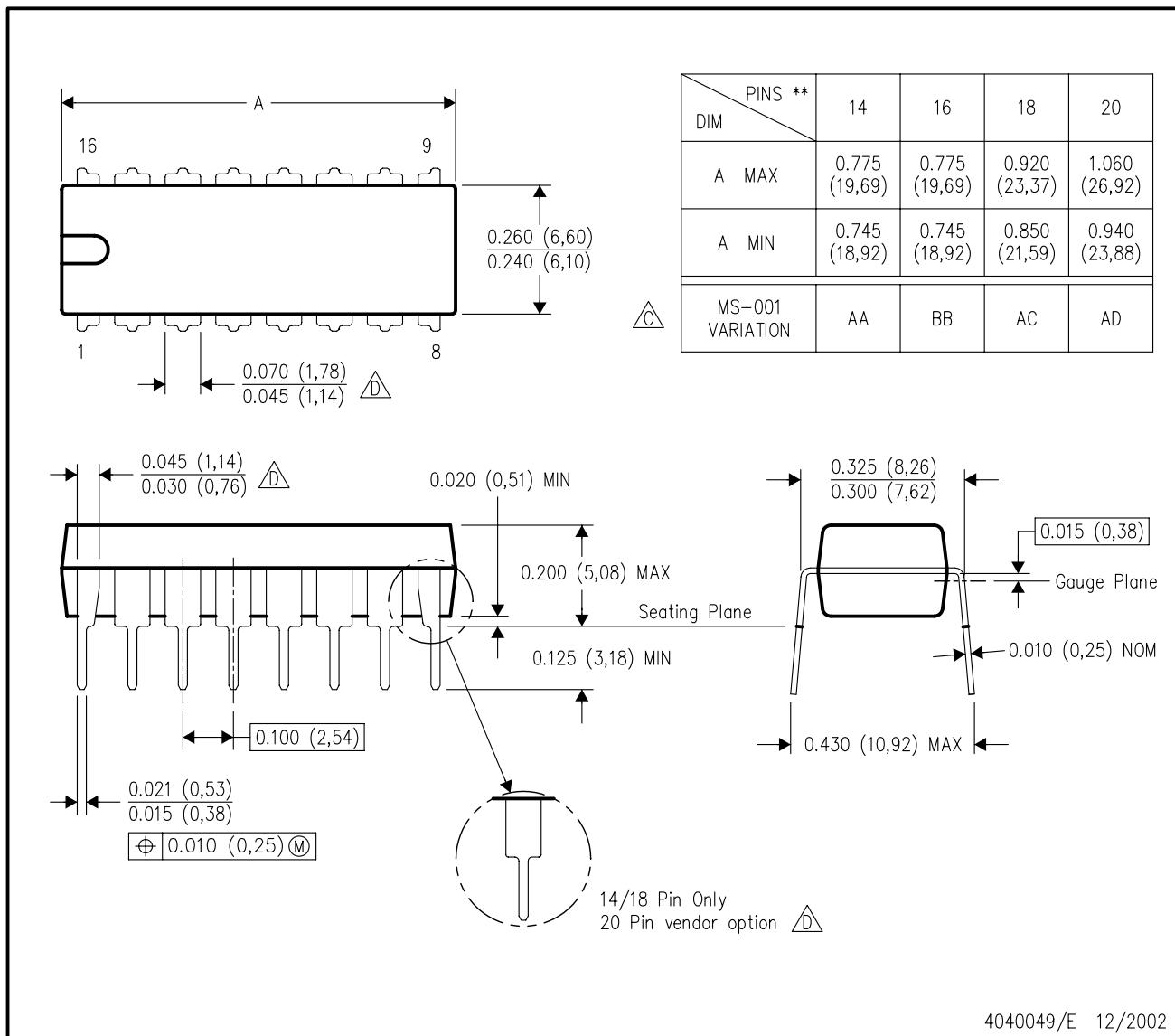
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



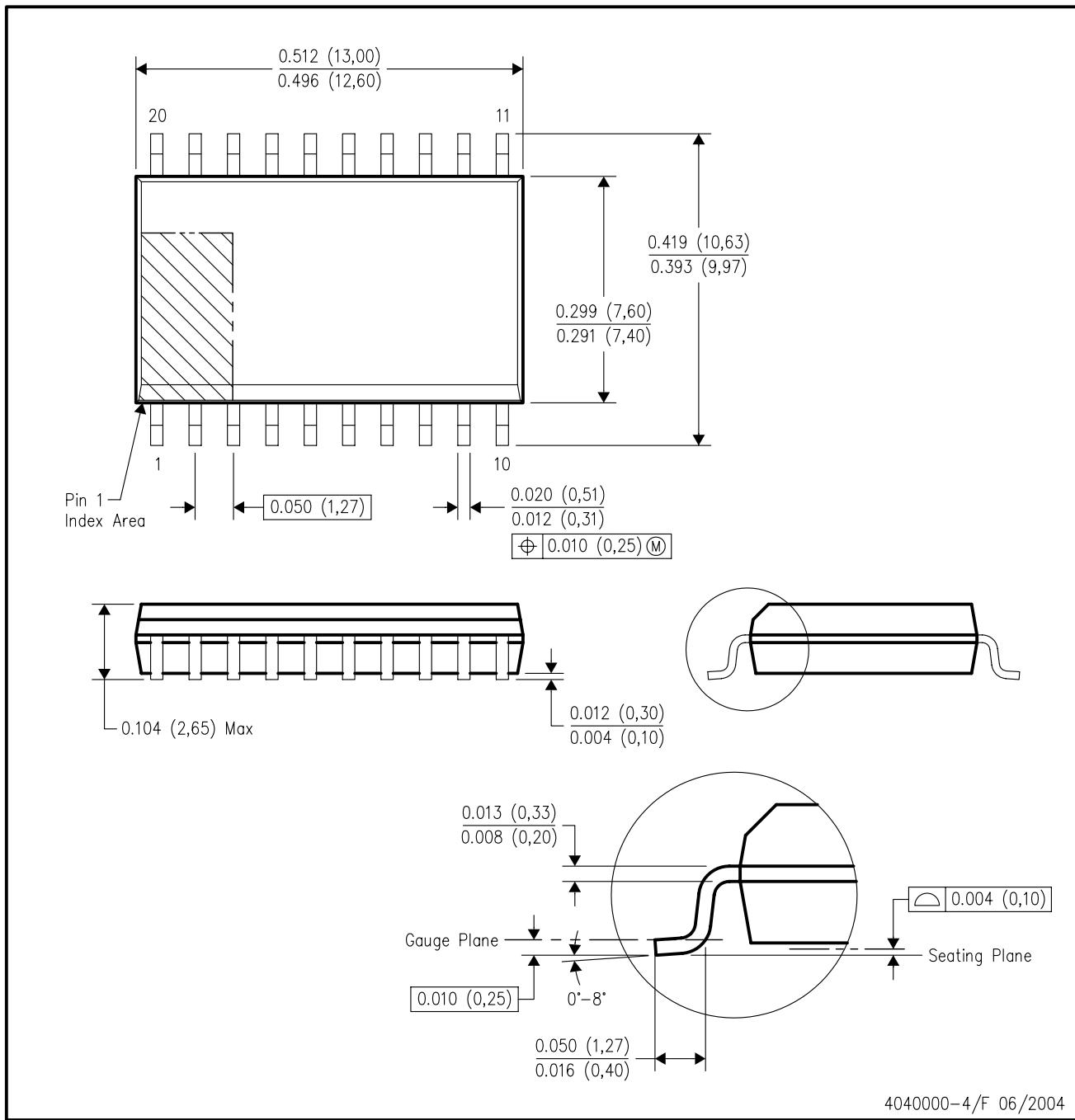
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

## NS (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



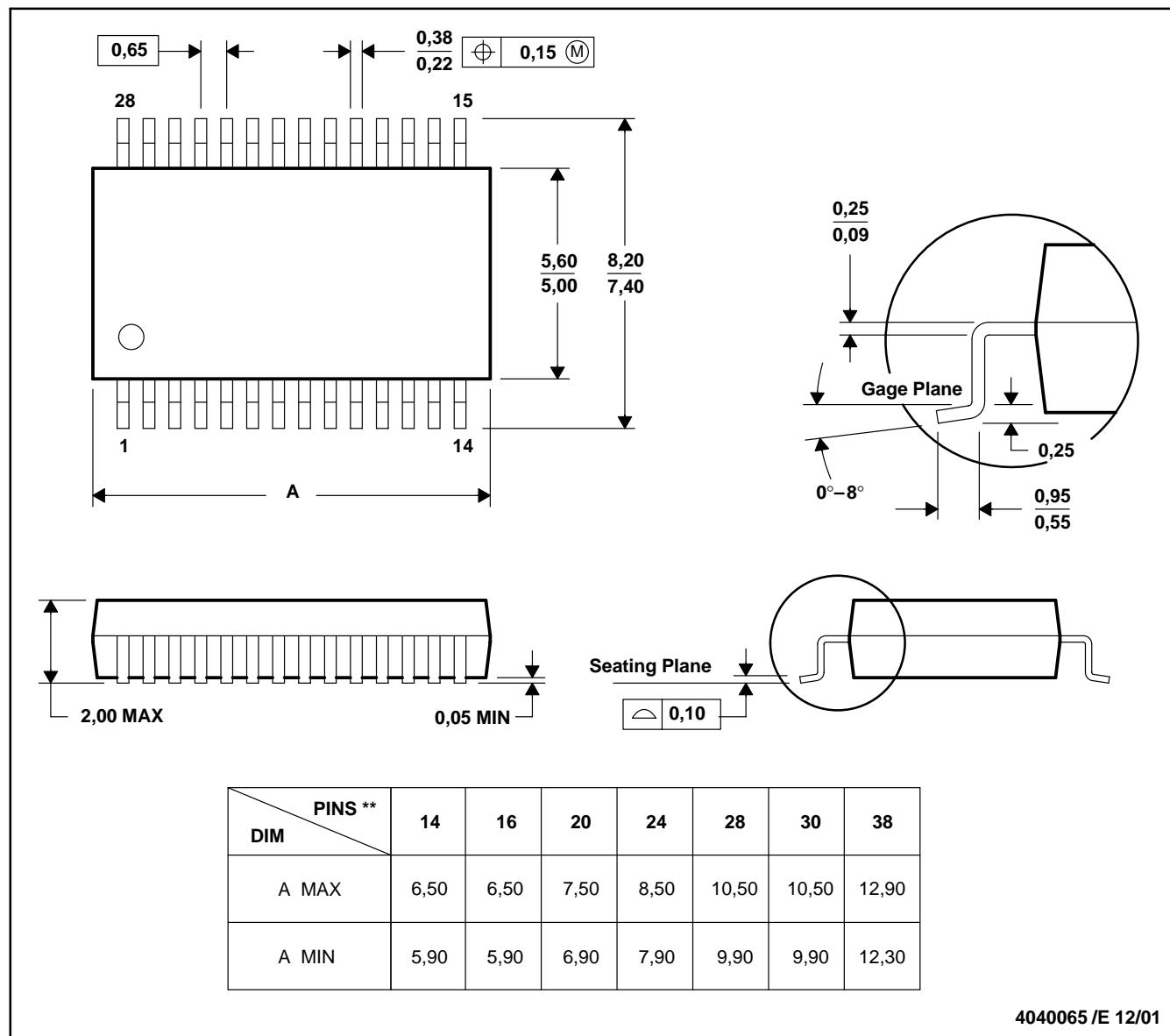
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

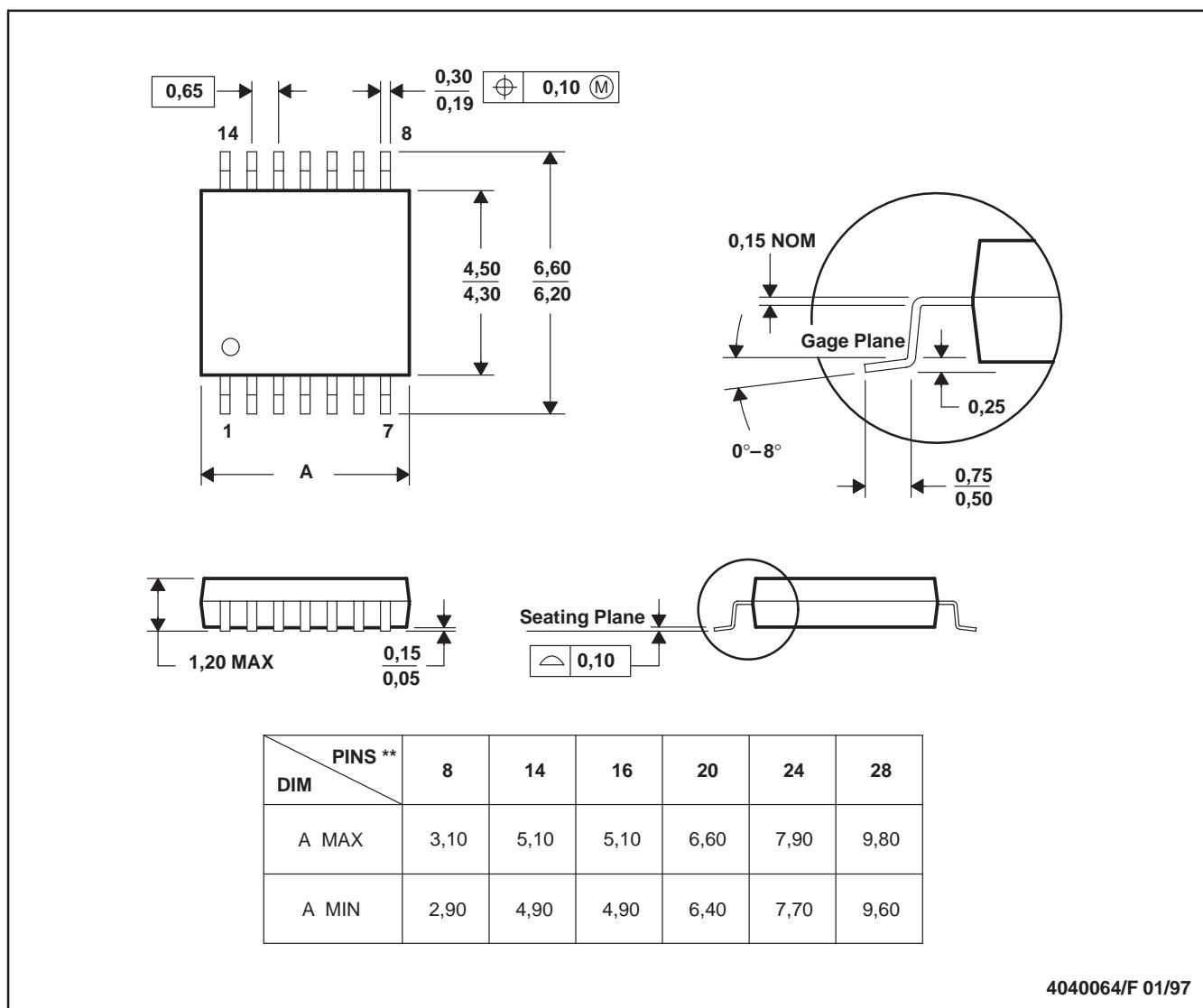


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

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