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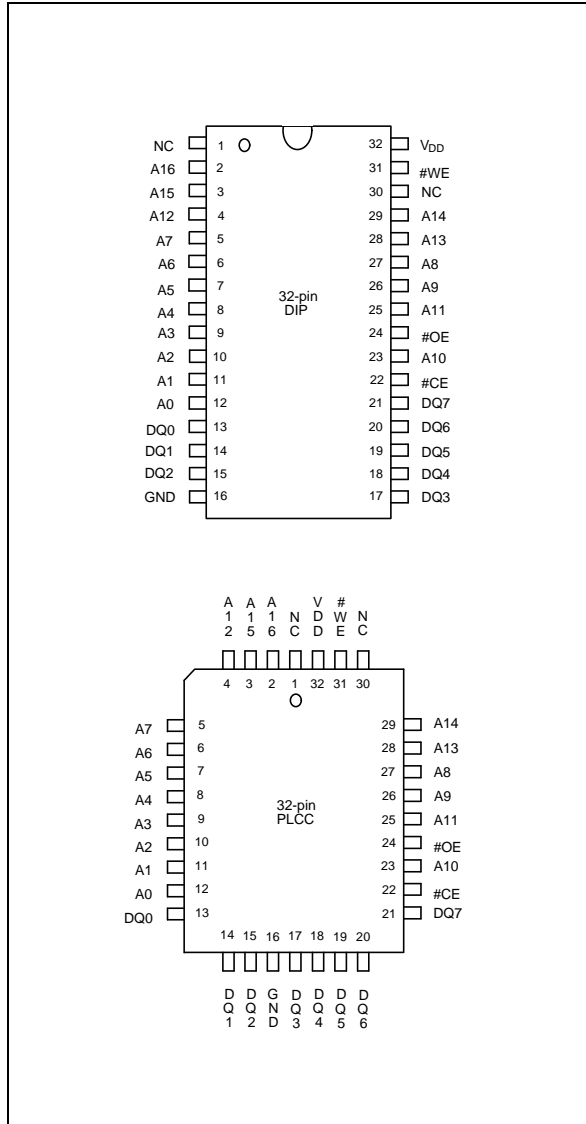# 128K ´ 8 CMOS FLASH MEMORY

GENERAL DESCRIPTION

The W29EE012 is a 1-megabit, 5-volt only CMOS flash memory organized as 128K × 8 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29EE012 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.
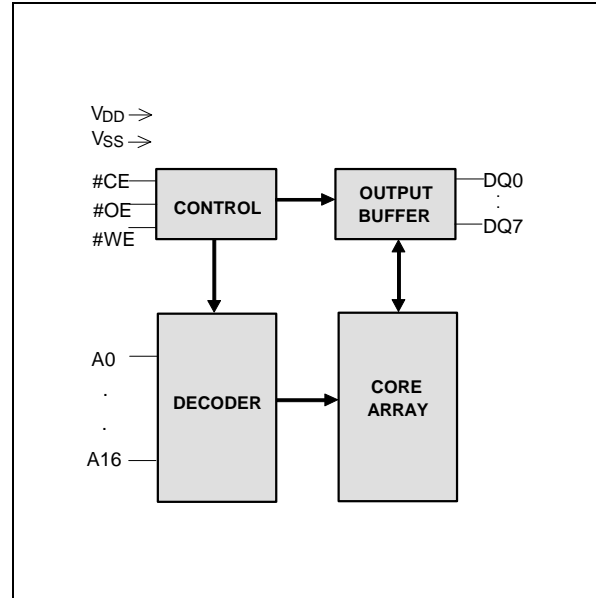
FEATURES

- Single 5-volt program and erase operations
- Fast page-write operations
  - 128 bytes per page
  - Page program cycle: 10 mS (max.)
  - Effective byte-program cycle time: 39 μS
  - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Page program/erase cycles: 1,000
- Ten-year data retention
- Software and hardware data protection

- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic program timing with internal V_{PP} generation
- End of program detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard byte-wide pinouts

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PIN CONFIGURATIONS

```
         32-pin DIP
    NC   1 O      32  VDD
    A16  2        31  #WE
    A15  3        30  NC
    A12  4        29  A14
    A7   5        28  A13
    A6   6        27  A8
    A5   7        26  A9
    A4   8        25  A11
    A3   9        24  #OE
    A2   10       23  A10
    A1   11       22  #CE
    A0   12       21  DQ7
    DQ0  13       20  DQ6
    DQ1  14       19  DQ5
    DQ2  15       18  DQ4
    GND  16       17  DQ3
```

```
        A  A  A        V  #
        1  1  1  N  N  D  W  N
        2  5  6  C  C  D  E  C
        4  3  2  1  32 31 30
    A7   5                29  A14
    A6   6                28  A13
    A5   7                27  A8
    A4   8   32-pin       26  A9
    A3   9   PLCC         25  A11
    A2   10               24  #OE
    A1   11               23  A10
    A0   12               22  #CE
    DQ0  13               21  DQ7
        14 15 16 17 18 19 20
        D  D  G  D  D  D  D
        Q  Q  N  Q  Q  Q  Q
        1  2  D  3  4  5  6
```

BLOCK DIAGRAM

PIN DESCRIPTION

SYMBOL	PIN NAME
A0 – A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29EE012 is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

Page Write Mode

The W29EE012 is programmed on a page basis. Every page contains 128 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FFh" during programming of the page.

The write operation is initiated by forcing #CE and #WE low and #OE high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device. Step 2 is an internal programming cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either #CE or #WE, whichever occurs last. The data are latched by the rising edge of either #CE or #WE, whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 200 μS, after the initial byte-load cycle, the W29EE012 will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional byte is loaded into the page buffer within 300 μS (T_{BLCO}) from the last byte-load cycle, i.e., there is no subsequent #WE high-to-low transition after the last rising edge of #WE. A_7 to A_{16} specify the page address. All bytes that are loaded into the page buffer must have the same page address. A_0 to A_6 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal programming cycle, all data in the page buffers, i.e., 128 bytes of data, are written simultaneously into the memory array. Before the completion of the internal programming cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a series of three-byte program commands (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29EE012 is shipped with the software data unprotection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte program command cycle. Once enabled, the software data protection will remain enabled unless the disable commands are issued. A power transition will not reset the software data protection feature. To reset the device to unprotected mode, a six-byte command sequence is required. See Table 3 for specific codes and Figure 10 for the timing diagram.

Hardware Data Protection

The integrity of the data stored in the W29EE012 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming and operation are inhibited when V_{DD} is less than 3.8V.

(3) Write Inhibit Mode: Forcing #OE low, #CE high, or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

Data Polling (DQ$_7$)-Write Status Detection

The W29EE012 includes a data polling feature to indicate the end of a programming cycle. When the W29EE012 is in the internal programming cycle, any attempt to read DQ$_7$ of the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the programming cycle is completed. DQ$_7$ will show the true data.

Toggle Bit (DQ$_6$)-Write Status Detection

In addition to data polling, the W29EE012 provides another method for determining the end of a program cycle. During the internal programming cycle, any consecutive attempts to read DQ$_6$ will produce alternating 0's and 1's. When the programming cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

5-Volt-Only Software Chip Erase

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycles, the device enters the internal chip erase mode, which is automatically timed and will be completed in 50 mS. The host system is not required to provide any control or timing during this operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (DAh). A read from address 0001H outputs the device code (C1h). The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing #CE and #OE low, #WE high, and raising A9 to 12 volts.

Note: The hardware SID read function is not included in all parts; please refer to Ordering Information for details.

TABLE OF OPERATING MODES

Operating Mode Selection

Operating Range = 0 to 70°C (Ambient Temperature), $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $V_{HH} = 12V$
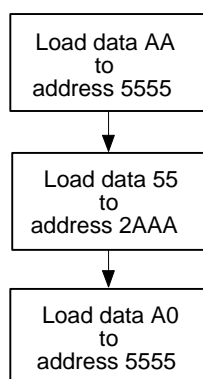
MODE	PINS				
	#CE	#OE	#WE	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	Din
Standby	V_{IH}	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}
	X	X	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
5-Volt Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Product ID	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1-A16 = V_{IL}; A9 = V_{HH}	Manufacturer Code DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}; A1-A16 = V_{IL}; A9 = V_{HH}	Device Code C1 (Hex)

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Command Codes for Software Data Protection

BYTE SEQUENCE	TO ENABLE PROTECTION		TO DISABLE PROTECTION	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	A0H	5555H	80H
3 Write	-	-	5555H	AAH
4 Write	-	-	2AAAH	55H
5 Write	-	-	5555H	20H

Software Data Protection Acquisition Flow

Software Data Protection Enable Flow

Load data AA
to
address 5555

↓

Load data 55
to
address 2AAA

↓

Load data A0
to
address 5555

Software Data Protection Disable Flow

Load data AA
to
address 5555

↓

Load data 55
to
address 2AAA

↓

Load data 80
to
address 5555

↓

Load data AA
to
address 5555

↓

Load data 55
to
address 2AAA

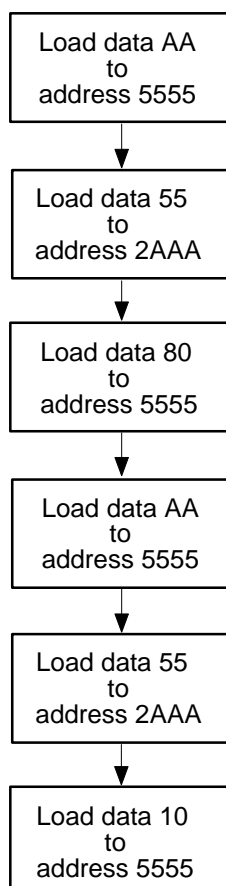↓

Load data 20
to
address 5555
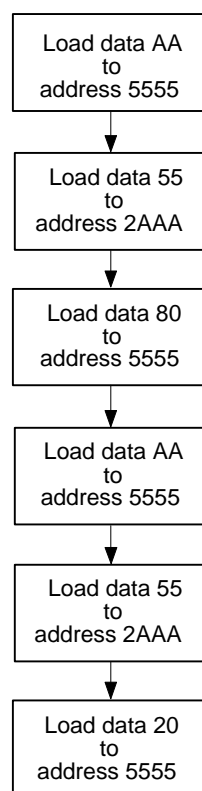
Notes for software program code:

Data Format: DQ7 − DQ0 (Hex)

Address Format: A14 − A0 (Hex)

Command Codes for Software Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	80H
3 Write	5555H	AAH
4 Write	2AAAH	55H
5 Write	5555H	10H

Sofware Chip Erase Acquisition Flow

```
Load data AA
to
address 5555
      |
      v
Load data 55
to
address 2AAA
      |
      v
Load data 80
to
address 5555
      |
      v
Load data AA
to
address 5555
      |
      v
Load data 55
to
address 2AAA
      |
      v
Load data 10
to
address 5555
```

Notes for software chip erase:

Data Format: DQ7 − DQ0 (Hex)

Address Format: A14 − A0 (Hex)

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Command Codes for Product Identification

BYTE SEQUENCE	SOFTWARE PRODUCT IDENTIFICATION ENTRY		SOFTWARE PRODUCT IDENTIFICATION EXIT	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	80H	5555H	F0H
3 Write	5555H	AAH	-	-
4 Write	2AAAH	55H	-	-
5 Write	5555H	60H	-	-
	Pause 10 μS		Pause 10 μS	

Software Product Identification Acquisition Flow

Product Identification Entry(1)   Product Identification Mode(2,3)   Product Identification

Load data AA to address 5555

Load data 55 to address 2AAA

Load data 80 to address 5555

Load data AA to address 5555

Load data 55 to address 2AAA

Load data 60 to address 5555

Pause 10 μS

Read address = 0 data = DA

Read address = 1 data = C1

Load data AA to address 5555

Load data 55 to address 2AAA

Load data FO to address 5555

Pause 10 μS

Normal Mode (4)
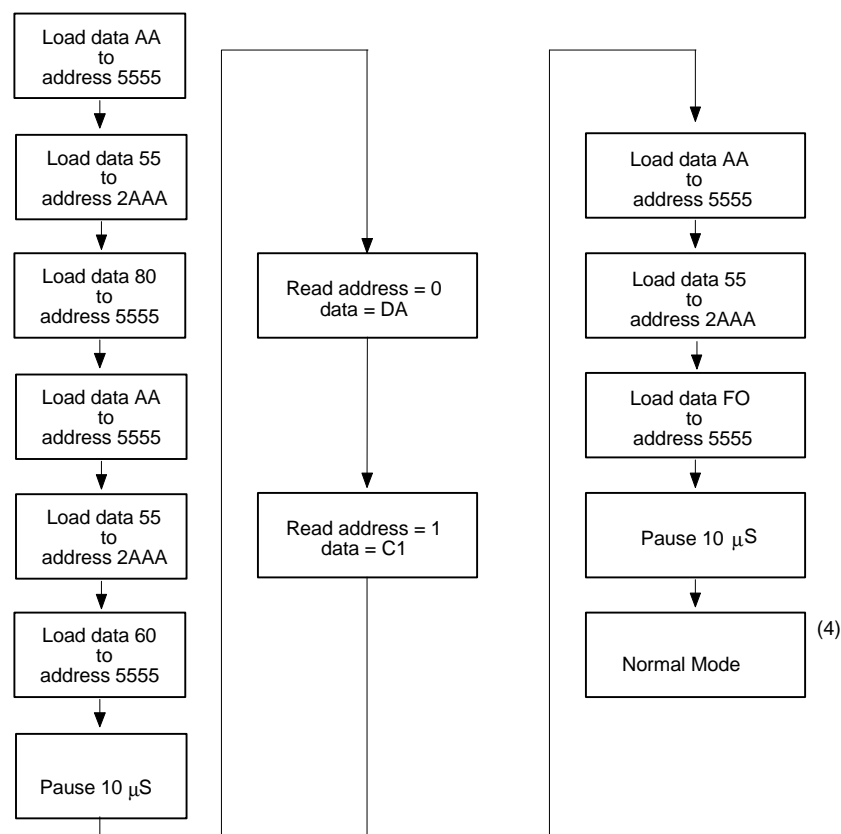
Notes for software product identification:

(1) Data format: DQ7 − DQ0 (Hex); address format: A14 − A0 (Hex).

(2) A1 − A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification mode if power down.

(4) The device returns to standard operation mode.

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V$_{SS}$ Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential Except #OE	-0.5 to V$_{DD}$ +1.0	V
Transient Voltage (≤20 nS) on Any Pin to Ground Potential	-1.0 to V$_{DD}$ +1.0	V
Voltage on #OE Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V$_{DD}$ = 5.0V ±10%, V$_{SS}$ = 0V, T$_A$ = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I$_{CC}$	#CE = #OE = V$_{IL}$, #WE = V$_{IH}$, all I/Os open Address inputs = V$_{IL}$/V$_{IH}$, at f = 5 MHz	-	-	50	mA
Standby V$_{DD}$ Current (TTL input)	I$_{SB1}$	#CE = V$_{IH}$, all I/Os open Other inputs = V$_{IL}$/V$_{IH}$	-	2	3	mA
Standby V$_{DD}$ Current (CMOS input)	I$_{SB2}$	#CE = V$_{DD}$ -0.3V, all I/Os open Other inputs = V$_{DD}$ -0.3V/GND	-	20	100	µA
Input Leakage Current	I$_{LI}$	V$_{IN}$ = GND to V$_{DD}$	-	-	1	µA
Output Leakage Current	I$_{LO}$	V$_{IN}$ = GND to V$_{DD}$	-	-	10	µA
Input Low Voltage	V$_{IL}$	-	-0.3	-	0.8	V
Input High Voltage	V$_{IH}$	-	2.0	-	V$_{DD}$ +0.5	V
Output Low Voltage	V$_{OL}$	I$_{OL}$ = 2.1 mA	-	-	0.45	V
Output High Voltage	V$_{OH}$	I$_{OH}$ = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	T$_{PU.READ}$	100	µS
Power-up to Write Operation	T$_{PU.WRITE}$	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF

AC CHARACTERISTICS

AC Test Conditions

(V_{DD} = 5V ±10%)

PARAMETER	CONDITIONS	
	90 nS/120 nS	150 nS
Input Pulse Levels	0V/3V	0V/3V
Input Rise/Fall Time	5 nS	10 nS
Input/Output Timing Level	1.5V/1.5V	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 100 pF	1 TTL Gate and C_L = 100 pF

AC Test Load and Waveforms
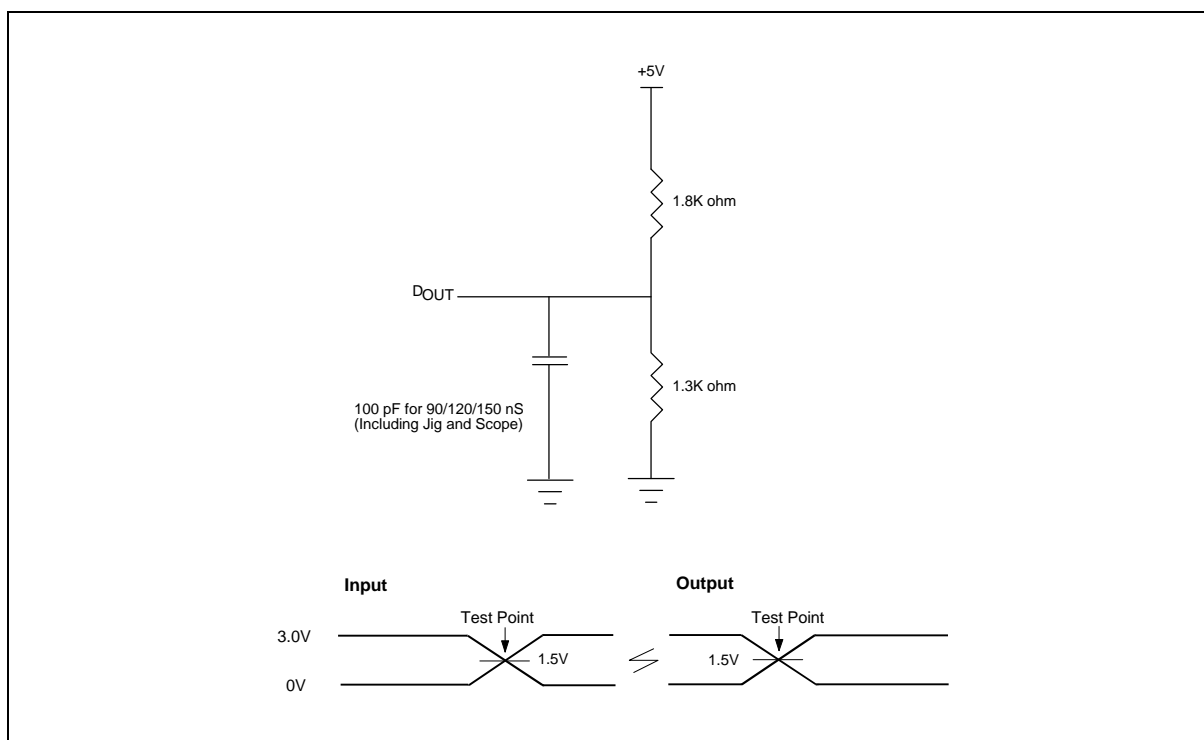
Read Cycle Timing Parameters

(V$_{DD}$ = 5.0V ±10%, V$_{SS}$ = 0V, T$_A$ = 0 to 70° C)

PARAMETER	SYM.	W29EE012		UNIT
		MIN.	MAX.	
Read Cycle Time	T$_{RC}$	150	-	nS
Chip Enable Access Time	T$_{CE}$	-	150	nS
Address Access Time	T$_{AA}$	-	150	nS
Output Enable Access Time	T$_{OE}$	-	70	nS
#CE Low to Active Output	T$_{CLZ}$	0	-	nS
#OE Low to Active Output	T$_{OLZ}$	0	-	nS
#CE High to High-Z Output	T$_{CHZ}$	-	45	nS
#OE High to High-Z Output	T$_{OHZ}$	-	45	nS
Output Hold from Address Change	T$_{OH}$	0	-	nS

Byte/Page-Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write Cycle (Erase and Program)	T$_{WC}$	-	-	10	mS
Address Setup Time	T$_{AS}$	0	-	-	nS
Address Hold Time	T$_{AH}$	50	-	-	nS
#WE and #CE Setup Time	T$_{CS}$	0	-	-	nS
#WE and #CE Hold Time	T$_{CH}$	0	-	-	nS
#OE High Setup Time	T$_{OES}$	10	-	-	nS
#OE High Hold Time	T$_{OEH}$	10	-	-	nS
#CE Pulse Width	T$_{CP}$	70	-	-	nS
#WE Pulse Width	T$_{WP}$	70	-	-	nS
#WE High Width	T$_{WPH}$	150	-	-	nS
Data Setup Time	T$_{DS}$	50	-	-	nS
Data Hold Time	T$_{DH}$	10	-	-	nS
Byte Load Cycle Time	T$_{BLC}$	0.22	-	200	μS
Byte Load Cycle Time-out	T$_{BLCO}$	300	-	-	μS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

   (a) High level signal's reference level is V$_{IH}$ and (b) low level signal's reference level is V$_{IL}$.

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Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W29EE012-90		W29EE012-12		W29EE012-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
#OE to Data Polling Output Delay	T_{OEP}	-	45	-	60	-	70	nS
#CE to Data Polling Output Delay	T_{CEP}	-	90	-	120	-	150	nS
#OE to Toggle Bit Output Delay	T_{OET}	-	45	-	60	-	70	nS
#CE to Toggle Bit Output Delay	T_{CET}	-	90	-	120	-	150	nS

TIMING WAVEFORMS

Read Cycle Timing Diagram
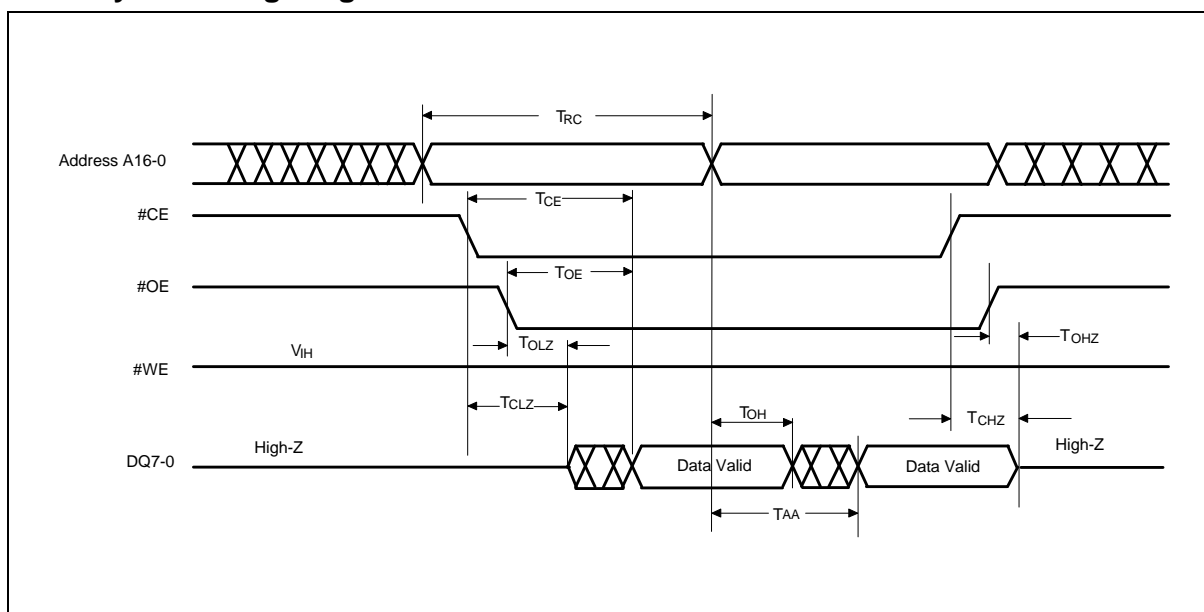
Timing Waveforms, continued

#WE Controlled Write Cycle Timing Diagram
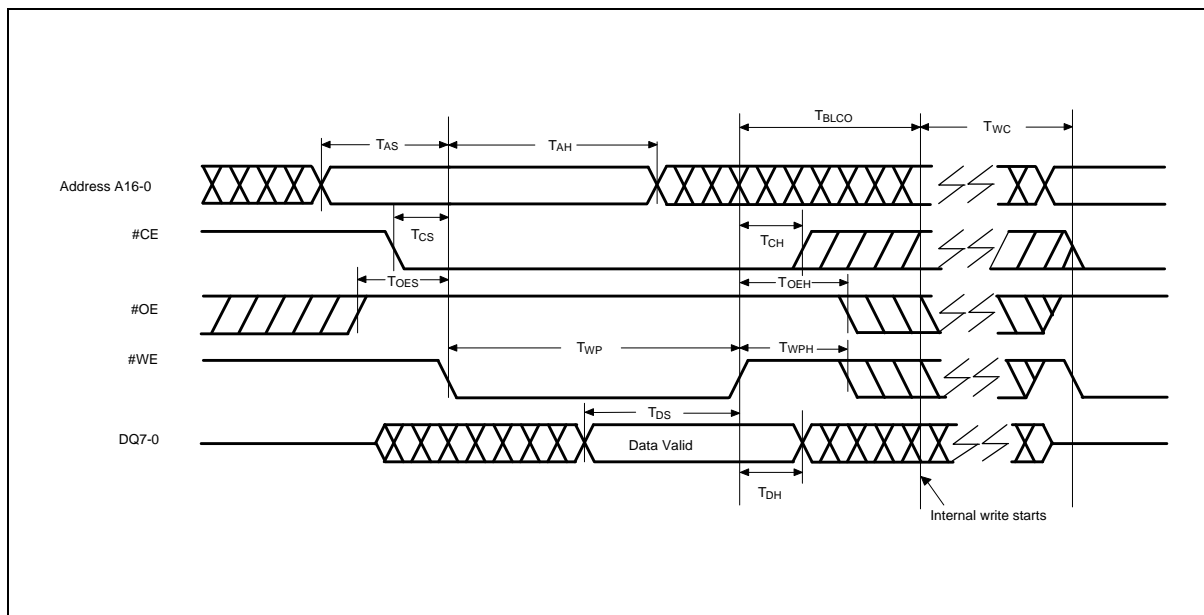
#CE Controlled Write Cycle Timing Diagram
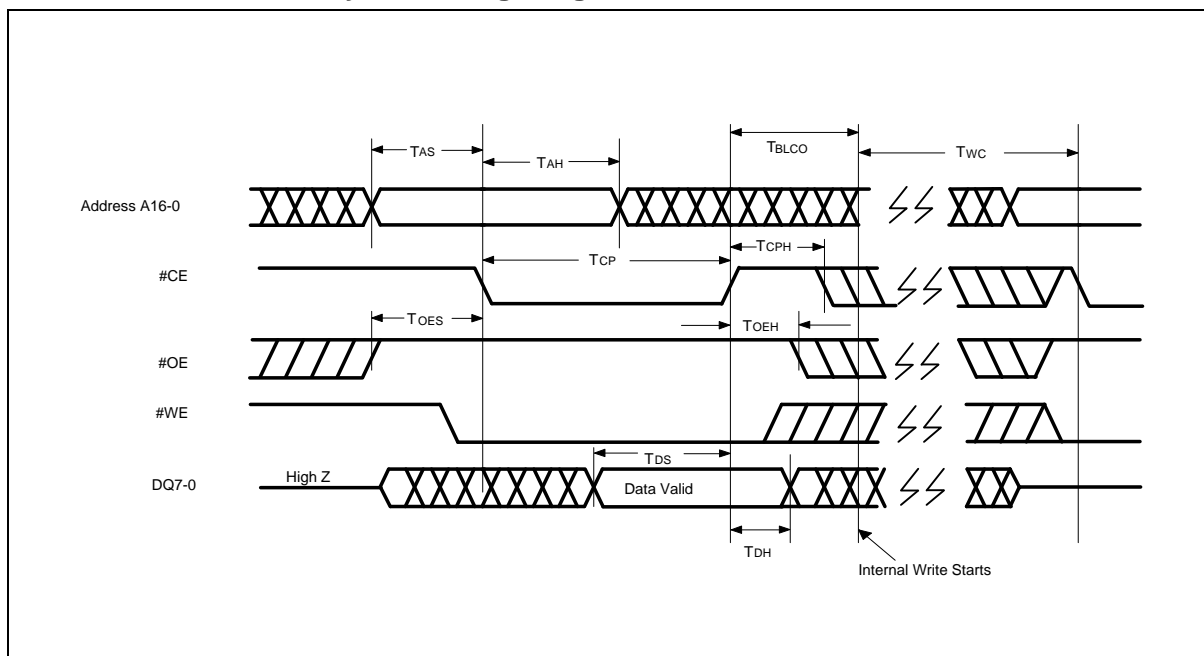
Timing Waveforms, continued

Page Write Cycle Timing Diagram
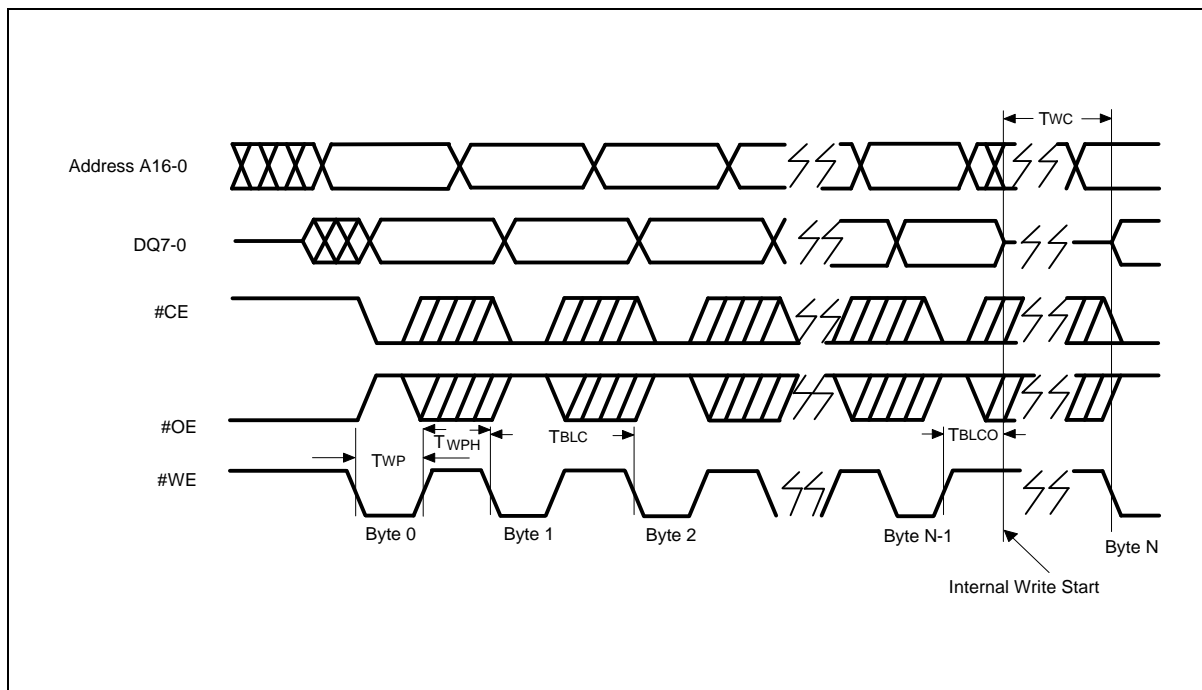
#DATA Polling Timing Diagram
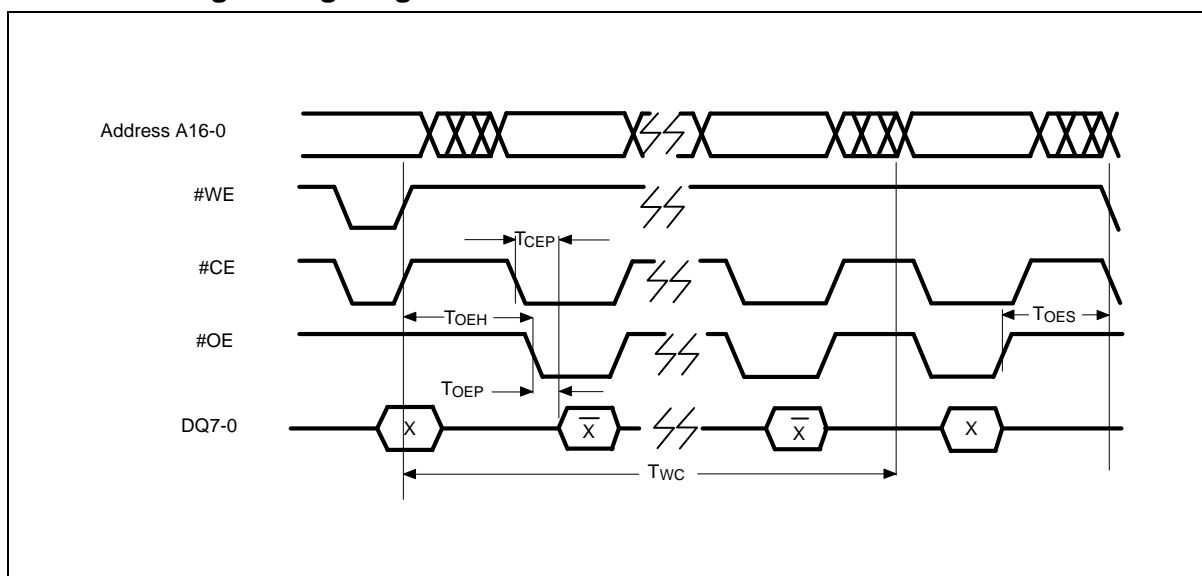
Timing Waveforms, continued

Toggle Bit Timing Diagram
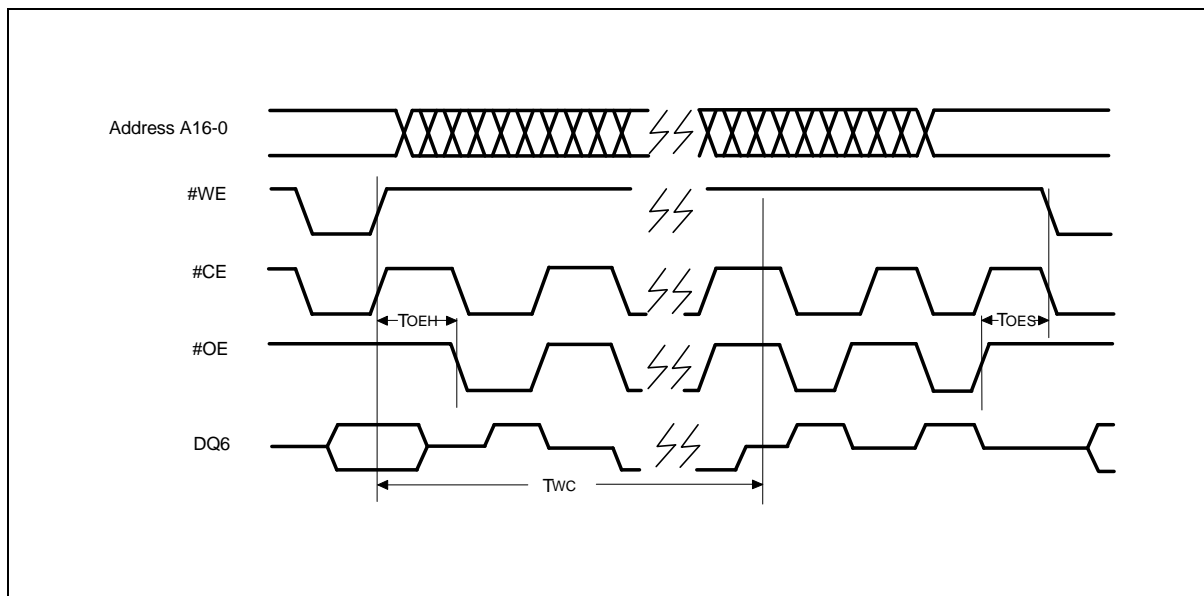
Page Write Timing Diagram Software Data Protection Mode

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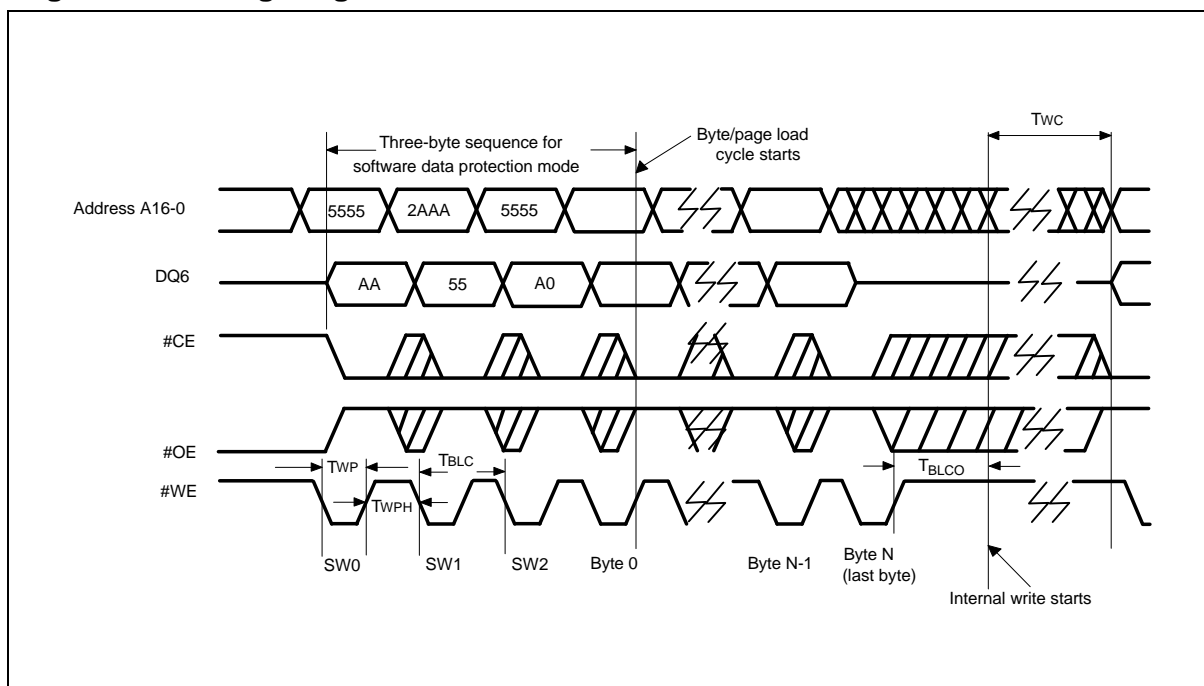
Timing Waveforms, continued

Reset Software Data Protection Timing Diagram
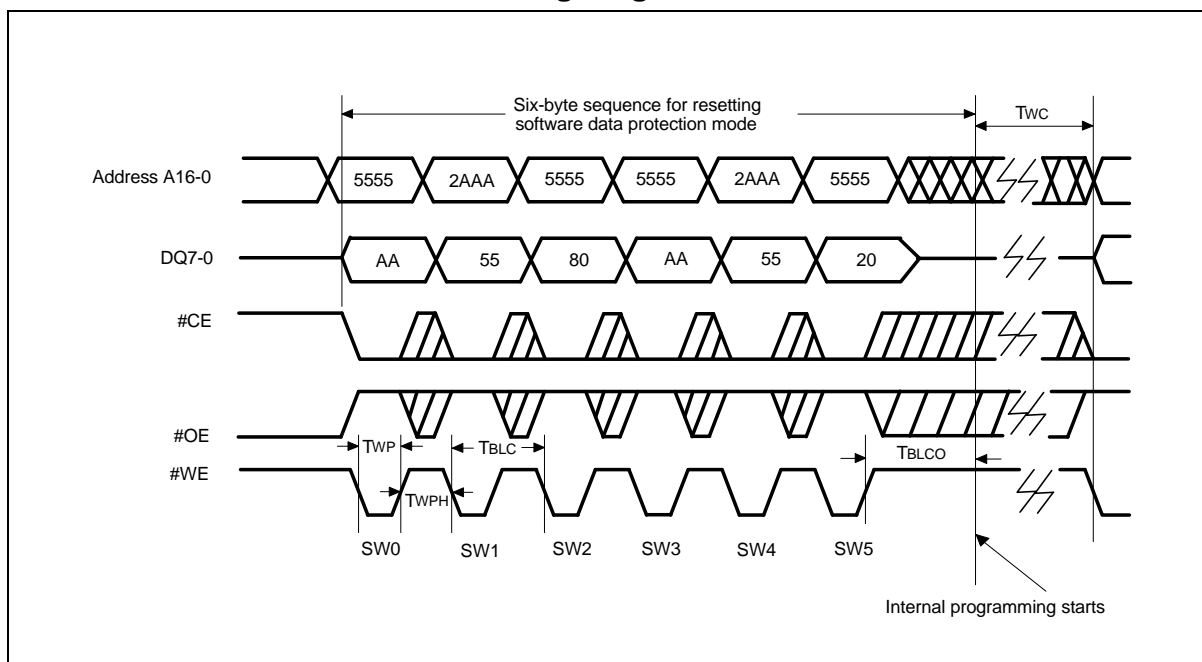
5 Volt-Only Software Chip Erase Timing Diagram
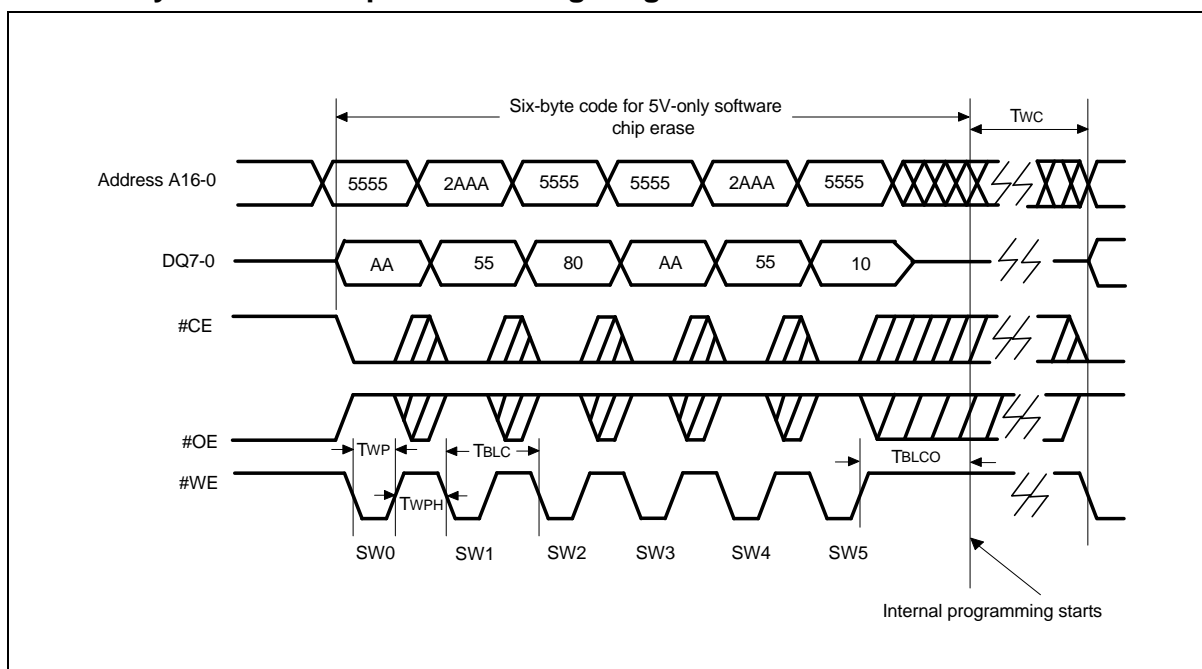
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V$_{DD}$ CURRENT MAX. (mA)	PACKAGE	HARDWARE SID READ FUNCTION
W29EE012		50	100	-	Y

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.

2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

3. In Hardware SID Read column: Y = with SID read function; N = without SID read function.

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BONDING PAD DIAGRAM
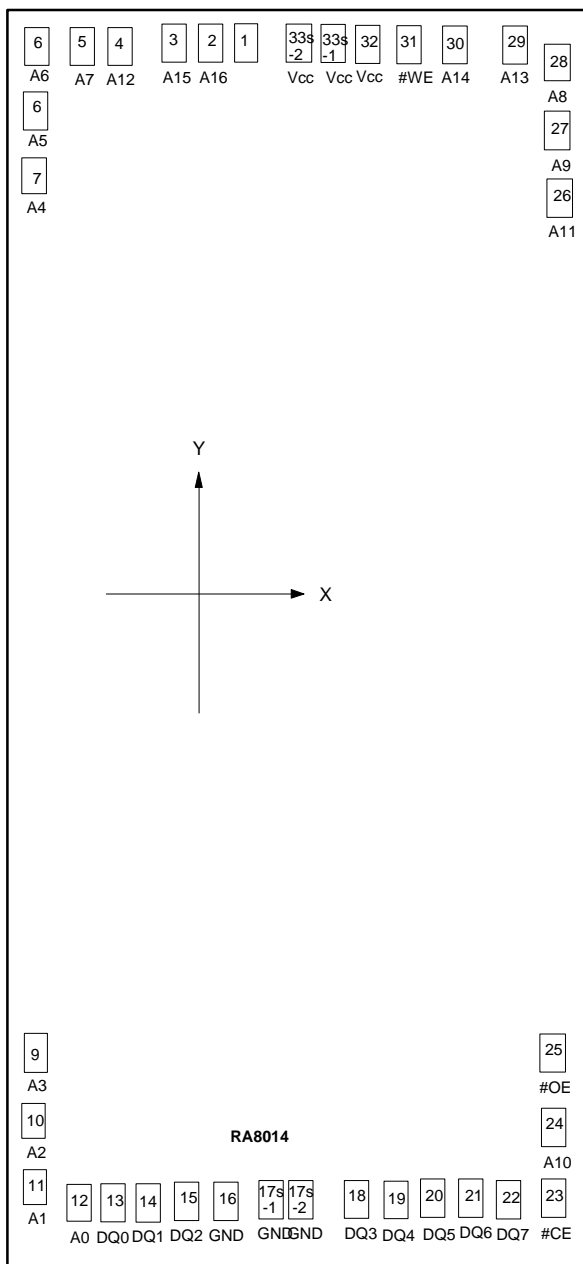
PAD NO.	X	Y
1	-187.04	1920.30
2	-380.84	1920.30
3	-517.64	1920.30
4	-1121.73	1920.30
5	-1258.52	1920.30
6	-1484.75	1901.22
7	-1484.75	1713.42
8	-1484.75	1576.62
9	-1453.92	-1577.46
10	-1453.92	-1742.70
11	-1453.92	-1879.50
12	-1240.62	-1923.06
13	-977.19	-1921.98
14	-727.22	-1921.98
15	-504.26	-1921.98
16	-264.72	-1900.20
17S-1	-86.90	-1900.20
17S-2	-1.70	-1900.20
18	286.06	-1909.98
19	509.01	-1909.98
20	758.98	-1909.98
21	981.94	-1909.98
22	1231.90	-1909.98
23	1469.29	-1897.26
24	1468.29	-1708.32
25	1469.29	-1571.52
26	1476.60	1564.62
27	1476.60	1752.42
28	1476.60	1889.22
29	1311.85	1920.30
30	891.00	1920.30
31	523.36	1920.30
32	310.36	1914.24
33S-1	180.16	1914.24
33S-2	94.96	1914.24

Note: For bare chip form (C.O.B.) applications, the substrate must be connected to VDD or left floating in the PCB layout.

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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jan. 1997	-	Initial Issued
A2	Apr. 2000	10	Modify V_{IH}/V_{IL} = 0V/3V and V_{OH}/V_{OL} = 1.5V/1.5V
A3	Mar. 26, 2002	1, 17, 19, 20	Delete Package Description
		1,11	Delete Access Time
		4, 17	Add in Hardware SID Read function note
		4	Modify V_{DD} Power Up/Down Detection in Hardware Data Protection
		18	Add Bonding Pad Diagram