



CY62128V Family

128K x 8 Static RAM

Features

- **Low voltage range:**
 - 2.7V–3.6V (CY62128V)
 - 2.3V–2.7V (CY62128V25)
 - 1.6V–2.0V (CY62128V18)
- **Low active power and standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The CY62128V family is composed of three high-performance CMOS static RAMs organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and

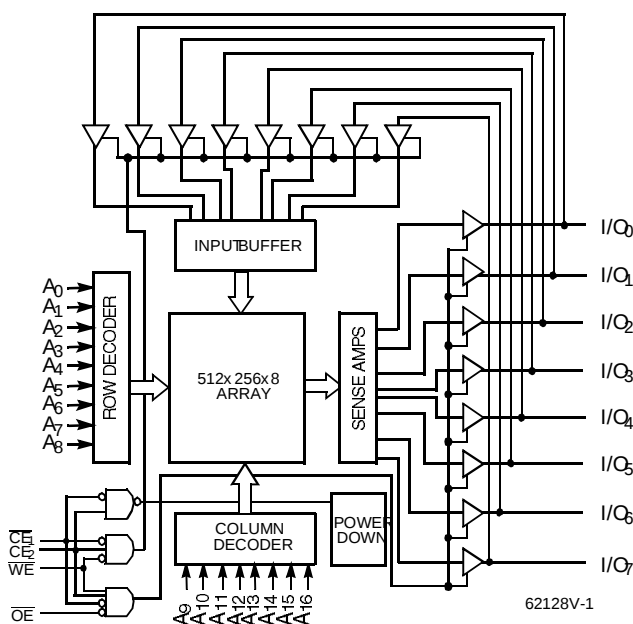
three-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected. The CY62128V family is available in the standard 450-mil-wide SOIC, TSOP, and STSOP packages.

Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and the chip enable two ($\overline{CE}_2$) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

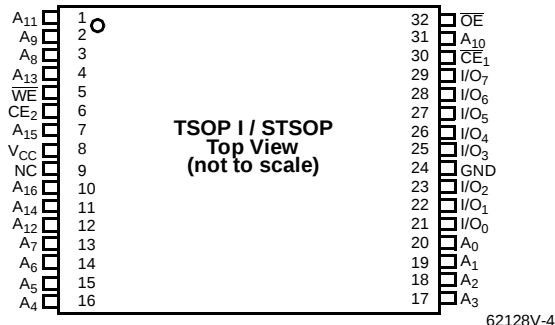
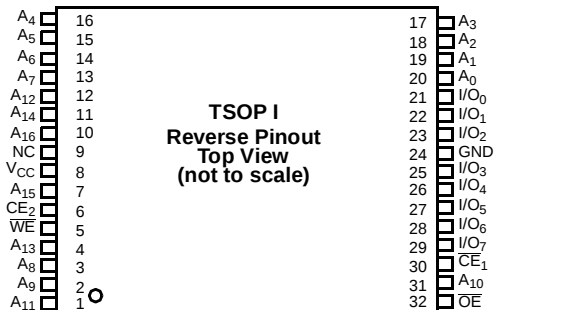
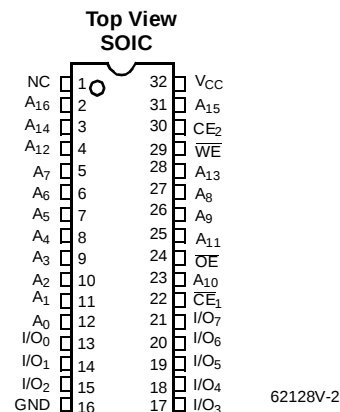
Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two ($\overline{CE}_2$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $\overline{CE}_2$ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, $\overline{CE}_2$ HIGH, and $\overline{WE}$ LOW).

Logic Block Diagram



Pin Configurations



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied 55°C to +125°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14) -0.5V to +4.6V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	1.6V to 3.6V
Industrial	-40°C to +85°C	1.6V to 3.6V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Commercial)			
					Operating (I_{CC})		Standby (I_{SB2})	
	Min.	Typ. ^[2]	Max.		Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62128V	2.7V	3.0V	3.6V	70 ns	20 mA	40 mA	0.4 μ A	100 μ A (15 μ A = LL)
CY62128V25	2.3V	2.5V	2.7V	100 ns	15 mA	20 mA	0.3 μ A	50 μ A (10 μ A = LL)
CY62128V18	1.6V	1.8V	2.0V	200 ns	10 mA	15 mA	0.3 μ A	30 μ A (10 μ A = LL)

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62128V-70			Unit
					Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −1.0 mA			2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA					0.4	V
V _{IH}	Input HIGH Voltage				2		V _{CC} +0.5V	V
V _{IL}	Input LOW Voltage				−0.5		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}			−1	±1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled			−1	±1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	L		20	40	mA
				LL				
			Ind'l	L				
				LL				
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l	L		15	300	μA
				LL				
			Ind'l	L				
				LL				
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} − 0.3V V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	L		0.4	100	μA
				LL			15	μA
			Ind'l	L			100	μA
				LL			30	μA

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$ Typ, $T_A = 25^\circ\text{C}$.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62128V25-100			CY62128V18-200			Unit
				Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −0.1 mA		2.4			0.8* V _{CC}			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 0.1 mA				0.4			0.2	V
V _{IH}	Input HIGH Voltage			2		V _{CC} +0.5	0.7* V _{CC}		V _{CC} +0.3	V
V _{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.3* V _{CC}	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		−1	±1	+1	−1	±0.1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		−1	±1	+1	−1	±0.1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	L		15	20		10	15	mA
			LL							
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	L		15	300		5	100	μA
			LL							
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$ V _{IN} ≥ V _{CC} − 0.3V or V _{IN} ≤ 0.3V, f = 0	L		0.4	50		0.4	30	μA
			LL			12			10	μA
			Indust'l Temp Range	LL				24		

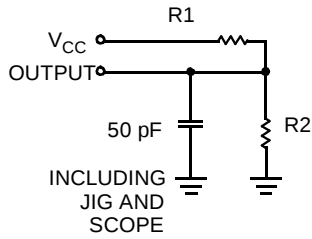
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.0V	6	pF
C _{OUT}	Output Capacitance		8	pF

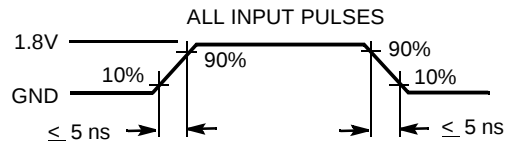
Note:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

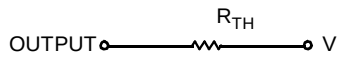


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62128V-6

Equivalent to: THÉVENIN EQUIVALENT

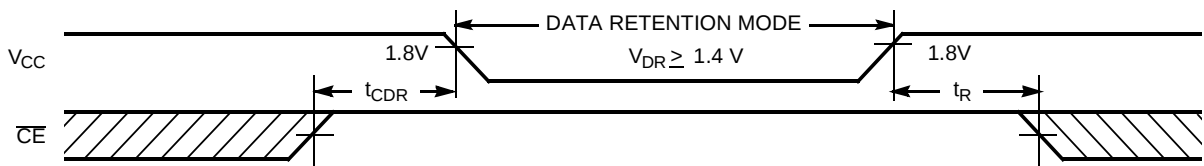


Parameters	3.3V	2.5V	1.8V	Unit
R1	1213	15909	10800	Ohms
R2	1378	4487	4154	Ohms
R _{TH}	645	3500	3000	Ohms
V _{TH}	1.75V	0.55V	0.50V	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description		Conditions ^[4]	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention			1.4			V
I _{CCDR}	Data Retention Current	Com'I	L		0.4	10	μA
			LL			10	μA
		Ind'I	L			20	μA
			LL			20	μA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time			0			ns
t _R	Operation Recovery Time			t _{RC}			ns

Data Retention Waveform



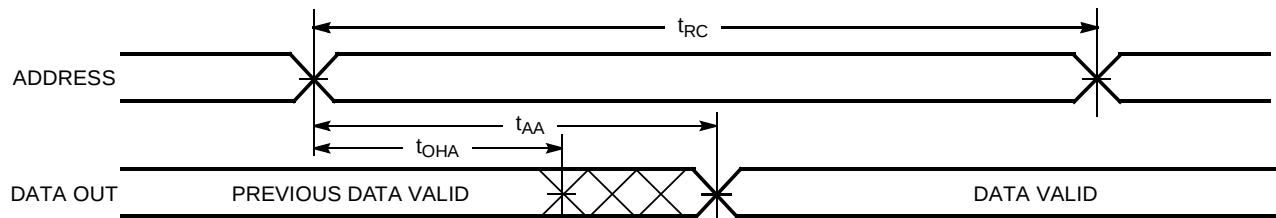
C62128V-7

Note:

- No input may exceed V_{CC}+0.3V.

Switching Characteristics Over the Operating Range^[5]

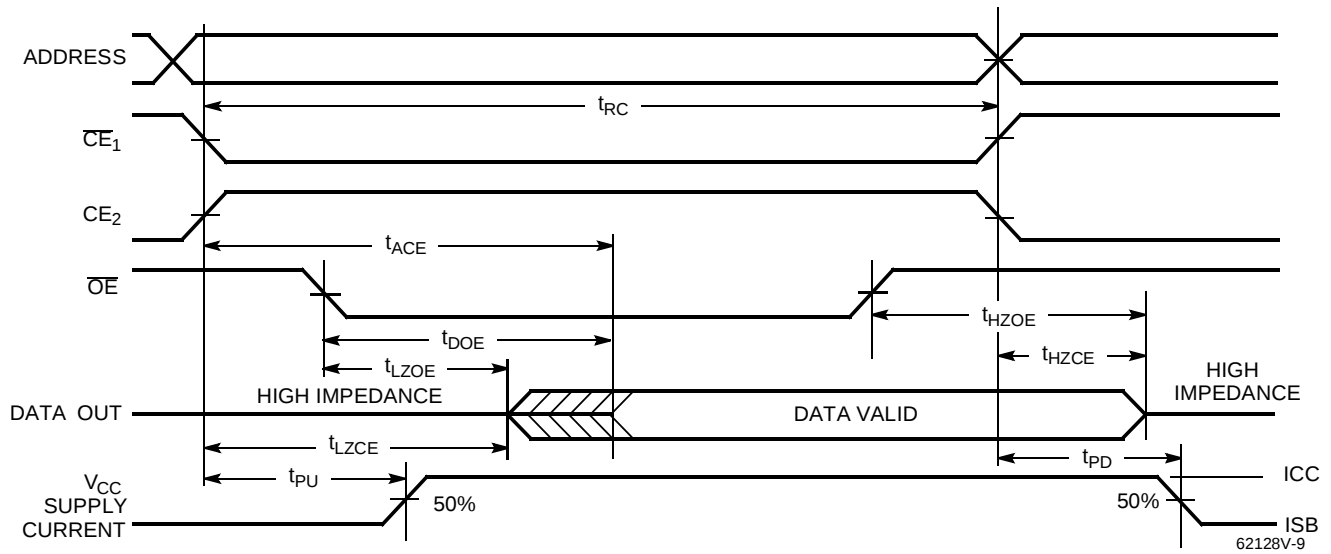
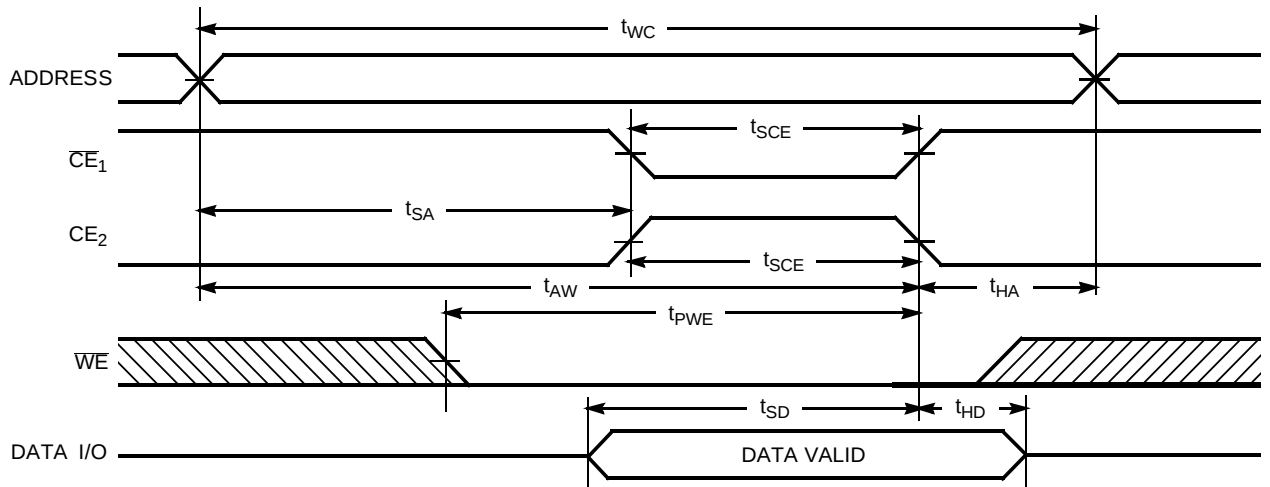
Parameter	Description	CY62128V-70		CY62128V25-100		CY62128V18-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	70		100		200		ns
t _{AA}	Address to Data Valid		70		100		200	ns
t _{OHA}	Data Hold from Address Change	10		10		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		70		100		200	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		35		75		125	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[6]	10		10		10		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[6, 7]		25		50		75	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[6]	10		10		10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[6, 7]		25		50		75	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		70		100		200	ns
WRITE CYCLE ^[8,9]								
t _{WC}	Write Cycle Time	70		100		200		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	60		100		190		ns
t _{AW}	Address Set-Up to Write End	60		100		190		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	55		90		125		ns
t _{SD}	Data Set-Up to Write End	30		60		100		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[6, 7]		25		50		100	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[6]	5		10		15		ns

Switching Waveforms
Read Cycle No. 1^[10, 11]


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Notes:

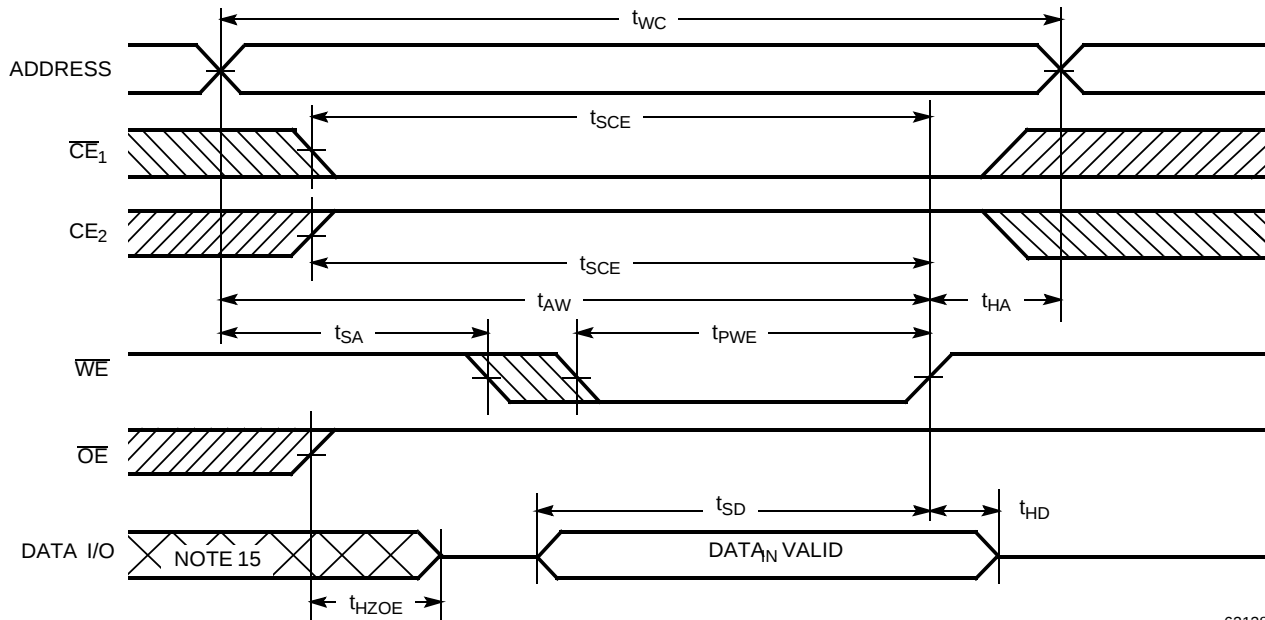
- Test conditions assume signal transition time of 5 ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ HIGH and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ signals must be LOW and $\overline{CE}_2$ HIGH to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .
- Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}, \overline{CE}_2 = V_{IH}$.
- $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 ($\overline{OE}$ Controlled)^[11,12]

Write Cycle No. 1 ($\overline{CE}_1$ or CE_2 Controlled)^[13,14]


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Notes:

12. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)^[13,14]


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Note:

15. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O ₀ –I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

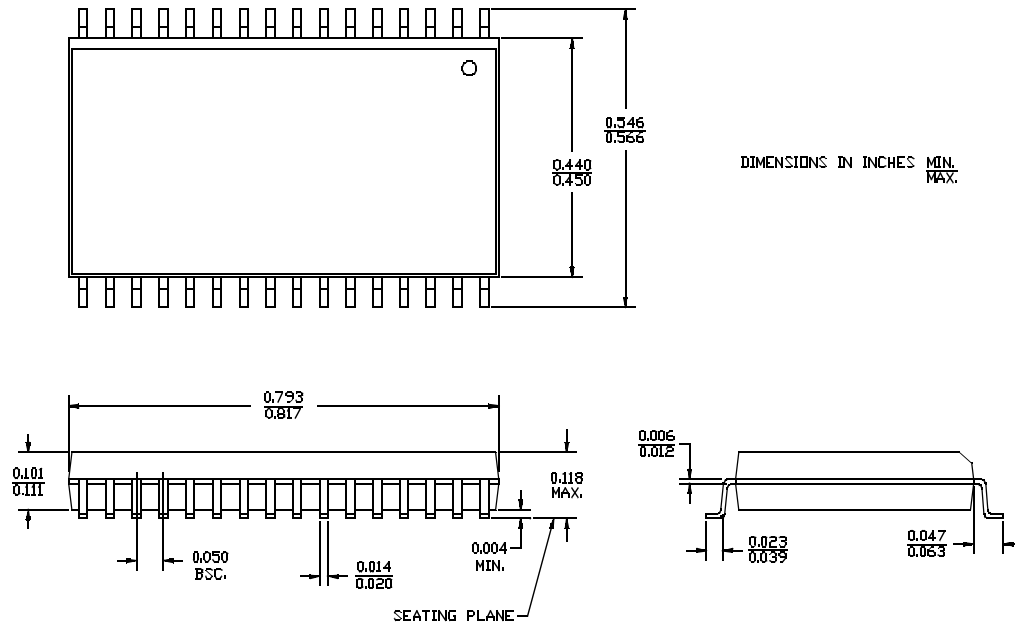
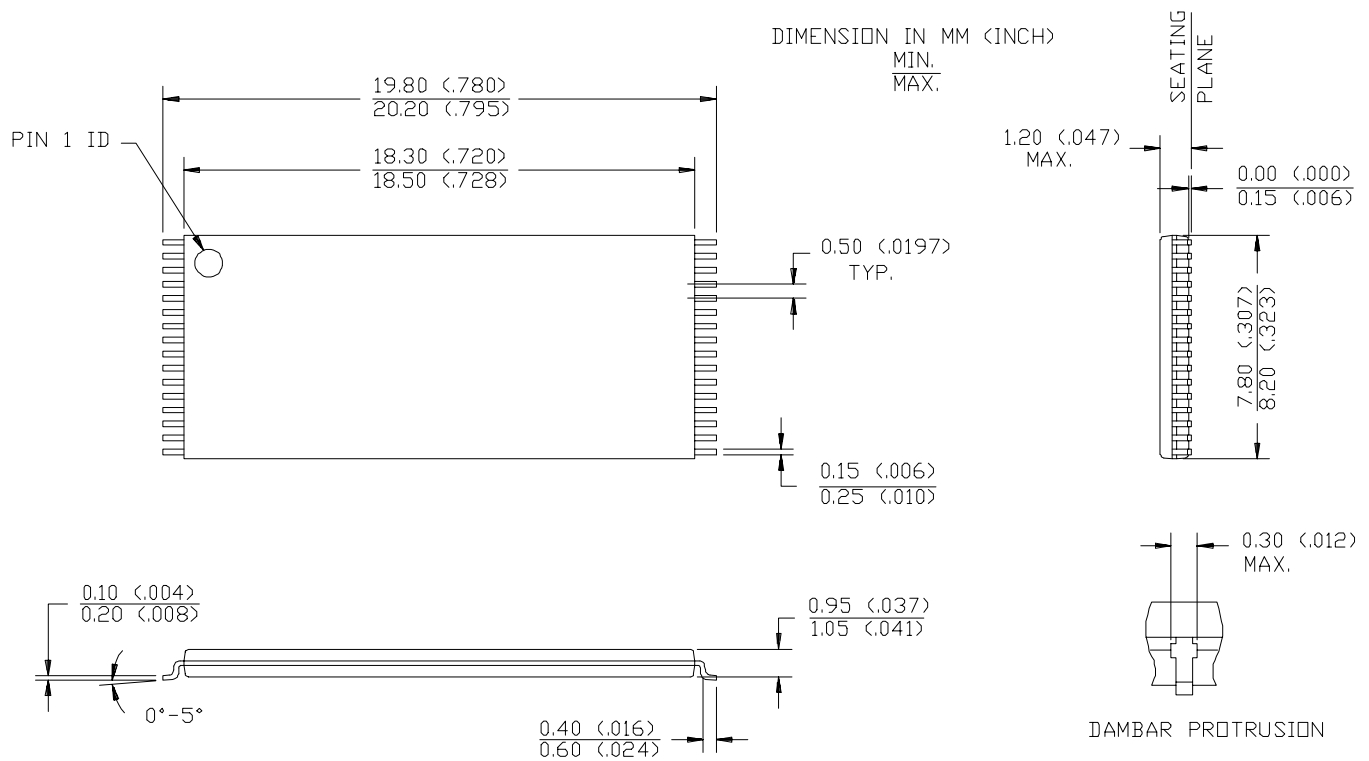
Ordering Information

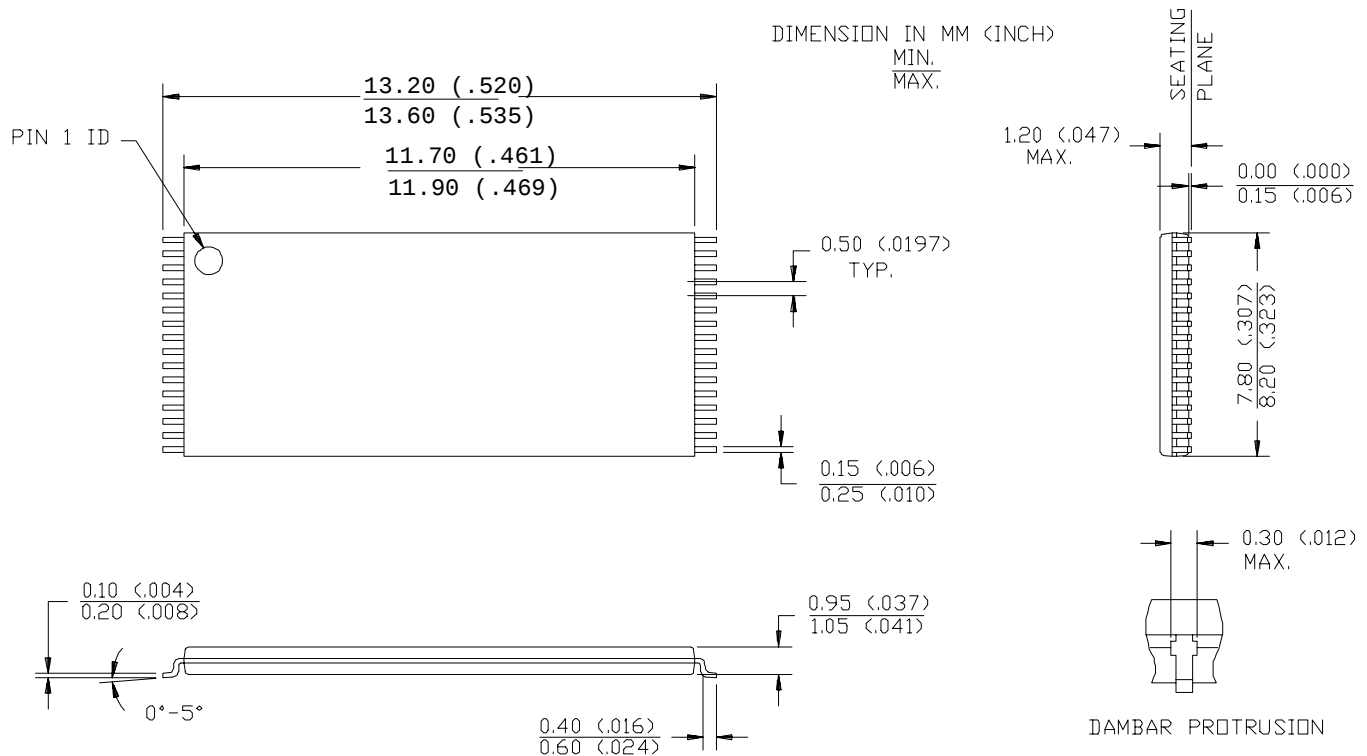
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62128VL-70SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128VLL-70SC	S34		
	CY62128VL-70ZC	Z32	32-Lead TSOP Type 1	
	CY62128VLL-70ZC	Z32		
	CY62128VL-70ZAC	ZA32	32-Lead STSOP Type 1	
	CY62128VLL-70ZAC	ZA32		
	CY62128VL-70ZRC	ZR32	32-Lead Reverse TSOP 1	
	CY62128VLL-70ZRC	ZR32		
70	CY62128VL-70SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128VLL-70SI	S34		
	CY62128VL-70ZI	Z32	32-Lead TSOP Type 1	
	CY62128VLL-70ZI	Z32		
	CY62128VL-70ZAI	ZA32	32-Lead STSOP Type 1	
	CY62128VLL-70ZAI	ZA32		
	CY62128VL-70ZRI	ZR32	32-Lead Reverse TSOP 1	
	CY62128VLL-70ZRI	ZR32		
100	CY62128V25L-100SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128V25LL-100SC	S34		
	CY62128V25L-100ZC	Z32	32-Lead TSOP Type 1	
	CY62128V25LL-100ZC	Z32		
	CY62128V25L-100ZAC	ZA32	32-Lead STSOP Type 1	
	CY62128V25LL-100ZAC	ZA32		
	CY62128V25L-100ZRC	ZR32	32-Lead Reverse TSOP 1	
	CY62128V25LL-100ZRC	ZR32		
100	CY62128V25L-100SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128V25LL-100SI	S34		
	CY62128V25L-100ZI	Z32	32-Lead TSOP Type 1	
	CY62128V25LL-100ZI	Z32		
	CY62128V25L-100ZAI	ZA32	32-Lead STSOP Type 1	
	CY62128V25LL-100ZAI	ZA32		
	CY62128V25L-100ZRI	ZR32	32-Lead Reverse TSOP 1	
	CY62128V25LL-100ZRI	ZR32		
200	CY62128V18L-200SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128V18LL-200SC	S34		
	CY62128V18L-200ZC	Z32	32-Lead TSOP Type 1	
	CY62128V18LL-200ZC	Z32		
	CY62128V18L-200ZAC	ZA32	32-Lead STSOP Type 1	
	CY62128V18LL-200ZAC	ZA32		
	CY62128V18L-200ZRC	ZR32	32-Lead Reverse TSOP 1	
	CY62128V18LL-200ZRC	ZR32		

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
200	CY62128V18L-200SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128V18LL-200SI	S34		
	CY62128V18L-200ZI	Z32	32-Lead TSOP Type 1	
	CY62128V18LL-200ZI	Z32		
	CY62128V18L-200ZAI	ZA32	32-Lead STSOP Type 1	
	CY62128V18LL-200ZAI	ZA32		
	CY62128V18L-200ZRI	ZR32	32-Lead Reverse TSOP 1	
	CY62128V18LL-200ZRI	ZR32		

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Package Diagrams
32-Lead (450 Mil) Molded SOIC S32

32-Lead Thin Small Outline Package Z32


Package Diagrams (continued)
32-Lead Shrink Thin Small Outline Package ZA32

32-Lead Reverse Thin Small Outline Package ZR32
