



# ICs for Consumer Electronics

Controller for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction

TDA 16846/TDA 16847

Data Sheet 2000-01-14

<b>TDA 16846/TDA 16847</b>		
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# Controller for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction

**TDA 16846**  
**TDA 16847**

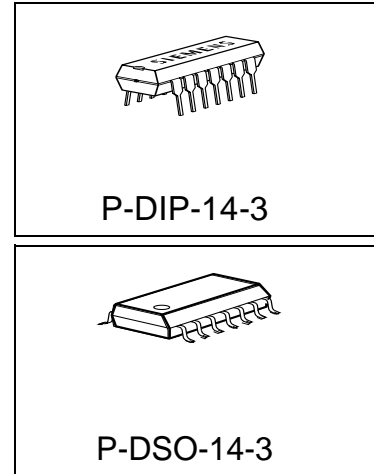
**Preliminary Data**

**Bipolar IC**

## 1 Overview

### 1.1 Features

- Line Current Consumption with PFC
- Low Power Consumption
- Stable and Adjustable Standby Frequency
- Very Low Start-up Current
- Soft-Start for Quiet Start-up
- Free usable Fault Comparators
- Synchronization and Fixed Frequency Facility
- Over- and Undervoltage Lockout
- Switch Off at Mains Undervoltage
- Temporary high power circuit (only TDA 16847)
- Mains Voltage Dependent Fold Back Point Correction
- Continuous Frequency Reduction with Decreasing Load
- Adjustable and Voltage Dependent Ringing Suppression Time



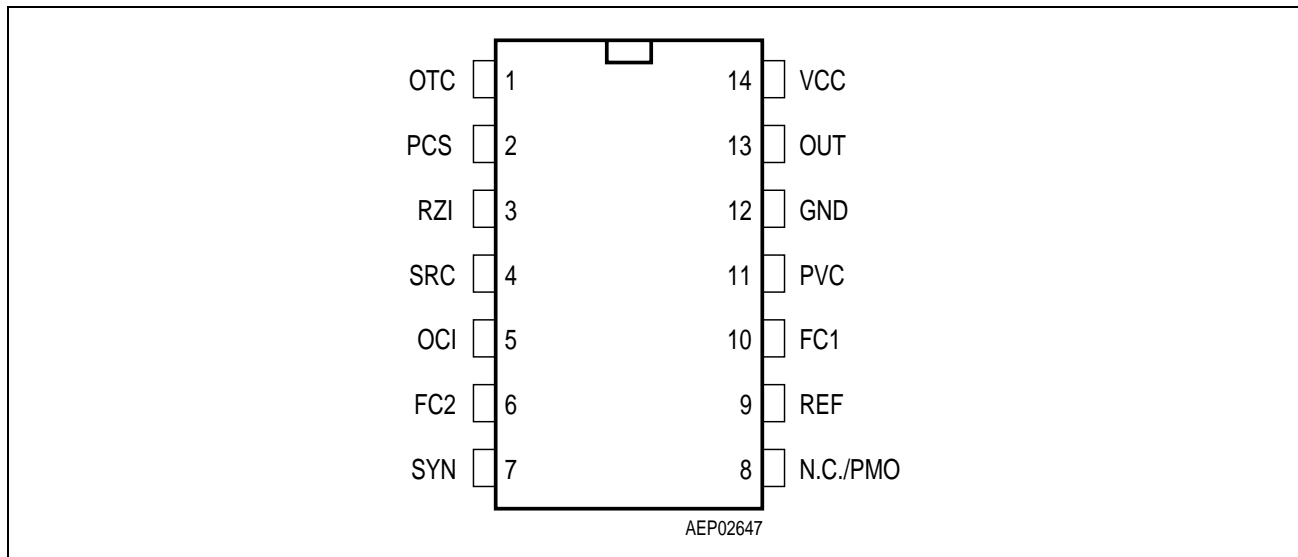
Type	Ordering Code	Package
TDA 16846	Q67000-A9377	P-DIP-14-3
TDA 16847	Q67000-A9378	P-DIP-14-3
TDA 16846G	Q67006-A9430	P-DSO-14-3
TDA 16847G	Q67006-A9412	P-DSO-14-3

### 1.2 Description

The TDA 16846 is optimized to control free running or fixed frequency flyback converters with or without Power Factor Correction (Current Pump). To provide low power consumption at light loads, this device reduces the switching frequency continuously with load, towards an adjustable minimum (e. g. 20 kHz in standby mode). Additionally, the start up current is very low. To avoid switching stresses of the power devices, the power transistor is always switched on at minimum voltage. A special circuit is implemented to avoid jitter. The device has several protection functions:  $V_{CC}$  over- and undervoltage, mains undervoltage, current limiting and 2 free usable fault comparators. Regulation can be done by using the internal error amplifier or an opto coupler feedback (additional input). The output driver is ideally suited for driving a power MOSFET, but it can also be used for a bipolar transistor. Fixed frequency and synchronized operation are also possible.

The TDA 16846 is suited for TV-, VCR- sets and SAT receivers. It also can be good used in PC monitors.

The TDA 16847 is identical with TDA 16846 but has an additional power measurement output (pin 8) which can be used for a Temporary High Power Circuit.



**Figure 1** Pin Configuration (top view)

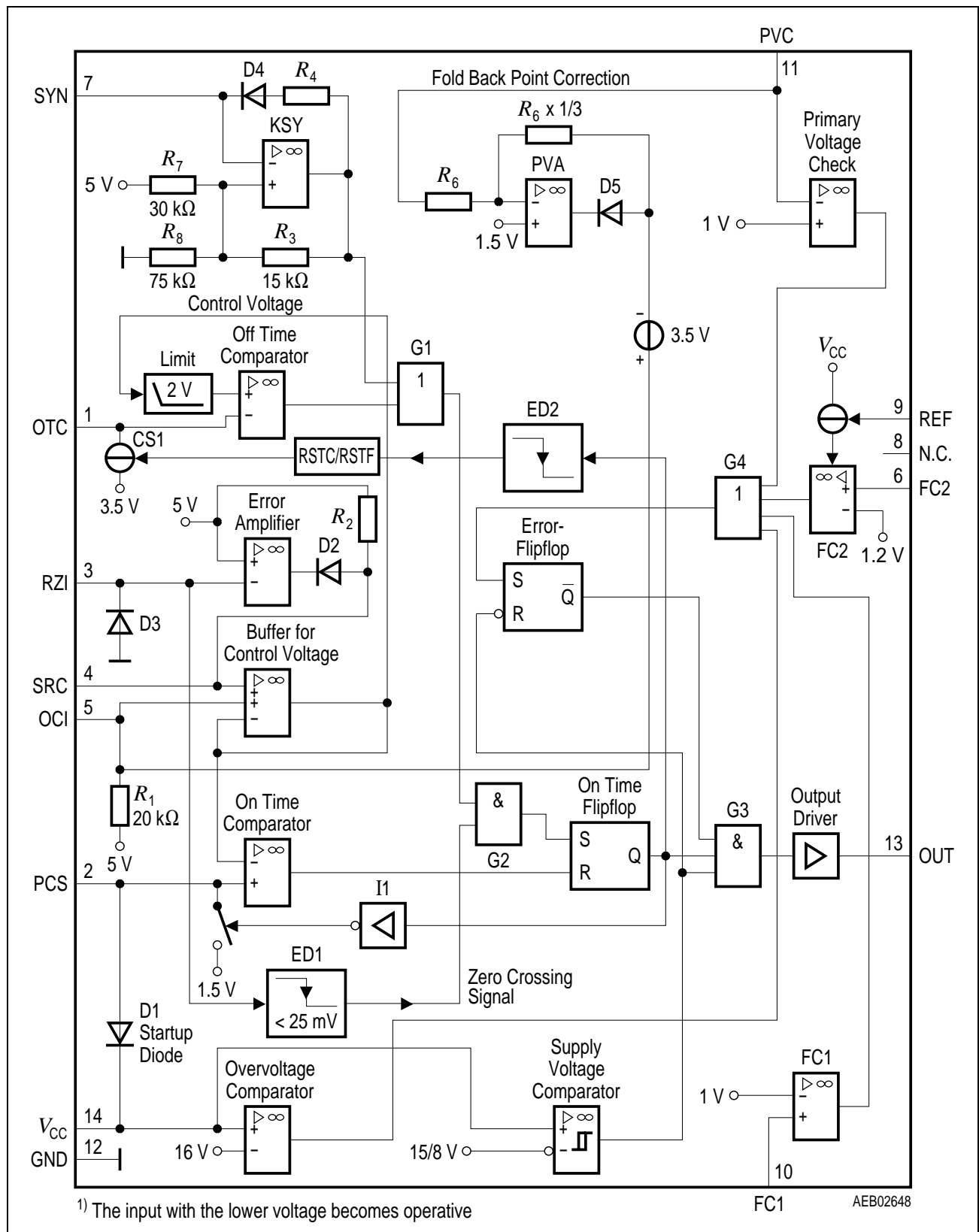
### 1.3 Pin Definitions and Functions

Pin	Symbol	Function
1	OTC	Off Time Circuit
2	PCS	Primary Current Simulation
3	RZI	Regulation and Zero Crossing Input
4	SRC	Soft-Start and Regulation Capacitor
5	OCI	Opto Coupler Input
6	FC2	Fault Comparator 2
7	SYN	Synchronization Input
8	N.C./PMO	Not Connected (TDA 16846)/PMO (TDA 16847)
9	REF	Reference Voltage and Current
10	FC1	Fault Comparator 1
11	PVC	Primary Voltage Check
12	GND	Ground
13	OUT	Output
14	VCC	Supply Voltage

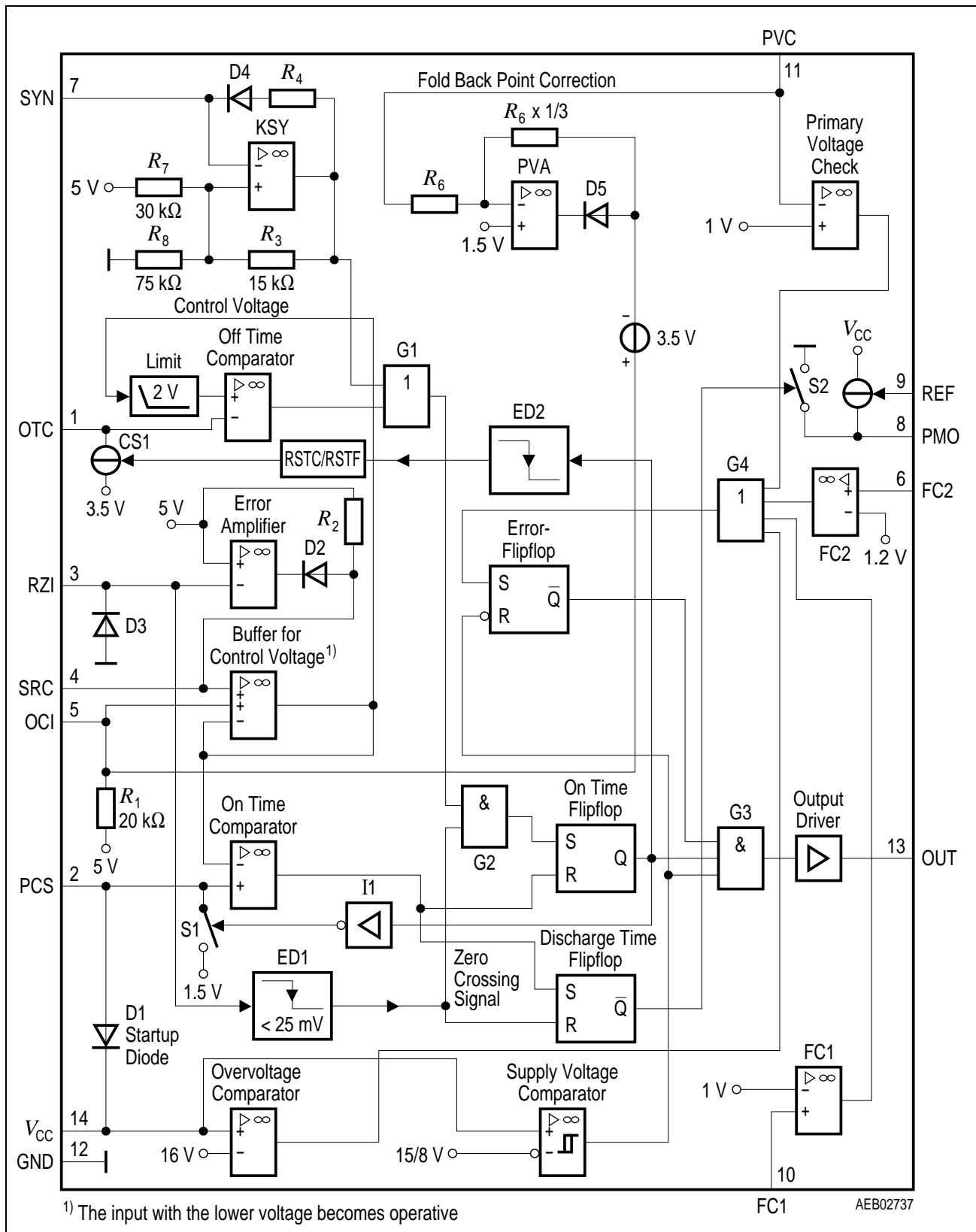
## 1.4 Short Description of the Pin Functions

Pin	Function
1	A parallel RC-circuit between this pin and ground determines the ringing suppression time and the standby-frequency.
2	A capacitor between this pin and ground and a resistor between this pin and the positive terminal of the primary elcap quantifies the max. possible output power of the SMPS.
3	This is the input of the error amplifier and the zero crossing input. The output of a voltage divider between the control winding and ground is connected to this input. If the pulses at pin 3 exceed a 5 V threshold, the control voltage at pin 4 is lowered.
4	This is the pin for the control voltage. A capacitor has to be connected between this pin and ground. The value of this capacitor determines the duration of the softstart and the speed of the control.
5	If an opto coupler for the control is used, it's output has to be connected between this pin and ground. The voltage divider at pin 3 has then to be changed, so that the pulses at pin 3 are below 5 V.
6	Fault comparator 2: If a voltage > 1.2 V is applied to this pin, the SMPS stops.
7	If fixed frequency mode is wanted, a parallel RC circuit has to be connected between this pin and ground. The RC-value determines the frequency. If synchronized mode is wanted, sync pulses have to be fed into this pin.
8	Not connected (TDA 16846). / This is the power measurement output of the Temporary High Power Circuit. A capacitor and a RC-circuit has to be connected between this pin and ground (TDA 16847).
9	Output for reference voltage (5 V). With a resistor between this pin and ground the fault comparator 2 (pin 6) is enabled.
10	Fault comparator 1: If a voltage > 1 V is applied to this pin, the SMPS stops.
11	This is the input of the primary voltage check. The voltage at the anode of the primary elcap has to be fed to this pin via a voltage divider. If the voltage of this pin falls below 1 V, the SMPS is switched off. A second function of this pin is the primary voltage dependent fold back point correction (only active in free running mode).
12	Common ground.
13	Output signal. This pin has to be connected across a serial resistor with the gate of the power transistor.
14	Connection for supply voltage and startup capacitor. After startup the supply voltage is produced by the control winding of the transformer and rectified by an external diode.

## 1.5 Block Diagrams



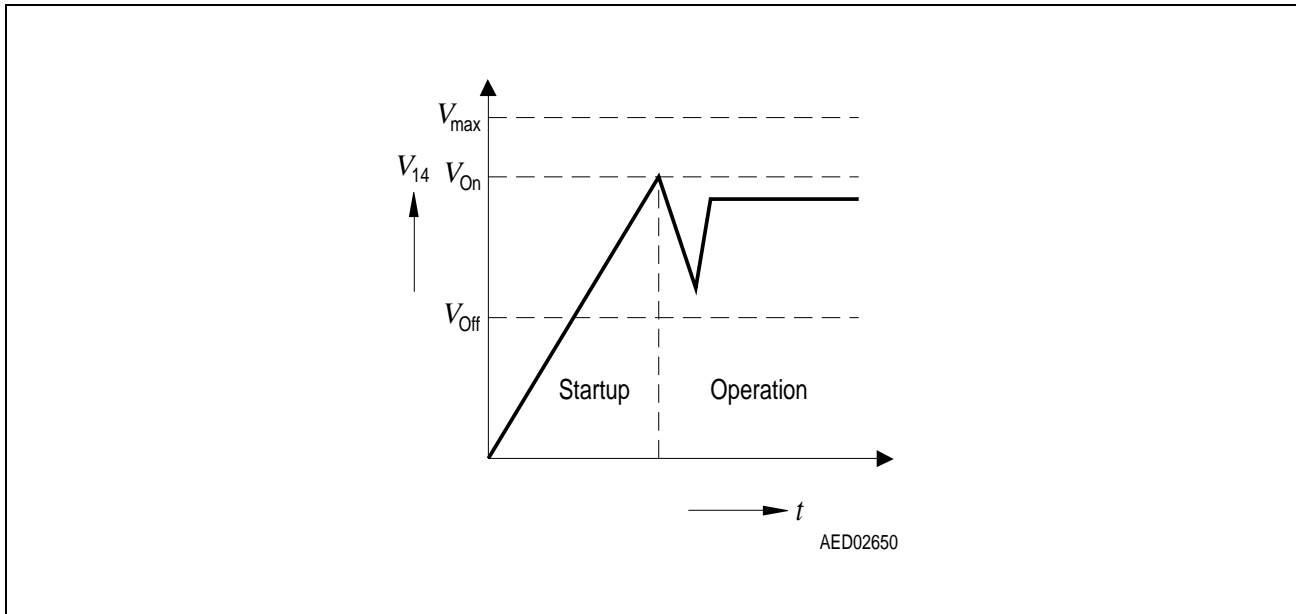
**Figure 2 TDA 16846**



**Figure 3 TDA 16847**







**Figure 5 Startup Voltage Diagram**

### Primary Current Simulation PCS (Pin 2) / Current Limiting

A voltage proportional to the current of the power transistor is generated at Pin 2 by the RC-combination  $R_2$ ,  $C_2$  (**Figure 4**). The voltage at Pin 2 is forced to 1.5 V when the power transistor is switched off and during its switch on time  $C_2$  is charged by  $R_2$  from the rectified mains. The relation of  $V_2$  and the current in the power transistor ( $I_{\text{primary}}$ ) is

$$V_2 = 1,5 \text{ V} + \frac{L_{\text{primary}} \times I_{\text{primary}}}{R_2 \times C_2}$$

$L_{\text{primary}}$ : Primary inductance of the transformer

The voltage  $V_2$  is applied to one input of the On Time Comparator ONTC (see **Figure 2**). The other input is the control voltage. If  $V_2$  exceeds the control voltage, the driver switches off (current limiting). The maximum value of the control voltage is the internal reference voltage 5 V, so the maximum current in the power transistor ( $I_{\text{Mprimary}}$ ) is

$$I_{\text{Mprimary}} = \frac{3,5 \text{ V} \times R_2 \times C_2}{L_{\text{primary}}}$$

The control voltage can be reduced by either the Error Amplifier EA (current mode regulation), or by an opto coupler at Pin 5 (regulation with opto coupler isolation) or by the voltage  $V_{11}$  at Pin 11 (Fold Back Point Correction).

### Fold Back Point Correction PVC (Pin 11)

$V_{11}$  is deviated by a voltage divider from the rectified mains and reduces the limit of the possible current maximum in the power transistor if the mains voltage increases. I.e. this limit is independent of the mains (only active in free running mode). The maximum current ( $I_{Mprimary}$ ) depending on the voltage  $V_{11}$  at Pin 11 is

$$I_{Mprimary} = \frac{(4 \text{ V} - V_{11}/3) \times R_2 \times C_2}{L_{primary}}$$

### Off-Time Circuit OTC (Pin 1)

**Figure 6** shows the Off-Time Circuit which determines the load dependent frequency course. When the driver switches off (**Figure 7**) the capacitor  $C_1$  is charged by current  $I_1$  (approx. 1 mA) until the capacitor's voltage reaches 3.5 V. The charge time TC1 is

$$TC1 \approx \frac{C_1 \times 1,5 \text{ V}}{1 \text{ mA}}$$

For proper operation of the special internal anti jitter circuit, TC1 should have the same value as the resonance time "TR" of the power circuit (**Figure 7**). After charging  $C_1$  up to 3.5 V the current source is disconnected and  $C_1$  is discharged by resistor  $R_1$ . The voltage  $V_1$  at Pin 1 is applied to the Off-Time Comparator (OFTC). The other input of OFTC is the control voltage. The value of the control voltage at the input of OFTC is limited to a minimum of 2 V (for stable frequency at very light load). The On-Time Flip Flop (ONTF) is set, if the output of OFTC is high <sup>1)</sup> and the voltage  $V_3$  at Pin 3 falls below 25 mV (zero crossing signal is high). This ensures switching on of the power transistor at minimum voltage. If no zero crossing signal is coming into pin 3, the power transistor is switched on after an additional delay until  $V_1$  falls below 1.5 V (see **Figure 6**, OFTCD). As long as  $V_1$  is higher than the limited control voltage, ONTF is disabled to suppress wrong zero crossings of  $V_3$ , due to parasitic oscillations from the transformer after switch-off. The discharge time of  $C_1$  is a function of the control voltage.

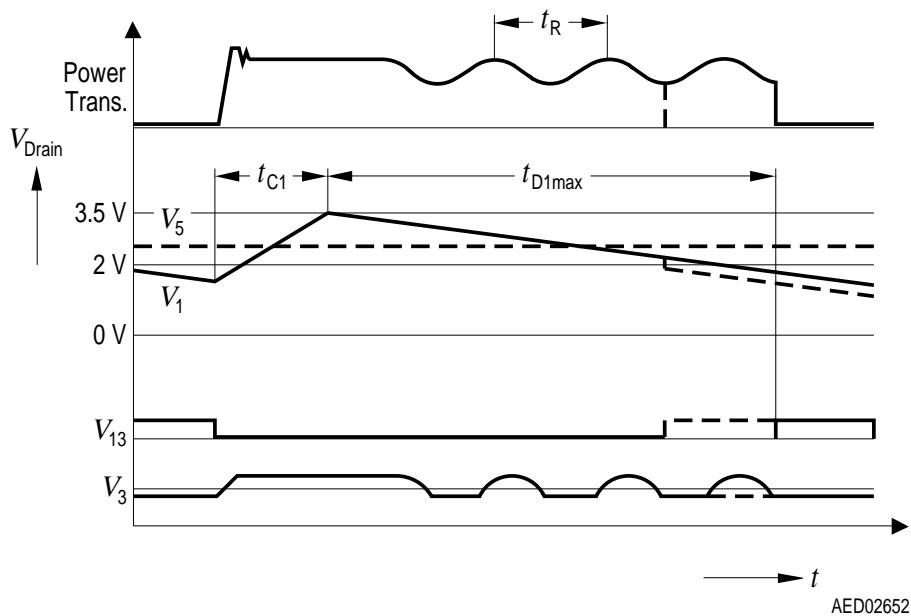
<sup>1)</sup> i.e.  $V_1$  is less than the limited control voltage.

Control Voltage	Output Power	Off-time TD1
1.5 - 2 V	Low	Constant (TD1 <sub>MAX.</sub> ), const. frequency stand by
2 - 3.5 V	Medium	Decreasing
3.5 - 5 V	High	Free running, switch-on at first minimum

If the control voltage is below 2 V (at low output power) the "off-time" is maximum and constant

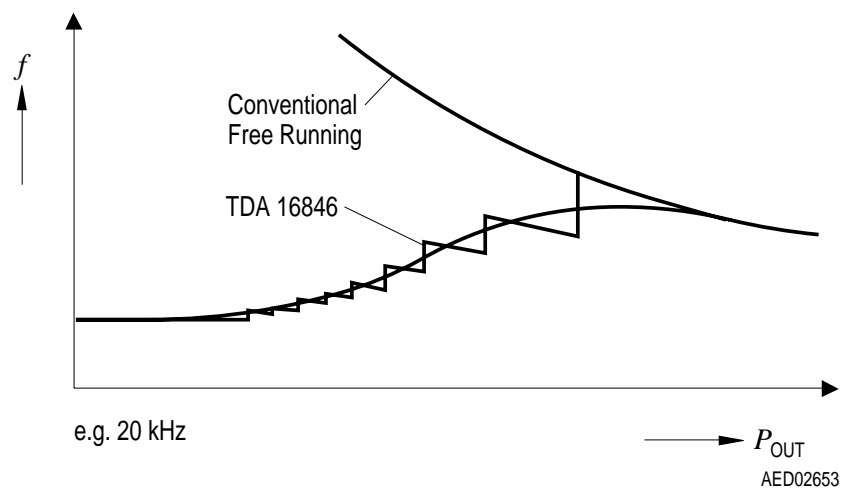
$$TD1_{max} \approx 0,47 \times R_1 \times C_1$$





**Figure 7** Pulse Diagram of Off-Time-Circuit

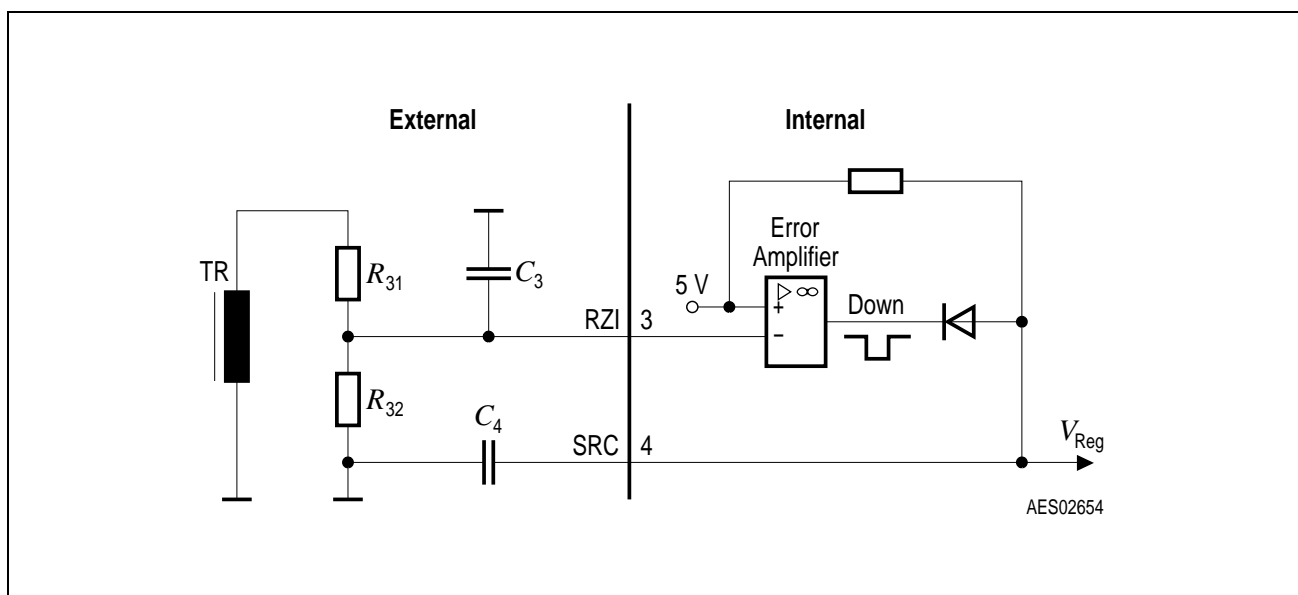
**Figure 8** shows the converters switching frequency as a function of the output power.



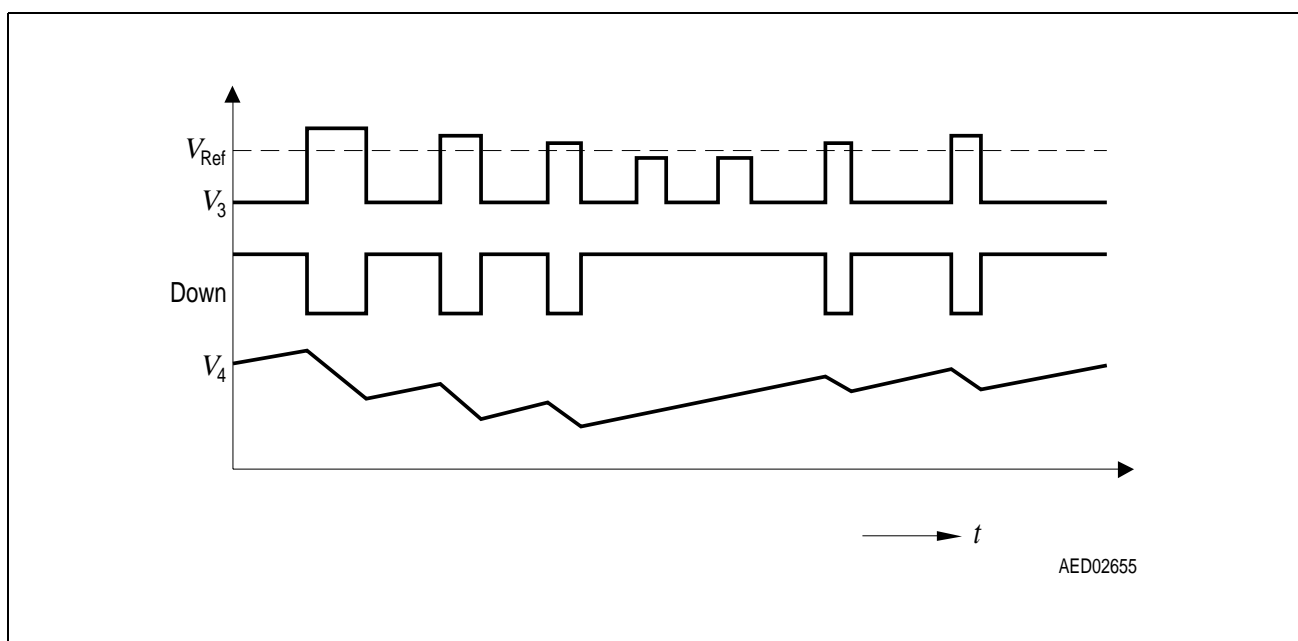
**Figure 8** Load Dependant Frequency Course

### Error Amplifier EA / Soft-Start (Pin 3, Pin 4)

**Figure 9** shows the simplified Error Amplifier circuit. The positive input of the Error Amplifier (EA) is the reference voltage 5 V. The negative input is the pulsed output voltage from the auxiliary winding, divided by  $R_{31}$  and  $R_{32}$ . The capacitor  $C_3$  is dimensioned only for delaying zero crossings and smoothing the first spike after switch-off. Smoothing of the regulation voltage is done with the soft start capacitor  $C_4$  at Pin 4. During start up  $C_4$  is charged with a current of approx. 2  $\mu$ A (Soft Start). **Figure 10** shows the voltage diagrams of the Error Amplifier circuit.



**Figure 9** Error Amplifier



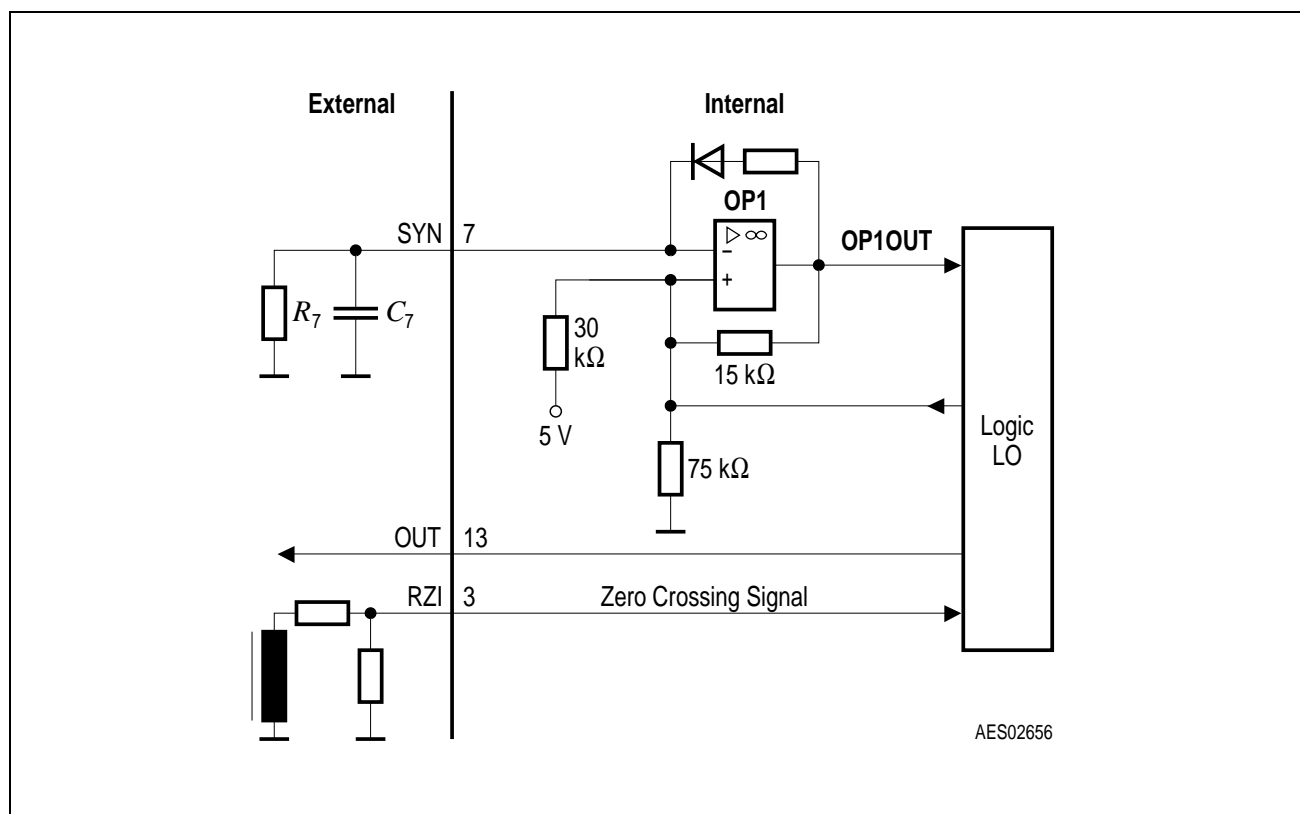
**Figure 10** Regulation Pulse Diagram

## Fixed Frequency and Synchronization Circuit SYN (Pin 7)

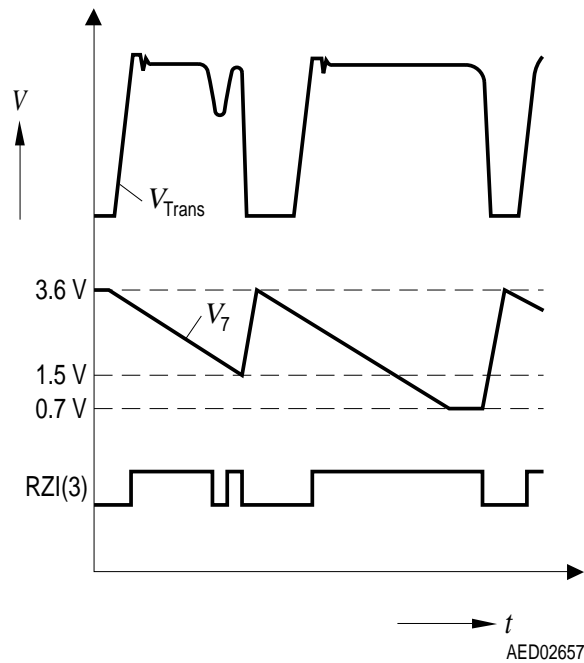
**Figure 11** shows the Fixed Frequency and Synchronization Circuit. The circuit is disabled when Pin 7 is not connected. With  $R_7$  and  $C_7$  at Pin 7 the circuit is working.  $C_7$  is charged fast by approx. 1 mA and discharged slowly by  $R_7$  (**Figure 11**). The power transistor is switched on at beginning of the charge phase. The switching frequency is (charge time ignored)

$$f \approx \frac{1,18}{R_7 \times C_7}$$

When the oscillator circuit is working the Fold Back Point Correction is disabled (not necessary in fixed frequency mode). “Switch on” is only possible when a “zero crossing” has occurred at Pin 3, otherwise “switch-on” will be delayed (**Figure 12**).

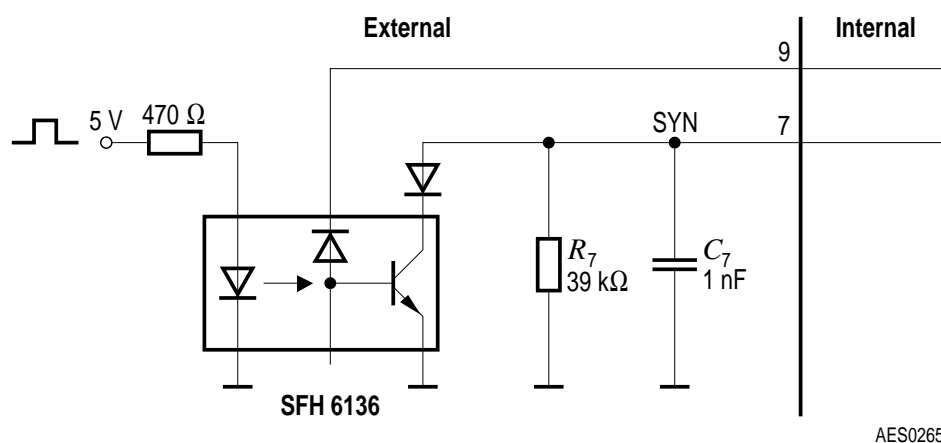


**Figure 11 Synchronization and Fixed Frequency Circuit**



**Figure 12 Pulse Diagram for Fixed Frequency Circuit**

Synchronization mode is also possible. The synchronization frequency must be higher than the oscillator frequency.



**Figure 13 Ext. Synchronization Circuit**

### **3 Protection Functions**

The chip has several protection functions:

#### **Current Limiting**

See “Primary Current Simulation PCS (Pin 2) / Current Limiting” and “Fold Back Point Correction PVC (Pin 11)”.

#### **Over- and Undervoltage Lockout OV/SVC (Pin 14)**

When  $V_{14}$  at Pin 14 exceeds 16 V, e. g. due to a fault in the regulation circuit, the Error Flip Flop ERR is set and the output driver is shut-down. When  $V_{14}$  goes below the lower SVC threshold, ERR is reset and the driver output (Pin 13) and the soft-start (Pin 4) are shut down and actively held low.

#### **Primary Voltage Check PVC (Pin 11)**

When the voltage  $V_{11}$  at Pin 11 goes below 1 V the Error Flip Flop (ERR) is set. E.g. a voltage divider from the rectified mains at Pin 11 prevents from high input currents at too low input voltage.

#### **Free Usable Fault Comparator FC1 (Pin 10)**

When the voltage at Pin 10 exceeds 1 V, the Error Flip Flop (ERR) is set. This can be used e. g. for mains overvoltage shutdown.

#### **Free Usable Fault Comparator FC2 (Pin 6)**

When the voltage at Pin 6 exceeds 1.2 V, the Error Flip Flop (ERR) is set. A resistor between Pin 9 (REF) and ground is necessary to enable this fault comparator.

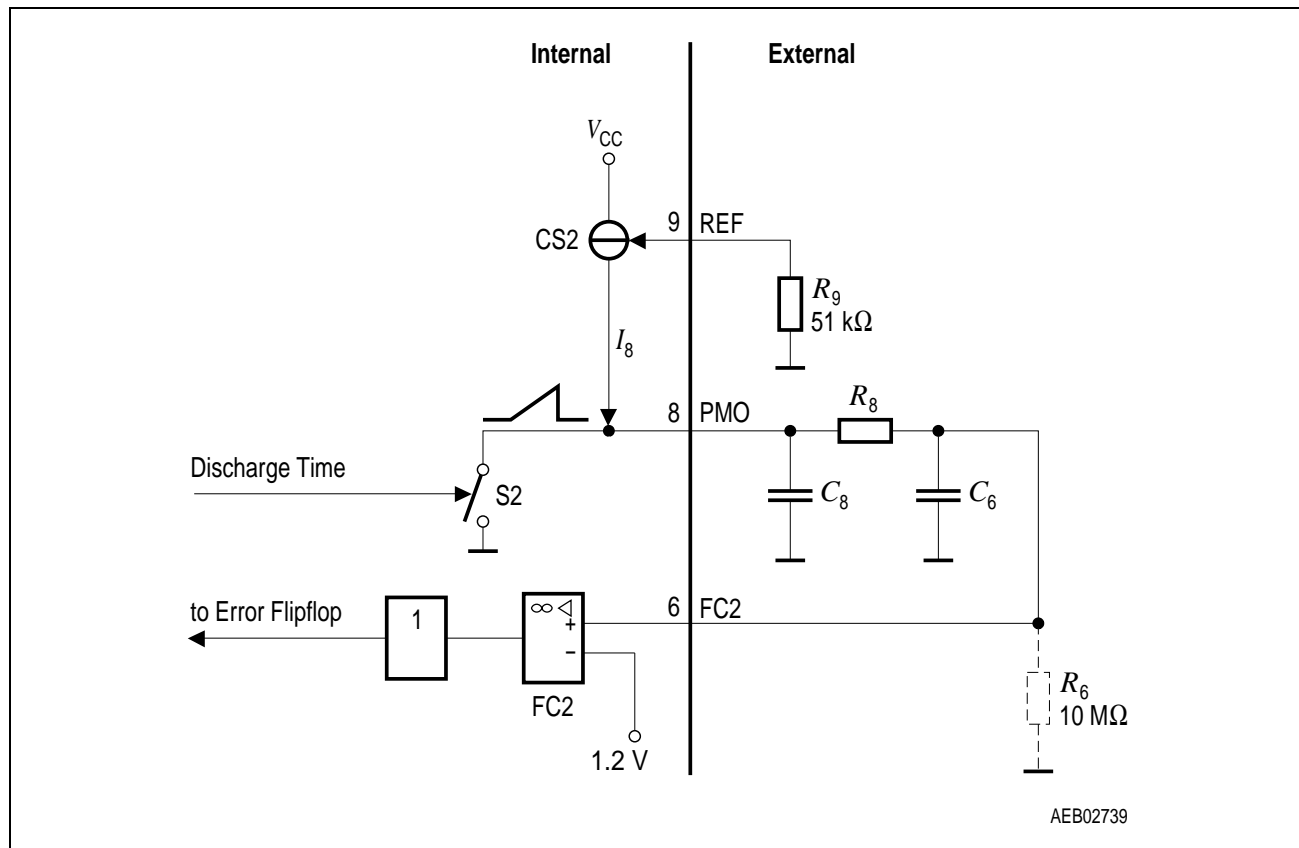
#### **Voltage dependent Ringing Suppression Time**

During start-up and short-circuit operation, the output voltage of the converter is low and parasitic zero crossings are applied for a longer time at Pin 3. Therefore the Ringing Suppression Time TC1 (see “Off-Time Circuit OTC (Pin 1)”) is made longer with factor 2.5 at low output voltage. To ensure start-up of the circuit, the value of resistor  $R_1$  (Pin 1, **Figure 6**) must be higher than 20 k $\Omega$ .



## 4 Temporary High Power Circuit FC2, PMO, REF (Pin 6, 8, 9, TDA 16847)

Figure 14 shows the Temporary High Power Circuit:



**Figure 14**

The Temporary High Power Circuit (THPC) consists of two parts:

First a power measurement circuit is implemented: The capacitor  $C_8$  at Pin 8 is charged with a constant current  $I_8$  during the discharge time of the flyback transformer and connected to ground the other time. So the average of the sawtooth voltage  $V_8$  at Pin 8 is proportional to the converters output power (at constant output voltages). The charge current  $I_8$  for  $C_8$  is dimensioned by the resistor  $R_9$  at Pin 9:

$$I_8 = 5 \text{ V} / R_9$$

Second a High Power Shutdown Comparator (FC2) is implemented: When the voltage  $V_6$  at Pin 6 exceeds 1.2 V the Error Flip Flop (ERR) is set. The output voltage of the power measurement circuit (Pin 8) is smoothed by  $R_8/C_6$  and applied to the “high power shutdown” input at Pin 6. The relation between this voltage  $V_6$  and the output power of the converter  $P$  is approximately:

$$V_6 \approx (P \times L_{\text{Secondary}} \times 5 \text{ V}) / (V_{\text{OUT}}^2 \times C_8 \times R_9)$$

$L_{\text{Secondary}}$ : The transformers secondary inductance

$V_{\text{OUT}}$ : The converters output voltage

So the time constant of  $R_9/C_8$  for a certain high power shutdown level  $P_{\text{SD}}$  is:

$$R_9 \times C_8 \approx (P_{\text{SD}} \times L_{\text{Secondary}} \times 4.2) / V_{\text{OUT}}^2$$

The converters high power shutdown level can be dimensioned lower (by  $R_9$ ,  $C_8$ ) than the current limit level (see “current limiting”). So because of the delay  $R_8/C_6$ , the converter can deliver maximum output power (current limit level) for a certain time (e. g. for power pulses like motor start current) and a power below the high power shutdown level for unlimited time. This has the advantage that the thermal dimensioning of the power devices is only needed for the lower power level. Once the voltage  $V_6$  exceeds 1.2 V there are no more charge or discharge actions at Pin 8. The voltage  $V_6$  remains high due to the bias current out of HPC and the converter remains switched-off. Reset can be done by either plug-off the supply from the mains or with a high value resistor  $R_6$  (**Figure 14**).  $R_6$  causes a reset every view seconds. When Pin 9 is not connected or gets too less current the temporary high power circuit is disabled.

## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

All voltages listed are referenced to ground (0 V,  $V_{SS}$ ) except where noted.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply Voltage at Pin 14	$V_{CC}$	– 0.3	17	V	–
Voltage at Pin 1, 4, 5, 6, 7, 9, 10	–	– 0.3	6	V	–
Voltage at Pin 2, 8, 11	–	– 0.3	17	V	–
Voltage at Pin 3	RZI		6	V	
Current into Pin 3		– 10		mA	$V_3 < -0.3 \text{ V}$
Current into Pin 9	REF	– 1	–	mA	–
Current into Pin 13	OUT		100	mA	$V_{13} > V_{CC}$
		– 100		mA	$V_{13} < 0 \text{ V}$
ESD Protection	–	–	2	kV	MIL STD 883C method 3015.6, 100 pF, 1500 $\Omega$
Storage Temperature	$T_{stg}$	– 65	125	°C	–
Operating Junction Temperature	$T_J$	– 25	125	°C	–
Thermal Resistance Junction-Ambient	$R_{thJA}$	–	110	K/W	P-DIP-14-3
Soldering Temperature	–	–	260	°C	–
Soldering Time	–	–	10	s	–

*Note: Stresses above those listed here may cause permanent damage to the device.  
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## 5.2 Characteristics

Unless otherwise stated,  $-25\text{ }^{\circ}\text{C} < T_j < 125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Start-Up Circuit

Supply current, OFF	$I_{14}$	–	40	100	$\mu\text{A}$	$0 < V_{CC} < V_{14\text{ ON}}$
Supply current, ON	$I_{14}$	–	5	8	$\text{mA}$	Output low
Turn-ON threshold	$V_{14\text{ ON}}$	14.5	15	15.5	$\text{V}$	–
Turn-OFF threshold	$V_{14\text{ OFF}}$	7.5	8	8.5	$\text{V}$	–

### Primary Current Simulation PCS (Pin 2) / Current Limiting

Basic value	$V_2$	1.45	1.5	1.55	$\text{V}$	$I_2 = 100\text{ }\mu\text{A}$
Peak value	$V_2$	4.85	5	5.15	$\text{V}$	$V_{11} = 1.2\text{ V}$
On-time	–	9.0	10.5	11.5	$\mu\text{s}$	$V_{11} = 1.2\text{ V}$ , $C_2 = 220\text{ pF}$ , $I_2 = 75\text{ }\mu\text{A}$
Bias current Pin 2	–	– 1.0	– 0.3	–	$\mu\text{A}$	–

### Fold Back Point Correction PVC (Pin 11)

Peak value	$V_2$	3.8	4.1	4.3	$\text{V}$	$V_{11} = 4.5\text{ V}$
On-time	–	6.2	7.5	8.5	$\mu\text{s}$	$V_{11} = 4.5\text{ V}$ , $C_2 = 220\text{ pF}$ , $I_2 = 75\text{ }\mu\text{A}$
Bias current Pin 11	–	– 1.0	– 0.3	–	$\mu\text{A}$	–

### Off-Time Circuit OTC (Pin 1)

Charge current	$I_1$	0.9	1.1	1.4	$\text{mA}$	$V_3 > 3\text{ V}$
Charge current	$I_1$	0.35	0.5	0.65	$\text{mA}$	$V_3 < 2\text{ V}$
Peak value	$V_1$	3.38	3.5	3.62	$\text{V}$	–
Basic value	$V_1$	1.92	2	2.08	$\text{V}$	–

## 5.2 Characteristics (cont'd)

Unless otherwise stated,  $-25\text{ }^{\circ}\text{C} < T_j < 125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
T12 Charge time	TC1	0.85	1.0	1.3	$\mu\text{s}$	$V_3 > 3\text{ V}$ , $C_1 = 680\text{ pF}$ , $R_1 = 100\text{ k}\Omega$
T13 Charge time	TC1	1.9	2.4	3.0	$\mu\text{s}$	$V_3 < 2\text{ V}$ , $C_1 = 680\text{ pF}$ , $R_1 = 100\text{ k}\Omega$
Off-time	TD1 <sub>MAX.</sub>	65	72	80	$\mu\text{s}$	$C_1 = 680\text{ pF}$ , $R_1 = 100\text{ k}\Omega$
Bias current Pin 1	–	– 1.1	– 0.4	–	$\mu\text{A}$	–
Zero crossing threshold (Pin 3)	–	15	25	35	mV	–
Delay to switch-on	–	280	350	480	ns	–
Bias current Pin 3	–	– 2	– 1.2	–	$\mu\text{A}$	$V_3 < 25\text{ mV}$

### Error Amplifier EA (Pin 3, Pin 4)

Input threshold (Pin 3)	$V_{EATH}$	4.85	5	5.15	V	–
Bias current Pin 3	–	–	– 0.9	–	$\mu\text{A}$	$V_3 > 3\text{ V}$
Soft-start charge current (Pin 4)	–	– 2.5	– 1.8	– 1.2	$\mu\text{A}$	–

### Opto Coupler Input (Pin 5)

Input voltage range	$V_5$	0.3	–	6	V	–
Pull high resistor to $V_{REF}$	$R_1$	15	20	25	k $\Omega$	–

## 5.2 Characteristics (cont'd)

Unless otherwise stated,  $-25\text{ }^{\circ}\text{C} < T_j < 125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Fixed Frequency and Synchronization Circuit SYN (Pin 7)

Frequency	–	78	88	98	kHz	$C_7 = 470\text{ pF}$ , $R_7 = 20\text{ k}\Omega$
Charge current	$I_7$	1.0	1.3	1.6	mA	–
Upper threshold	$V_7$	3.5	3.6	3.7	V	–
Lower threshold	$V_7$	1.43	1.5	1.57	V	–
Charge time	–	0.4	0.55	0.75	$\mu\text{s}$	–
Bias current Pin 7	–	– 2.4	– 1.8	– 1.1	$\mu\text{A}$	–
Input voltage range	$V_7$	0.3	–	6	V	–

### Undervoltage Lockout SVC (Pin 14)

Threshold	$V_{14\text{ OFF}}$	7.5	8	8.5	V	–
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### Overvoltage Lockout OV (Pin 14)

Threshold	$V_{14\text{ OV}}$	15.7	16.5	17	V	–
Delta-OV- $V_{14\text{ ON}}$	–	0.5	–	–	V	–

### Primary Voltage Check PVC (Pin 11)

Threshold	$V_{11}$	0.95	1	1.06	V	–
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### Reference Voltage (Pin 9)

Voltage at Pin 9	$V_9$	4.8	5	5.15	V	$I_9 = 100\text{ }\mu\text{A}$
Current into Pin 9	$I_9$	– 200	–	0	$\mu\text{A}$	$V_{\text{EATH(Pin 3)}} -$ $V_9 < 50\text{ mV}$

## 5.2 Characteristics (cont'd)

Unless otherwise stated,  $-25\text{ }^{\circ}\text{C} < T_j < 125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Fault Comparator FC2 (Pin 6)

HPC Threshold	$V_6$	1.12	1.2	1.28	V	–
Bias Current Pin 6	–	– 1.0	– 0.3	0.1	$\mu\text{A}$	–

### Fault Comparator FC1 (Pin 10)

Threshold	$V_{10}$	0.95	1	1.06	V	–
Bias current Pin 10	–	0.48	0.9	1.2	$\mu\text{A}$	–

### Power Measurement Output PMO (Pin 8, only TDA 16847)

Charge current Pin 8	$I_8$	– 110	– 100	– 90	$\mu\text{A}$	$I_9 = -100\text{ }\mu\text{A}$
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### Output Driver OD (Pin 13)

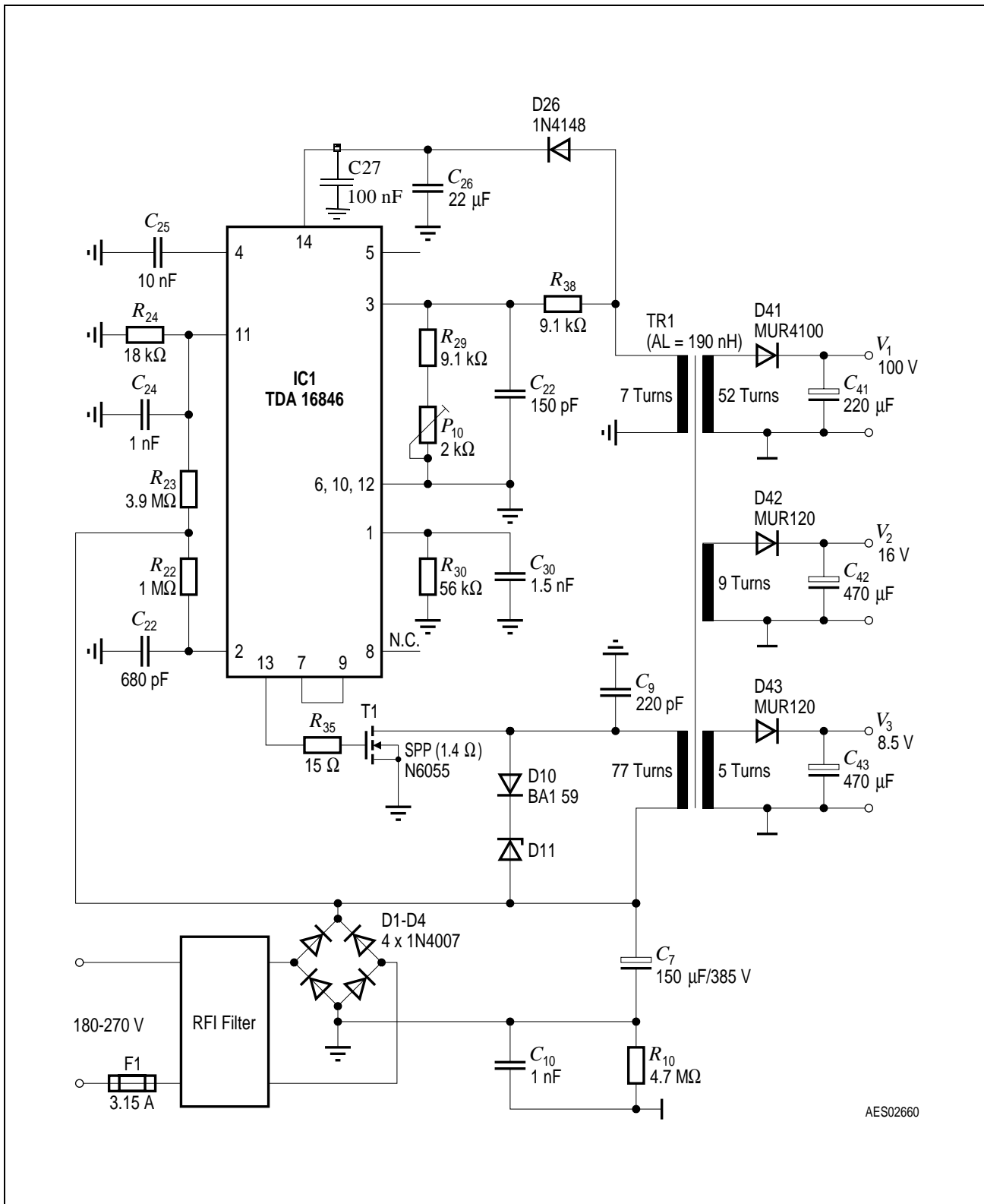
Output voltage low state	$V_{13\text{ low}}$	1.1	1.8	2.4	V	$I_{13} = 100\text{ mA}$
Output voltage high state	$V_{13\text{ high}}$	9.2	10	11	V	$I_{13} = -100\text{ mA}$
Output voltage during low supply voltage	$V_{13\text{ ac low}}$	0.8	1.8	2.5	V	$I_{13} = -10\text{ mA}$ , $V_{14}$ increasing: $0 < V_{14} < V_{14\text{ ON}}$ $V_{14}$ decreasing: $0 < V_{14} < V_{14\text{ OFF}}$
Rise time	–	70	110	180	ns	$C_{13} = 10\text{ nF}$ , $V_{13} = 2 \dots 8\text{ V}$
Fall time	–	30	50	80	ns	$C_{13} = 10\text{ nF}$ , $V_{13} = 2 \dots 8\text{ V}$

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ }^{\circ}\text{C}$  and the given supply voltage.*



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**Figure 16** Circuit Diagram for Standard Application

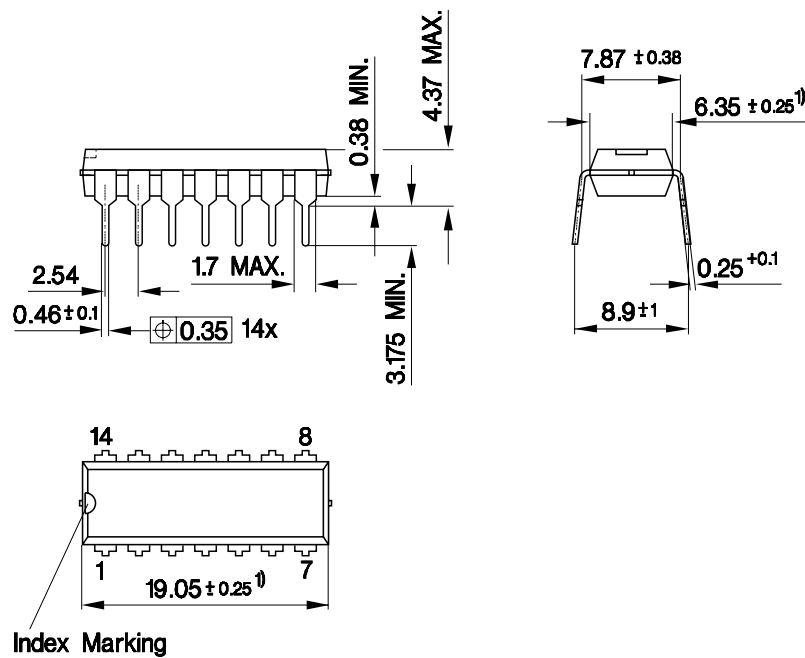


2000-01-14

## Package Outlines

### P-DIP-14-3

(Plastic Dual In-line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05584

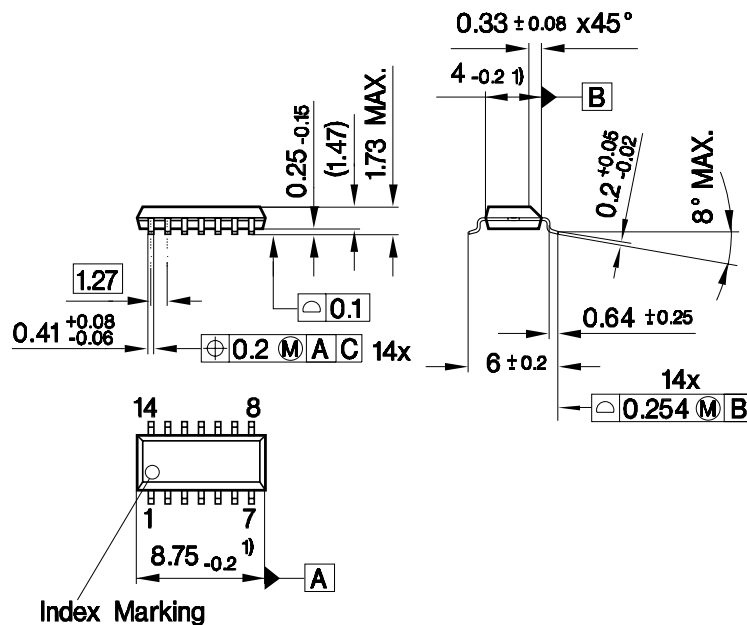
### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

## P-DSO-14-3

(Plastic Dual In-line Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

## Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm