



# 900MHz ISM-Band, 250mW Power Amplifiers with Analog or Digital Gain Control

MAX2232/MAX2233

## General Description

The MAX2232/MAX2233 low-voltage, silicon RF power amplifiers (PAs) are designed for use in the 900MHz ISM band. They operate from a single +2.7V to +5.5V supply, allowing them to be powered directly from a 3-cell NiCd or a 1-cell Lithium-Ion battery. The devices typically deliver 250mW (+24dBm) of output power at 915MHz from a single +3.6V supply, or 150mW (+22dBm) from a single +2.7V supply. At +24dBm output power, power-added efficiency (PAE) is 44%.

The MAX2232/MAX2233 provide 24dB of gain, which is adjustable over a continuous 24dB span via the analog gain-control pin of the MAX2232 or in two 10dB steps via the 2-bit programmable gain-control DAC of the MAX2233. An external capacitor sets the RF output power envelope ramp time, reducing spurious emissions during power-up and power-down by providing a gradual change in output power (MAX2232).

The MAX2232/MAX2233 feature a low-power shutdown mode, which typically draws less than 1 $\mu$ A of supply current, saving power during "idle slots" in time-division multiple-access (TDMA) systems. The  $\Delta$ VSWR of the RF input in shutdown mode relative to normal operation is 1.2:1. The devices also feature a thermal shutdown function, enabling the PA to protect itself from excessive temperature conditions that could damage the IC. A capacitor to ground limits thermal cycling by setting a thermal shutdown timeout period.

The MAX2232/MAX2233 are available in a space-saving, thermally enhanced 16-pin power-QSOP (PQSOP) package.

## Applications

- 900MHz ISM Band
- Digital Cordless Phones
- Wireless Data
- FM Analog Transmitters
- 868MHz European ISM Band

Functional Diagrams appear at end of data sheet.

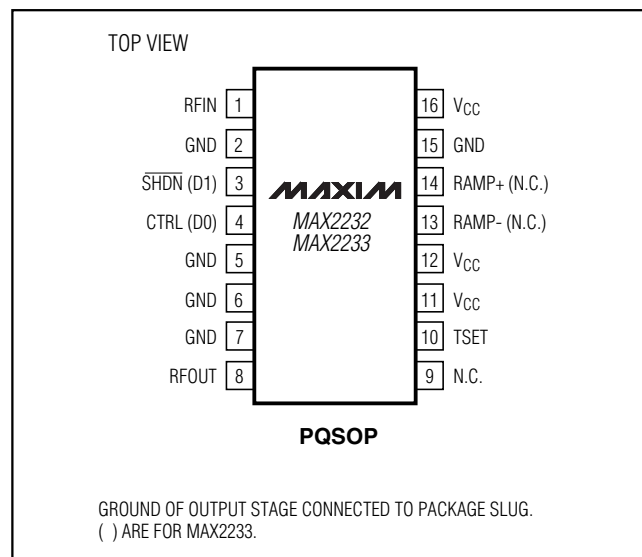
## Features

- ◆ 800MHz to 1000MHz Frequency Range
- ◆ 250mW (+24dBm) Output Power at 915MHz from +3.6V Supply
- ◆ +2.7V to +5.5V Single-Supply Operation
- ◆ 44% Power-Added Efficiency
- ◆ 24dB Power Gain
- ◆ 24dB Analog Gain-Control Range (MAX2232)
- ◆ Three Levels of Digitally Programmed Power Gain in 10dB Steps (MAX2233)
- ◆ Programmable RF Power Envelope Ramping (MAX2232)
- ◆ Thermal Shutdown
- ◆ Programmable Thermal Shutdown Timeout Period
- ◆ 0.2 $\mu$ A Low-Power Shutdown Mode
- ◆ Low  $\Delta$ VWSR in Standby and Shutdown Modes

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2232EEEE	-40°C to +85°C	16 PQSOP
MAX2233EEEE	-40°C to +85°C	16 PQSOP

## Pin Configuration



# 900MHz ISM-Band, 250mW Power Amplifiers with Analog or Digital Gain Control

## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND .....	-0.3V to +6.5V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
$\overline{\text{SHDN}}$ , CTRL, D0, D1 to GND .....	-0.3V to (V <sub>CC</sub> +0.3V)	16-Pin PQSOP (derate 80mW/°C above +70°C) .....
I <sub>RFIN</sub> .....	10mA	Operating Temperature Range .....
RFIN Power (50Ω AC-coupled source) .....	+10dBm	Storage Temperature Range .....
Output Load VSWR .....	6:1	Lead Temperature (soldering, 10s) .....

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +2.7V to +5.5V, V<sub>CTRL</sub> = +2.2V,  $\overline{\text{SHDN}}$  = V<sub>D0</sub> = V<sub>D1</sub> = +2V, T<sub>A</sub> = -40°C to +85°C. No input signal applied, unless otherwise noted. Typical values are at V<sub>CC</sub> = +3.6V and T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V <sub>CC</sub>		2.7		5.5	V
Shutdown Supply Current	I <sub>CC</sub>	V $\overline{\text{SHDN}}$ = 0.6V, V <sub>D0</sub> = V <sub>D1</sub> = 0.6V	V <sub>CC</sub> ≤ 3.6V	0.2	10	μA
			V <sub>CC</sub> = 5.5V		120	
Standby Supply Current	I <sub>CC</sub>	V <sub>CTRL</sub> ≤ 0.4V (MAX2232)		20.3	25	mA
Logic Input High	V <sub>IH</sub>	$\overline{\text{SHDN}}$ (MAX2232), D0, D1 (MAX2233)	2.0			V
Logic Input Low	V <sub>IL</sub>	$\overline{\text{SHDN}}$ (MAX2232), D0, D1 (MAX2233)			0.6	V
CTRL Input for Standby Mode	V <sub>CTRL</sub>	MAX2232			0.4	V
CTRL Input for Gain-Control Mode	V <sub>CTRL</sub>	MAX2232	0.6			V
Logic Input Current	I <sub>IH</sub>	V $\overline{\text{SHDN}}$ = 2.0V (MAX2232), V <sub>D0</sub> = V <sub>D1</sub> = 2.0V (MAX2233)	-1		10	μA
	I <sub>IL</sub>	V $\overline{\text{SHDN}}$ = GND (MAX2232), V <sub>D0</sub> = V <sub>D1</sub> = GND (MAX2233)	-1		1	
CTRL Input Current		V <sub>CTRL</sub> = GND	-1.5		1	μA
		V <sub>CTRL</sub> = 2.2V			1.5	

## AC ELECTRICAL CHARACTERISTICS

(MAX2232/MAX2233 Evaluation Kit, V<sub>CC</sub> = +3.6V, V<sub>CTRL</sub> = +2.2V,  $\overline{\text{SHDN}}$  = V<sub>CC</sub> (MAX2232), D0 = D1 = V<sub>CC</sub> (MAX2233), P<sub>RFIN</sub> = 0dBm, f<sub>RFIN</sub> = 915MHz, T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f <sub>IN</sub>	(Notes 1, 2)	902		928	MHz
Power Gain	G <sub>P</sub>			23.9		dB
Output Power	P <sub>OUT</sub>	V <sub>CC</sub> = 4.8V		25.4		dBm
		V <sub>CC</sub> = 3.6V (Note 1)	22.9	23.9	24.9	
		V <sub>CC</sub> = 3.0V		22.5		
		V <sub>CC</sub> = 2.7V		21.6		
Output Power Variation Over Temperature	ΔP <sub>OUT</sub>	T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub> (Note 1)		1.9	3.2	dB
Output Power, Medium-Power Mode	P <sub>OUT</sub>	D0 = GND, D1 = V <sub>CC</sub> (MAX2233 only)		15.8		dBm

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MAX2232/MAX2233

## AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2232/MAX2233 Evaluation Kit,  $V_{CC} = +3.6V$ ,  $V_{CTRL} = +2.2V$ ,  $\overline{SHDN} = V_{CC}$  (MAX2232),  $D0 = D1 = V_{CC}$  (MAX2233),  $P_{RFIN} = 0dBm$ ,  $f_{RFIN} = 915MHz$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power, Low-Power Mode	$P_{OUT}$	$D0 = V_{CC}$ , $D1 = GND$ (MAX2233 only)		6.5		dBm
Gain-Control Range (Note 3)	$\Delta GP$	$0.6V < V_{CTRL} < 2.2V$ (MAX2232 only)		23.6		dB
Power-Added Efficiency	PAE			44		%
Power-Added Efficiency at +21dBm Output Power	PAE	CTRL adjusted to give $P_{RFOUT} = +21dBm$ (MAX2232 only)		29		%
Supply Current, Medium-Power Mode	$I_{CC}$	$D0 = GND$ , $D1 = V_{CC}$ (MAX2233 only)		78.5		mA
Supply Current, Low-Power Mode	$I_{CC}$	$D0 = V_{CC}$ , $D1 = GND$ (MAX2233 only)		44.0		mA
Input VSWR	VSWR	$Z_{SOURCE} = 50\Omega$ (Note 1)		1.5:1		
Input VSWR Change, Shutdown Mode (Notes 1, 4)	$\Delta VSWR$			1.4:1		
Input VSWR Change, Standby Mode (Notes 1, 4)	$\Delta VSWR$	MAX2232 only		1.2:1		
Off-Isolation		$\overline{SHDN} = D0 = D1 = GND$		52		dB
		CTRL = GND (MAX2232 only)		38		
Maximum Nonharmonic Spurious Output Due to Load Mismatch		$V_{CC} = +2.7V$ to $+5.5V$ , 6:1 VSWR at any phase angle, $P_{RFIN} = +5dBm$		-60		dBc
Maximum Output Load VSWR Without Damage (Note1)		Any load phase angle, $P_{RFIN} = +5dBm$ , $T_A = T_{MIN}$ to $T_{MAX}$	6:1			
Harmonic Suppression		(Note 5)		29		dBc
Autoramping Rise Time		$C_{RAMP} = 0.22\mu F$ (Notes 1, 6) (MAX2232 only)		0.9		ms
Autoramping Fall Time		$C_{RAMP} = 0.22\mu F$ (Notes 1, 7) (MAX2232 only)		3.2		ms
Output Power Rise Time		RAMP+ = RAMP- = unconnected (Note 6)		0.4		$\mu s$
Thermal Shutdown Temperature	$T_{TH}$	$P_{RFIN} = 0dBm$ , $V_{CC} = +3.6V$		145		$^\circ C$
Thermal Shutdown Timeout Period	$t_{TH}$	$C_{TSET} = 0.22\mu F$ (Note 8)		900		ms

**Note 1:** Guaranteed by design.

**Note 2:** Operation outside this range is possible, but not characterized.

**Note 3:** Gain is monotonic with  $V_{CTRL}$ .

**Note 4:** Input VSWR relative to input impedance in operating mode.

**Note 5:** Harmonics measured on evaluation kit, which provides some harmonic attenuation in addition to the rejection provided by the IC. The combined suppression is specified.

**Note 6:** Time measured from  $\overline{SHDN}$  (MAX2232) low-to-high transition to when output power is within 1dB of final value. Includes effects of 1% tolerance capacitor.

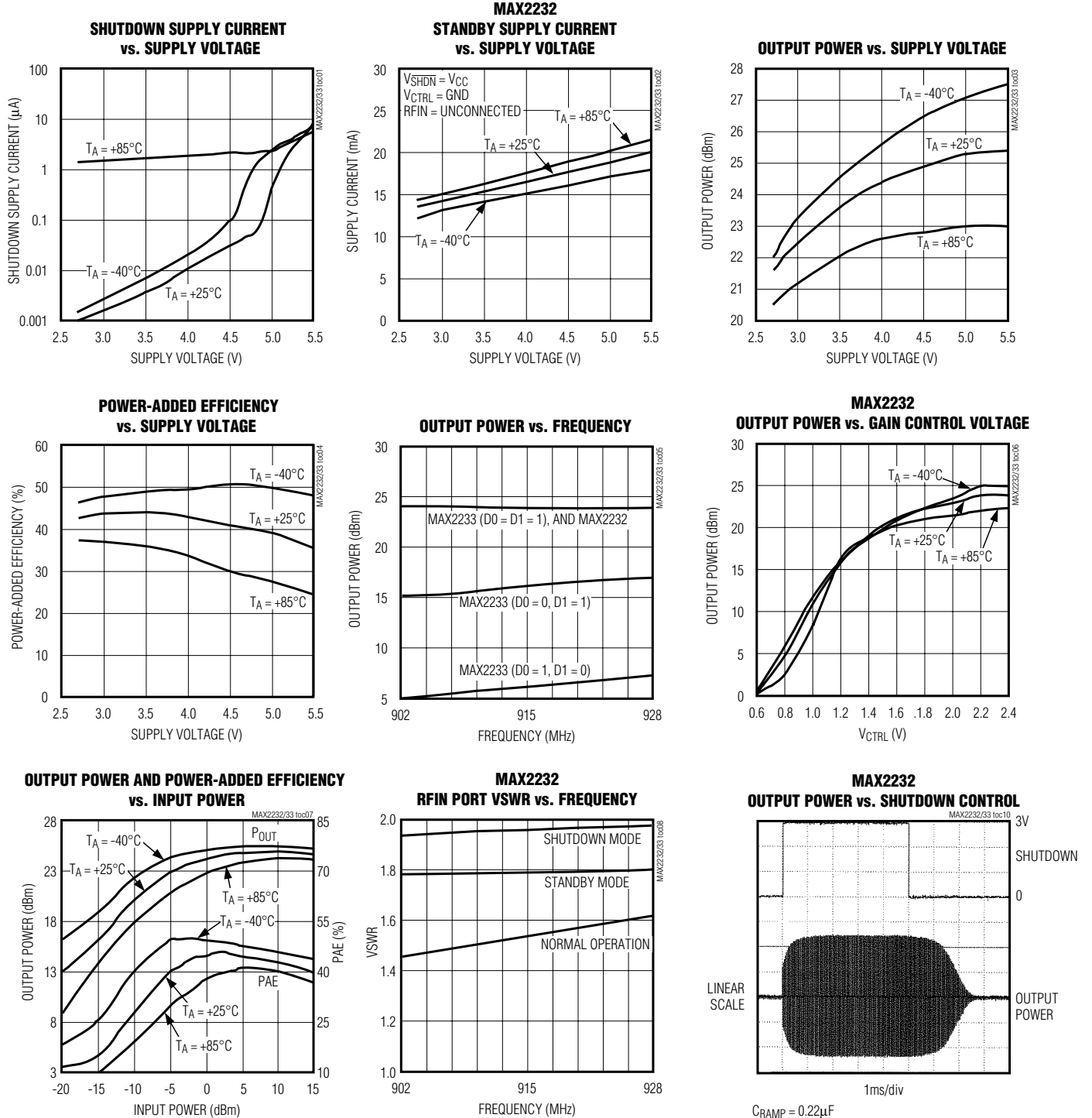
**Note 7:** Time measured from  $\overline{SHDN}$  (MAX2232) high-to-low transition to when output power is -20dB of final value. Includes effects of 1% tolerance capacitors.

**Note 8:** Time from die temperature dropping below Thermal Shutdown Temperature,  $T_{TH}$ , to when the device turns itself back on.

# 900MHz ISM-Band, 250mW Power Amplifiers with Analog or Digital Gain Control

## Typical Operating Characteristics

(MAX2232/MAX2233 Evaluation Kit,  $V_{CC} = +3.6V$ ,  $CTRL = V_{CC}$ ,  $\overline{SHDN} = D0 = D1 = V_{CC}$ ,  $P_{RFIN} = 0dBm$ ,  $f_{RFIN} = 915MHz$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# 900MHz ISM-Band, 250mW Power Amplifiers with Analog or Digital Gain Control

## Pin Description

MAX2232/MAX2233

PIN		NAME	FUNCTION
MAX2232	MAX2233		
1	1	RFIN	RF Input Port. Requires external matching network and blocking capacitor.
2	2	GND	Input Stage Ground. Connect directly to low-inductance ground plane. If vias are used, separate them from other GND pin vias.
3	—	$\overline{\text{SHDN}}$	Shutdown Control Input. Drive $\overline{\text{SHDN}}$ low to place the device in shutdown mode. Drive high for normal operation.
—	3	D1	Digital Gain/Shutdown Control Input. MSB of the 2-bit digital output power control. D0 and D1 set the output power to one of three discrete levels. To place the device in shutdown, drive D0 and D1 low (Table 2).
4	—	CTRL	Analog Gain-Control Input. Apply a voltage between 0.6V and 2.2V to vary the gain of the PA. Drive CTRL below 0.4V to place the device in standby mode. Drive CTRL above 2.2V to place the device in peak output power mode.
—	4	D0	Digital Gain/Shutdown Control Input. LSB of the 2-bit digital output power control. D0 and D1 set the output power to one of three discrete levels. To place the device in shutdown, drive D0 and D1 low (Table 2).
5, 6	5, 6	GND	Second Stage Ground. Connect directly to low-inductance ground plane. If vias are used, separate them from other GND pin vias.
7	7	GND	Output Stage Ground. Connect directly to low-inductance ground plane. If vias are used, separate them from other GND pin vias.
8	8	RFOUT	Open-Collector, RF Output Port. Connect output matching network to this pin.
9	9, 13, 14	N.C.	No Connection. Do not make a connection to this pin.
10	10	TSET	Thermal Shutdown Timeout Capacitor Terminal. Connect a capacitor from TSET to ground to limit thermal cycling.
11	11	VCC	Second Stage Supply Voltage. Bypass with appropriate capacitors to GND.
12	12	VCC	Input Stage Supply Voltage. Bypass with appropriate capacitors to GND.
13	—	RAMP-	Negative Terminal of Output Power Ramp Capacitor. Connect capacitor, C <sub>RAMP</sub> , between RAMP+ and RAMP- to control the rise and fall time of the output power ramp.
14	—	RAMP+	Positive Terminal of Output Power Ramp Capacitor. Connect capacitor, C <sub>RAMP</sub> , between RAMP+ and RAMP- to control the rise and fall time of the output power ramp.
15	15	GND	Bias Circuitry Ground. Connect directly to low-inductance ground plane. If vias are used, separate them from other GND pin vias.
16	16	VCC	Bias Circuitry Supply Voltage. Bypass with appropriate capacitors to GND.
SLUG	SLUG	GND	Output Stage Ground. Provides additional thermal conduction, as well as a low-inductance path to ground. Connect directly to low-inductance ground plane.

# 900MHz ISM-Band, 250mW Power Amplifiers with Analog or Digital Gain Control

## Detailed Description

The MAX2232/MAX2233 are nonlinear power amplifiers (PAs) intended for constant envelope applications (FM, FSK, GMSK). The devices operate over the 902MHz to 928MHz frequency range and provide typically 250mW of output power and 44% efficiency from a single +2.7V to +5.5V supply. Both devices typically provide 24dB of gain, which is adjustable over a continuous 24dB range through an analog voltage on CTRL of the MAX2232 or in two 10dB steps through the 2-bit programmable gain inputs (D0, D1) on the MAX2233. A low-power shutdown mode on both devices reduces supply current to 0.2 $\mu$ A.

All bias, gain control, and temperature-sensing circuitry is provided on-chip to save board space and reduce component count. The signal path includes a variable gain amplifier (VGA), an output driver, and an output power transistor. On-chip interstage matching networks are provided for optimal loading and power transfer. Internal bias circuitry responds to CTRL and  $\overline{\text{SHDN}}$  of the MAX2232, or to the 2-bit gain/shutdown control DAC of the MAX2233, providing optimum biasing and efficiency as well as shutdown and ramp control functions. A unique temperature-sensing circuit protects the device from overheating by shutting down the PA until a safe temperature is resumed.

The devices come in a 16-pin PQSOP package, which incorporates a slug on the bottom of the device to increase heat conduction and provide a low inductance path to ground.

### RF Input Stage (Variable Gain Amplifier)

The input stage includes a variable gain amplifier (VGA) with 24dB gain-control range. With the appropriate matching network, the input VSWR is nominally 1.5:1 during operation and the change in VSWR is only 1.2:1, relative to normal operation. This stage remains active during standby mode (MAX2232) to provide a constant input impedance but is off during shutdown mode (MAX2232/MAX2233). AC-couple this port with a DC-blocking capacitor.

### RF Second Stage (Driver)

The driver provides gain to overcome interstage matching losses and to produce a signal large enough to drive the output power transistor into saturation. The driver stage is off during standby (MAX2232) and shutdown (MAX2232/MAX2233) modes.

### RF Output Stage (Output Power Transistor)

The output power transistor delivers +24dBm of output power from a single +3.6V supply. The transistor's open-collector output requires a pull-up inductor to

VCC for proper biasing, as well as a proper output matching network to ensure optimum output power. Connect the output matching network to RFOUT (pin 8). See the *Typical Application Circuit* for bias and matching components suitable for 900MHz operation. The ground of the output stage is connected to a metal slug on the bottom of the MAX2232/MAX2233's 16-pin PQSOP package. The metal slug increases heat conduction and provides a low-inductance path to ground. Solder the metal slug to the PC-board ground plane.

## MAX2232

### Analog Gain Control and Power Management

#### Shutdown Mode

Drive the shutdown ( $\overline{\text{SHDN}}$ ) pin below 0.6V to place the MAX2232 in shutdown mode. The VGA, driver, and output transistor are off in shutdown mode and the supply current is typically reduced to 0.2 $\mu$ A. When  $\overline{\text{SHDN}}$  is above 2.0V, the device is enabled.

#### Standby Mode

Drive  $\overline{\text{SHDN}}$  above 2.0V and CTRL below 0.4V to place the MAX2232 in standby mode. In standby mode, the VGA remains biased while the driver and output transistor are disabled. Supply current is typically 20mA in standby mode. This mode allows the device to maintain a good input VSWR while maintaining 38dB of isolation. This is useful to users who drive the PA with a direct modulated VCO, where pulling of the VCO results from changes in the input VSWR.

#### Analog Gain Control

The voltage applied to the gain-control (CTRL) pin varies the output power of the MAX2232 continuously over a 24dB range. An internal comparator holds the PA to a constant peak output power if  $V_{\text{CTRL}}$  is above 2.2V. For  $V_{\text{CTRL}}$  below 0.4V, the PA is in standby mode. CTRL presents a high input impedance, allowing the  $V_{\text{CTRL}}$  voltage to be set with a resistor-divider or a voltage output DAC.

#### Output Power Autoramping

The internal bias circuitry of the MAX2232 automatically ramps the output power of the PA down or up at a constant rate (in W/sec) when switched in or out of shutdown mode. The output power is ramped to the level set by  $V_{\text{CTRL}}$  on the MAX2232. The output power rise and fall time ramp is set by placing a capacitor, CRAMP, between RAMP+ and RAMP-. This provides an easy means of avoiding spectral splatter and complying with transmit mask requirements, without using a separate controller. The output power rise and fall time is set by the value of CRAMP.

# 900MHz ISM-Band, 250mW Power Amplifiers with Analog or Digital Gain Control

## MAX2233

### Digital Gain Control and Power Management

The MAX2233 responds to logic-level signals at the device's 2-bit DAC inputs, D0 and D1, placing the device in shutdown mode or into one of three discrete output power levels. See Table 2 for operating modes and output power levels. Setting D0 and D1 to a logic-level low places the device in shutdown mode and reduces supply current to 0.2µA. The VGA, driver, and output stage are off in shutdown mode, while the input impedance is only slightly changed. Setting D0 and D1 to one of the other three modes adjusts the output power to one of three discrete levels in 10dB steps.

### Thermal Shutdown

The MAX2232/MAX2233 feature a thermal shutdown mode that helps to protect the device from damage when the die temperature becomes excessive. If the temperature of the die exceeds the thermal shutdown temperature,  $T_{TH}$ , the VGA is forced into a low-gain mode and output power is reduced to a minimum. After

the PA's die temperature drops below  $T_{TH}$ , the device remains in thermal shutdown mode for the thermal shutdown timeout period,  $t_{TH}$ . A single capacitor,  $C_{TSET}$ , from TSET to ground sets  $t_{TH}$ . The thermal shutdown timeout period helps to limit device thermal cycling that results if the source of the excessive temperature is not removed.  $t_{TH}$  is set by the value of  $C_{TSET}$ .

### Applications Information

Proper attention to voltage supply bypassing is essential for high-frequency RF circuit stability. Bypass  $V_{CC}$  with 0.1µF, 10nF, and 100pF capacitors in parallel with each other to ground. Use separate vias to the ground plane for each of the bypass capacitors and minimize trace length to reduce inductance. Use separate vias to the ground plane for each ground pin. Use low-inductance ground connections.

Decouple  $\overline{SHDN}$ , CTRL, D0, and D1 with 0.1µF capacitors to ground to minimize noise on the internal bias cell. Use a series resistor (typically 100Ω) to further reduce coupling of high-frequency signals into the control pins.

Table 1. MAX2232 Operating Modes

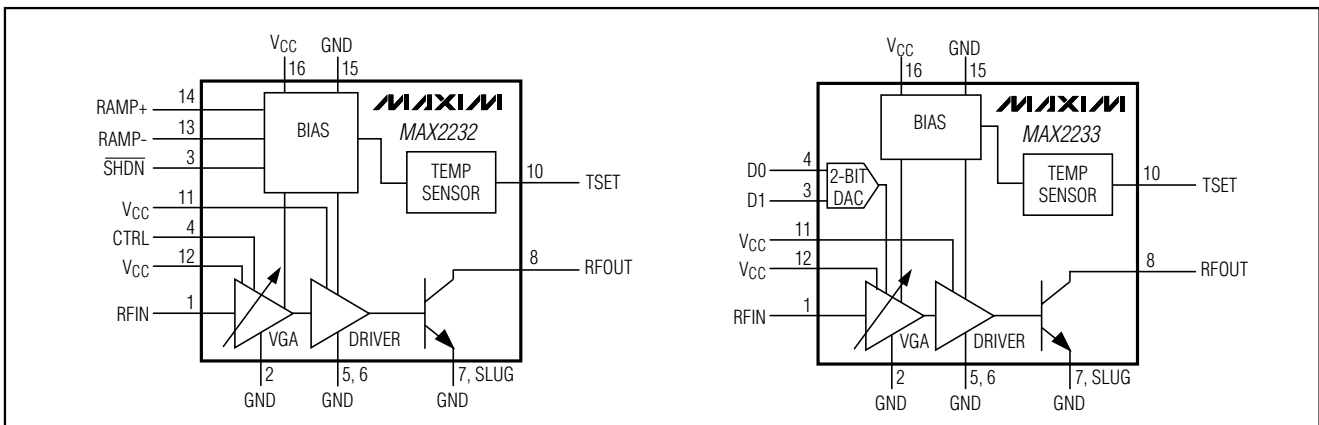
MODE	$V_{\overline{SHDN}}$	$V_{CTRL}$	OUTPUT POWER ( $P_{RFIN} = 0dBm$ , $V_{CC} = +3.6V$ )
Shutdown	< 0.6V	X	< -35dBm
Standby	> 2.0V	≤ 0.4V	< -35dBm
Variable Gain	> 2.0V	$0.6V \leq V_{CTRL} < 2.2V$	0dBm to +24dBm
Maximum Gain	> 2.0V	> 2.2V	+24 dBm

X = Don't care

Table 2. MAX2233 Operating Modes Truth Table

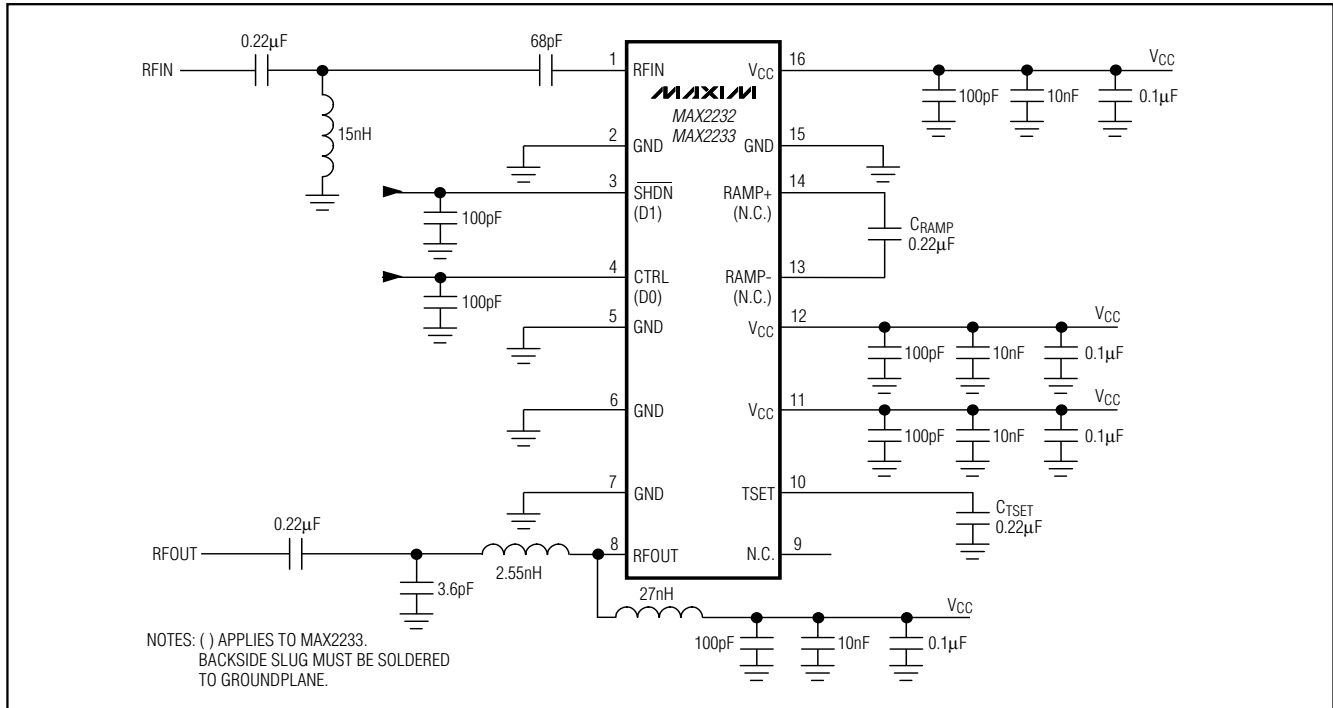
MODE	D1	D0	OUTPUT POWER ( $P_{RFIN} = 0dBm$ , $V_{CC} = +3.6V$ )
Shutdown	0	0	< -35dBm
Low Power	0	1	+6.5dBm
Medium Power	1	0	+15dBm
High Power	1	1	+24dBm

### Functional Diagrams



# 900MHz ISM-Band, 250mW Power Amplifiers with Analog or Digital Gain Control

## Typical Application Circuit



## Package Information

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.010	0.127	0.25
A2	.055	.059	1.40	1.55
B	.008	.012	0.20	0.31
C	.007	.010	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
D	.189	.196	4.80	4.98
X	.107	.123	2.717	3.124

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
D	.386	.391	9.80	9.98
X	.271	.287	6.883	7.290

NOTES:  
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS  
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"  
3. CONTROLLING DIMENSIONS: INCHES

MAXIM  
PROPRIETARY INFORMATION  
TITLE: PACKAGE OUTLINE, POWER QSDP (PSSDP2)  
APPROVAL: DOCUMENT CONTROL NO. 21-0063 REV. A 1/1

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