FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

SEMICONDUCTOR®

74LCX162244

Low Voltage 16-Bit Buffer/Line Driver with 26Ω Series Resistors in Outputs

General Description

The LCX162244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX162244 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

In addition, the outputs include equivalent 26Ω (nominal) series resistors to reduce overshoot and undershoot and are designed to sink/source up to 12 mA at V_{CC} = 3.0V.

The LCX162244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs and outputs

■ 2.3V–3.6V V_{CC} specifications provided

■ Outputs include equivalent series resistance of 26Ω to make external termination resistors unnecessary and reduce overshoot and undershoot

■ 5.3 ns t_{PD} max (V_{CC} = 3.0V), 20 μA I_{CC} max

■ Power down high impedance inputs and outputs

■ ±12 mA output drive (V_{CC} = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

■ ESD performance:
    Human body model > 2000V
    Machine model > 200V

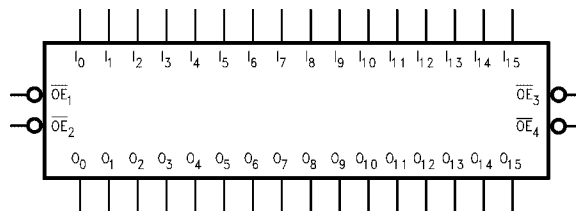■ Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Ordering Code:

Order Number	Package Number	Package Description
74LCX162244GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LCX162244MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX162244MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

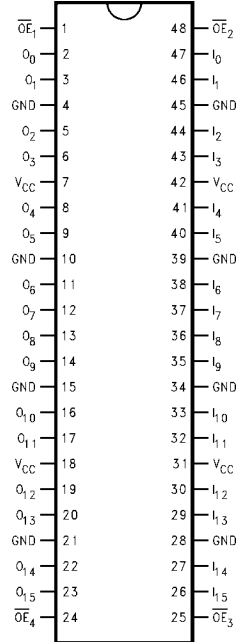**Note 1:** BGA package available in Tape and Reel only.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
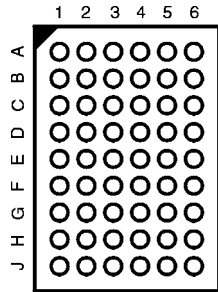
Logic Symbol

Connection Diagrams

Pin Assignment for SSOP and TSSOP

$\overline{OE}_1$	1		48	$\overline{OE}_2$
O_0	2		47	I_0
O_1	3		46	I_1
GND	4		45	GND
O_2	5		44	I_2
O_3	6		43	I_3
V_{CC}	7		42	V_{CC}
O_4	8		41	I_4
O_5	9		40	I_5
GND	10		39	GND
O_6	11		38	I_6
O_7	12		37	I_7
O_8	13		36	I_8
O_9	14		35	I_9
GND	15		34	GND
O_{10}	16		33	I_{10}
O_{11}	17		32	I_{11}
V_{CC}	18		31	V_{CC}
O_{12}	19		30	I_{12}
O_{13}	20		29	I_{13}
GND	21		28	GND
O_{14}	22		27	I_{14}
O_{15}	23		26	I_{15}
$\overline{OE}_4$	24		25	$\overline{OE}_3$

Pin Assignment for FBGA

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	I_{15}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

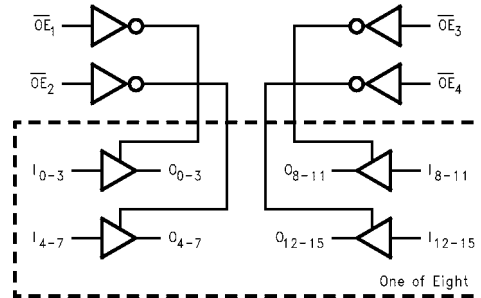| Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

The LCX162244 contains sixteen non-inverting buffers with 3-STATE standard outputs. The device is designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceiver/transmitters. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 5)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±12	
		V_{CC} = 2.7V – 3.0V		±8	mA
		V_{CC} = 2.3V – 2.7V		±4	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.3 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −4 mA	2.3	1.8		
		I_{OH} = −4 mA	2.7	2.2		
		I_{OH} = −6 mA	3.0	2.4		
		I_{OH} = −8 mA	2.7	2.0		
		I_{OH} = −12 mA	3.0	2.0		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 – 3.6		0.2	V
		I_{OL} = 4 mA	2.3		0.6	
		I_{OL} = 4 mA	2.7		0.4	
		I_{OL} = 6 mA	3.0		0.55	
		I_{OL} = 8 mA	2.7		0.6	
		I_{OL} = 12 mA	3.0		0.8	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5$	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.3 – 3.6		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C Min	Max	Units
I_OFF	Power-Off Leakage Current	V_IN or V_O = 5.5V	0		10	μA
I_CC	Quiescent Supply Current	V_I = V_CC or GND	2.3 – 3.6		20	μA
ΔI_CC	Increase in I_CC per Input	V_IH = V_CC −0.6V	2.3 – 3.6		500	μA

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Electrical Characteristics

Symbol	Parameter	T_A = −40°C to +85°C, R_L = 500 Ω V_CC = 3.3V ± 0.3V C_L = 50 pF Min	Max	V_CC = 2.7V C_L = 50 pF Min	Max	V_CC = 2.5V ± 0.2V C_L = 30 pF Min	Max	Units
t_PHL	Propagation Delay	1.0	5.3	1.0	6.0	1.0	6.4	ns
t_PLH	Data to Output	1.0	5.3	1.0	6.0	1.0	6.4	
t_PZL	Output Enable Time	1.0	6.3	1.0	7.1	1.0	8.2	ns
t_PZH		1.0	6.3	1.0	7.1	1.0	8.2	
t_PLZ	Output Disable Time	1.0	5.4	1.0	5.7	1.0	6.5	ns
t_PHZ		1.0	5.4	1.0	5.7	1.0	6.5	
t_OSHL	Output to Output Skew (Note 8)		1.0					ns
t_OSLH			1.0					

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_OSHL) or LOW-to-HIGH (t_OSLH). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_CC (V)	T_A = 25°C Typical	Units
V_OLP	Quiet Output Dynamic Peak V_OL	C_L = 50 pF, V_IH = 3.3V, V_IL = 0V	3.3	0.35	V
		C_L = 30 pF, V_IH = 2.5V, V_IL = 0V	2.5	0.25	
V_OLV	Quiet Output Dynamic Valley V_OL	C_L = 50 pF, V_IH = 3.3V, V_IL = 0V	3.3	−0.35	V
		C_L = 30 pF, V_IH = 2.5V, V_IL = 0V	2.5	−0.25	

Capacitance

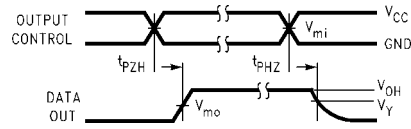| Symbol	Parameter	Conditions	Typical	Units
C_IN	Input Capacitance	V_CC = Open, V_I = 0V or V_CC	7	pF
C_OUT	Output Capacitance	V_CC = 3.3V, V_I = 0V or V_CC	8	pF
C_PD	Power Dissipation Capacitance	V_CC = 3.3V, V_I = 0V or V_CC, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)

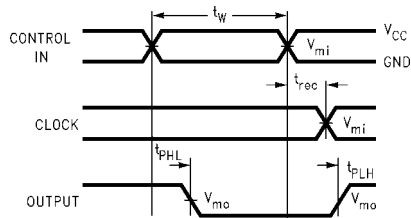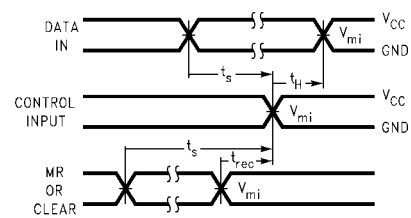| V$_I$	C$_L$
6V for V$_{CC}$ = 3.3V, 2.7V	50 pF
V$_{CC}$ * 2 for V$_{CC}$ = 2.5V	30 pF

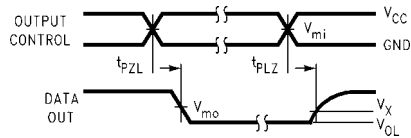**Waveform for Inverting and Non-Inverting Functions**

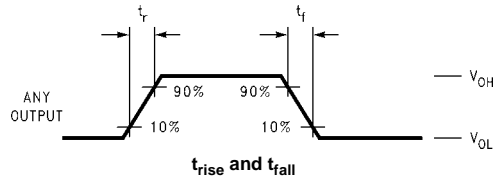**3-STATE Output High Enable and Disable Times for Logic**

Propagation Delay. Pulse Width and t$_{rec}$ Waveforms

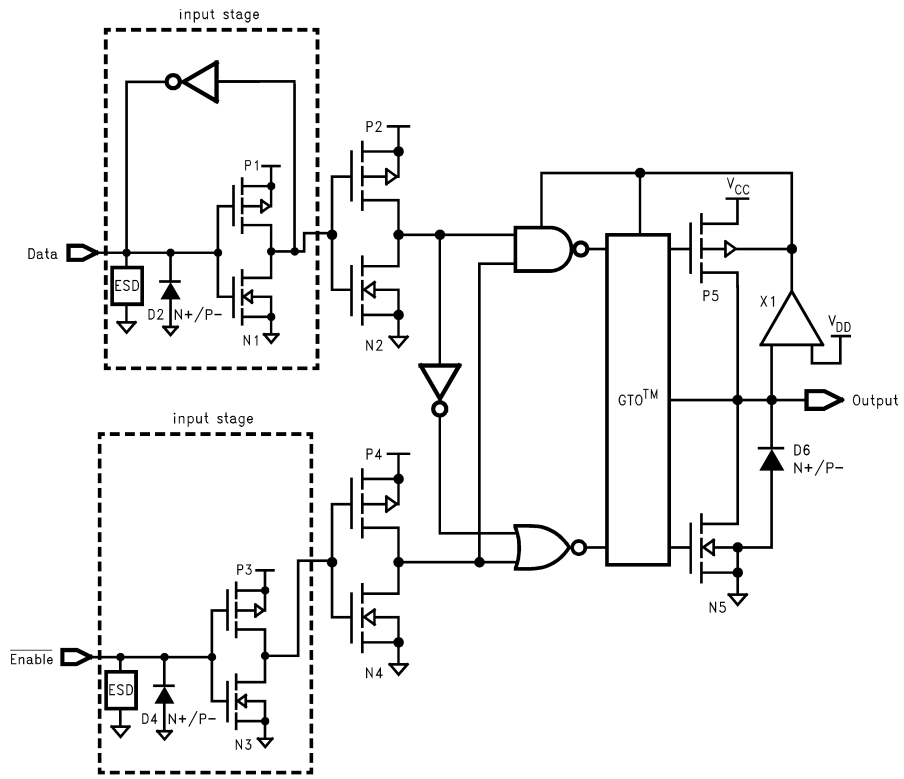**Setup Time, Hold Time and Recovery Time for Logic**

3-STATE Output Low Enable and Disable Times for Logic

t$_{rise}$ and t$_{fall}$

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_r$ = t$_f$ = 3ns)

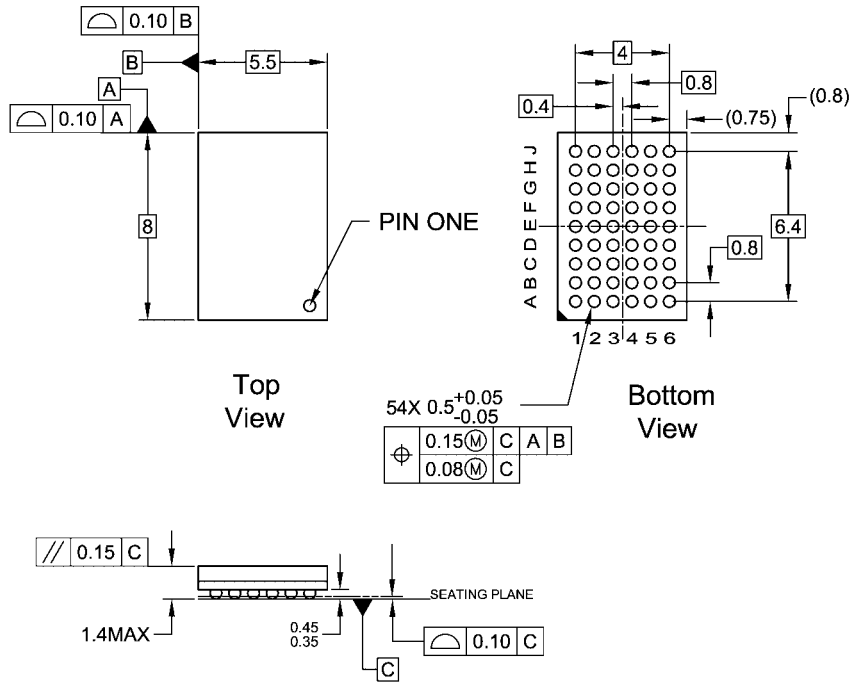| Symbol	V$_{CC}$		
	3.3V $\pm$ 0.3V	2.7V	2.5V $\pm$ 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

```
⌒ 0.10 B

B ◄── 5.5
A
⌒ 0.10 A ▲

8

PIN ONE ○

Top
View
```

```
├── 4 ──┤
0.4 ──►   ◄── 0.8
          (0.75) ◄──   (0.8)

J  ○○○|○○○
H  ○○○○○○
G  ○○○○○○
F  ○○○|○○○        6.4
E  ○○○○○○
D  ○○○|○○○   0.8
C  ○○○○○○
B  ○○○○○○
A  ○○○|○○○

A B C D E F G H J
1 2 3 4 5 6

54X 0.5 +0.05/-0.05

⊕  0.15 Ⓜ C A B
   0.08 Ⓜ C

Bottom
View
```

```
// 0.15 C

1.4 MAX        0.45
               0.35

C

SEATING PLANE

⌒ 0.10 C
```
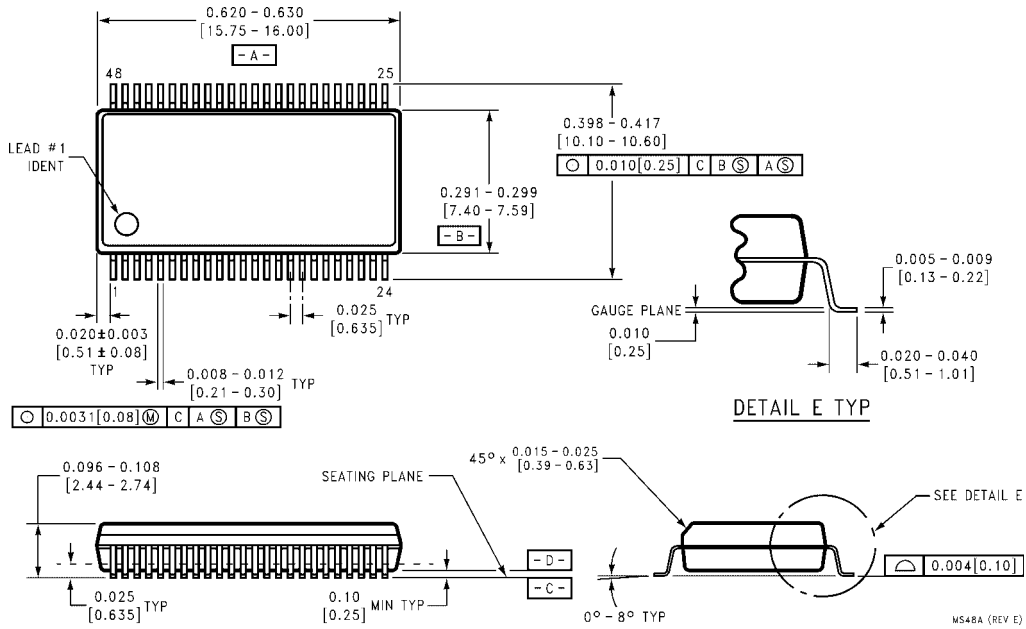
NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

○ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

1   24

0.025
[0.635] TYP

0.020±0.003
[0.51±0.08]
TYP

0.008 – 0.012
[0.21 – 0.30] TYP

○ 0.0031[0.08] Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE
0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

– D –
– C –

0° – 8° TYP

△ 0.004[0.10]

MS48A (REV E)

**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC

www.onsemi.com