

# MPC852T

## Hardware Specifications

This document contains detailed information for the MPC852T about power considerations, DC/AC electrical characteristics, AC timing specifications, and pertinent electrical and physical characteristics of the MPC852T. For information about functional characteristics of the processor, refer to the *MPC866 PowerQUICC Family Users Manual* (MPC866UM). The MPC852T contains a PowerPC™ processor core.

## 1 Overview

The MPC852T PowerQUICC™ is a 0.18-micron derivative of the MPC860 PowerQUICC family, and can operate up to 100 MHz on the MPC8xx core with a 66-MHz external bus. The MPC852T has a 1.8 V core and a 3.3 V I/O operation with 5-V TTL compatibility. The MPC852T integrated communications controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in Ethernet control applications, including CPE equipment, Ethernet routers and hubs, VoIP clients, and WiFi access points.

The MPC852T is a PowerPC architecture-based derivative of the Motorola MPC860 Quad Integrated Communications Controller (PowerQUICC). The CPU on the MPC852T is the MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches. The MPC852T is the subset of this family of devices.

### Contents

|                                                    |    |
|----------------------------------------------------|----|
| 1. Overview .....                                  | 1  |
| 2. Features .....                                  | 2  |
| 3. Maximum Tolerated Ratings .....                 | 5  |
| 4. Thermal Characteristics .....                   | 5  |
| 5. Power Dissipation .....                         | 6  |
| 6. DC Characteristics .....                        | 7  |
| 7. Thermal Calculation and Measurement .....       | 8  |
| 8. References .....                                | 10 |
| 9. Power Supply and Power Sequencing .....         | 10 |
| 10. Mandatory Reset Configurations .....           | 11 |
| 11. Layout Practices .....                         | 12 |
| 12. Bus Signal Timing .....                        | 13 |
| 13. IEEE 1149.1 Electrical Specifications .....    | 41 |
| 14. CPM Electrical Characteristics .....           | 43 |
| 15. FEC Electrical Characteristics .....           | 56 |
| 16. Mechanical Data and Ordering Information ..... | 60 |
| 17. Document Revision History .....                | 78 |

## 2 Features

The MPC852T is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). [Figure 1](#) shows the MPC852T block diagram.

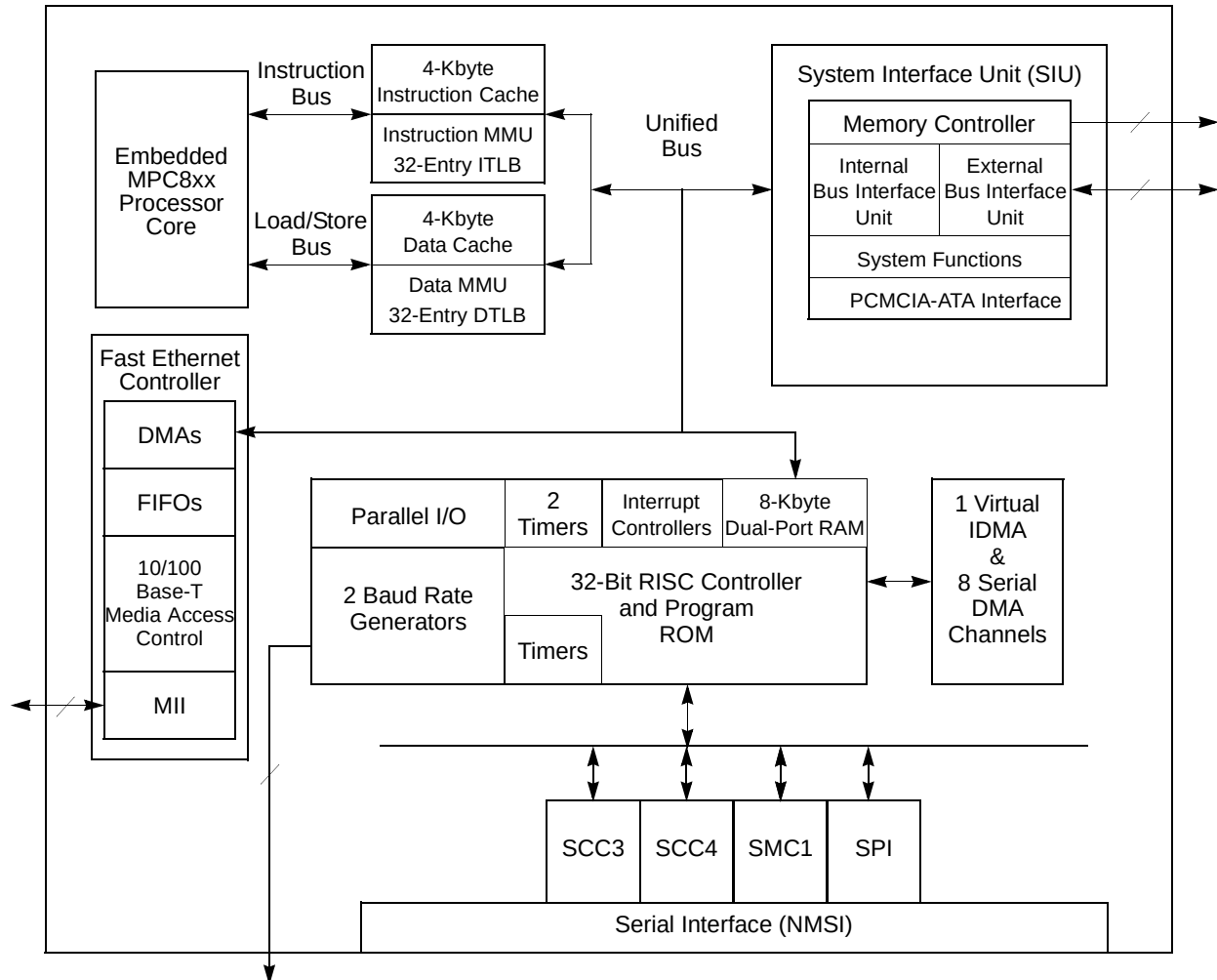
The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - The 50 MHz / 66 MHz core frequencies support both 1:1 and 2:1 modes.
  - The 80 MHz / 100 MHz core frequencies support 2:1 mode only.
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with 32 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - 4-Kbyte instruction cache is two-way, set-associative with 128 sets.
    - 4-Kbyte data cache is two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces, and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or  $\overline{\text{RAS}}$  to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller-programmable to support most size and speed memory interfaces
  - Four  $\overline{\text{CAS}}$  lines, four  $\overline{\text{WE}}$  lines, and one  $\overline{\text{OE}}$  line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet Controller (FEC)
- General-purpose timers
  - Two 16-bit timers or one 32-bit timer
  - Gate mode can enable or disable counting.
  - Interrupt can be masked on reference match and event capture.

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Seven port pins with interrupt capability
  - Eighteen internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest-priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - 8 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Two baud rate generators
  - Independent (can be connected to any SCC3/4 or SMC1)
  - Allows changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3 optional on SCC3 & SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Universal asynchronous receiver transmitter (UART)
  - Totally transparent (bit streams)
  - Totally transparent (frame-based with optional cyclic redundancy check (CRC))
- One SMC (serial management channels)
  - UART
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant

## Features

- Supports one independent PCMCIA socket; 8-memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power
- 1.8 V Core and 3.3 V I/O operation with 5-V TTL compatibility. Refer to [Table 5](#) for a listing of the 5-V Tolerant pins.



**Figure 1. MPC852T Block Diagram**

### 3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC852T. [Table 1](#) provides the maximum ratings and operating temperatures.

**Table 1. Maximum Tolerated Ratings**

| Rating                      | Symbol                                                    | Value                         | Unit |
|-----------------------------|-----------------------------------------------------------|-------------------------------|------|
| Supply voltage <sup>1</sup> | V <sub>DDL</sub> (core voltage)                           | – 0.3 to 3.4                  | V    |
|                             | V <sub>DDH</sub> (I/O voltage)                            | – 0.3 to 4                    | V    |
|                             | V <sub>DDSYN</sub>                                        | – 0.3 to 3.4                  | V    |
|                             | Difference between V <sub>DDL</sub> to V <sub>DDSYN</sub> | 100                           | mV   |
| Input voltage <sup>2</sup>  | V <sub>in</sub>                                           | GND – 0.3 to V <sub>DDH</sub> | V    |
| Storage temperature range   | T <sub>stg</sub>                                          | – 55 to +150                  | °C   |

<sup>1</sup> The power supply of the device must start its ramp from 0.0 V.

<sup>2</sup> Functional operating conditions are provided with the DC electrical specifications in [Table 5](#). Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

**Caution:** All inputs that tolerate 5 V cannot be more than 2.5 V greater than V<sub>DDH</sub>. This restriction applies to power-up and normal operation (that is, if the MPC852T is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

**Table 2. Operating Temperatures**

| Rating                              | Symbol              | Value | Unit |
|-------------------------------------|---------------------|-------|------|
| Temperature <sup>1</sup> (standard) | T <sub>A(min)</sub> | 0     | °C   |
|                                     | T <sub>J(max)</sub> | 95    | °C   |
| Temperature (extended)              | T <sub>A(min)</sub> | – 40  | °C   |
|                                     | T <sub>J(max)</sub> | 100   | °C   |

<sup>1</sup> Minimum temperatures are guaranteed as ambient temperature, T<sub>A</sub>. Maximum temperatures are guaranteed as junction temperature, T<sub>J</sub>.

This device contains circuitry protecting against damage that high-static voltage or electrical fields cause; however, Motorola recommends taking normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V<sub>DD</sub>). -- V<sub>DDH</sub>.

### 4 Thermal Characteristics

[Table 3](#) shows the thermal characteristics for the MPC852T.

**Table 3. MPC852T Thermal Resistance Data**

| Rating                               | Environment           |                         | Symbol                        | Value | Unit |
|--------------------------------------|-----------------------|-------------------------|-------------------------------|-------|------|
| Junction to ambient <sup>1</sup>     | Natural convection    | Single layer board (1s) | $R_{\theta JA}$ <sup>2</sup>  | 49    | °C/W |
|                                      |                       | Four layer board (2s2p) | $R_{\theta JMA}$ <sup>3</sup> | 32    |      |
|                                      | Air flow (200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ <sup>3</sup> | 41    |      |
|                                      |                       | Four layer board (2s2p) | $R_{\theta JMA}$ <sup>3</sup> | 29    |      |
| Junction to board <sup>4</sup>       |                       |                         | $R_{\theta JB}$               | 24    |      |
| Junction to case <sup>5</sup>        |                       |                         | $R_{\theta JC}$               | 13    |      |
| Junction to package top <sup>6</sup> | Natural convection    |                         | $\Psi_{JT}$                   | 3     |      |
|                                      | Air flow (200 ft/min) |                         | $\Psi_{JT}$                   | 2     |      |

<sup>1</sup> Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal

<sup>3</sup> Per JEDEC JESD51-6 with the board horizontal

<sup>4</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2

## 5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

**Table 4. Power Dissipation ( $P_D$ )**

| Die Revision | Bus Mode | Frequency (MHz) | Typical <sup>1</sup> | Maximum <sup>2</sup> | Unit |
|--------------|----------|-----------------|----------------------|----------------------|------|
| 0            | 1:1      | 50              | 110                  | 140                  | mW   |
|              |          | 66              | 150                  | 180                  | mW   |
|              | 2:1      | 66              | 140                  | 160                  | mW   |
|              |          | 80              | 170                  | 200                  | mW   |
|              |          | 100             | 210                  | 250                  | mW   |

<sup>1</sup> Typical power dissipation is measured at 1.9 V.

<sup>2</sup> Maximum power dissipation at  $V_{DDL}$  and  $V_{DDSYN}$  is at 1.9 V. and  $V_{DDH}$  is at 3.465 V.

#### NOTE

Values in Table 4 represent  $V_{DDL}$ -based power dissipation, and do not include I/O power dissipation over  $V_{DDH}$ . I/O power dissipation varies widely by application that buffer current can cause, depending on external circuitry.

The  $V_{DDSYN}$  power dissipation is negligible.

## 6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC852T.

**Table 5. DC Electrical Specifications**

| Characteristic                                                                                                                                                                                    | Symbol                                      | Min                  | Max       | Unit    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|----------------------|-----------|---------|
| Operating voltage                                                                                                                                                                                 | $V_{DDH}$                                   | 3.135                | 3.465     | V       |
|                                                                                                                                                                                                   | $V_{DDL}$                                   | 1.7                  | 1.9       | V       |
|                                                                                                                                                                                                   | $V_{DDSYN}$                                 | 1.7                  | 1.9       | V       |
|                                                                                                                                                                                                   | Difference between $V_{DDL}$ to $V_{DDSYN}$ | —                    | 100       | mV      |
| Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25], PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{TRST}$ , TMS, MII_TXEN, MII_MDIO) <sup>1</sup> | $V_{IH}$                                    | 2.0                  | 3.465     | V       |
| Input low voltage                                                                                                                                                                                 | $V_{IL}$                                    | GND                  | 0.8       | V       |
| EXTAL, EXTCLK input high voltage                                                                                                                                                                  | $V_{IHC}$                                   | $0.7 \times V_{DDH}$ | $V_{DDH}$ | V       |
| Input leakage current, $V_{in} = 5.5$ V (Except TMS, $\overline{TRST}$ , DSCK and DSDI pins) for 5-V tolerant pins <sup>1</sup>                                                                   | $I_{in}$                                    | —                    | 100       | $\mu A$ |
| Input leakage current, $V_{in} = V_{DDH}$ (Except TMS, $\overline{TRST}$ , DSCK, and DSDI)                                                                                                        | $I_{in}$                                    | —                    | 10        | $\mu A$ |
| Input leakage current, $V_{in} = 0$ V (Except TMS, $\overline{TRST}$ , DSCK and DSDI pins)                                                                                                        | $I_{in}$                                    | —                    | 10        | $\mu A$ |
| Input capacitance <sup>2</sup>                                                                                                                                                                    | $C_{in}$                                    | —                    | 20        | pF      |

Table 5. DC Electrical Specifications (continued)

| Characteristic                                                                                                                                                                                                                                                                                                                    | Symbol   | Min | Max | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----|-----|------|
| Output high voltage, $I_{OH} = -2.0$ mA,<br>$V_{DDH} = 3.0$ V<br>Except XTAL and open drain pins                                                                                                                                                                                                                                  | $V_{OH}$ | 2.4 | —   | V    |
| Output low voltage<br>$I_{OL} = 2.0$ mA (CLKOUT)<br>$I_{OL} = 3.2$ mA <sup>3</sup><br>$I_{OL} = 5.3$ mA <sup>4</sup><br>$I_{OL} = 7.0$ mA (TXD1/pa14, txd2/pa12)<br>$I_{OL} = 8.9$ mA ( $\overline{TS}$ , $\overline{TA}$ , $\overline{TEA}$ , $\overline{BI}$ , $\overline{BB}$ ,<br>$\overline{HRESET}$ , $\overline{SRESET}$ ) | $V_{OL}$ | —   | 0.5 | V    |

<sup>1</sup> The PA[0:3], PA[8:11], PB15, PB[24:25], PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK,  $\overline{TRST}$ , TMS, MII\_TXEN, MII\_MDIO are 5 V-tolerant pins.

<sup>2</sup> Input capacitance is periodically sampled.

<sup>3</sup> A(0:31), TSIZ0/ $\overline{REG}$ , TSIZ1, D(0:31), DP(0:3)/ $\overline{IRQ}$ (3:6), RD/ $\overline{WR}$ ,  $\overline{BURST}$ ,  $\overline{RSV}/\overline{IRQ2}$ , IWP(0:1)/VFLS(0:1), RXD3/PA11, TXD3/PA10, RXD4/PA9, TXD4/PA8, TIN3/BRGO3/CLK5/PA3, BRGCLK2/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, TOUT4/CLK8/PA0, SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, SMTXD1/PB25, SMRXD1/PB24, BRGO3/PB15, RTS1/DREQ0/PC15, RTS3/PC13, RTS4/PC12, CTS3/PC7, CD3/PC6, CTS4/SDACK1/PC5, CD4/PC4, MII-RXD3/PD15, MII-RXD2/PD14, MII-RXD1/PD13, MII-MDC/PD12, MII-TXERR/RXD3/PD11, MII-RX0/TXD3/PD10, MII-TXD0/RXD4/PD9, MII-RXCLK/TXD4/PD8, MII-TXD3/PD5, MII-RXDV/RTS4/PD6, MII-RXERR/RTS3/PD7, MII-TXD2/REJECT3/PD4, MII-TXD1/REJECT4/PD3, MII\_CRS, MII\_MDIO, MII\_TXEN, MII\_COL

<sup>4</sup>  $\overline{BDIP}/\overline{GPL\_B}$ (5),  $\overline{BR}$ ,  $\overline{BG}$ , FRZ/ $\overline{IRQ6}$ ,  $\overline{CS}$ (0:5),  $\overline{CS}$ (6),  $\overline{CS}$ (7),  $\overline{WE0}/\overline{BS\_B0}/\overline{IORD}$ ,  $\overline{WE1}/\overline{BS\_B1}/\overline{IOWR}$ ,  $\overline{WE2}/\overline{BS\_B2}/\overline{PCOE}$ ,  $\overline{WE3}/\overline{BS\_B3}/\overline{PCWE}$ ,  $\overline{BS\_A}$ (0:3),  $\overline{GPL\_A0}/\overline{GPL\_B0}$ ,  $\overline{OE}/\overline{GPL\_A1}/\overline{GPL\_B1}$ ,  $\overline{GPL\_A}$ (2:3)/ $\overline{GPL\_B}$ (2:3)/ $\overline{CS}$ (2:3), UPWAITA/ $\overline{GPL\_A4}$ ,  $\overline{GPL\_A5}$ ,  $\overline{ALE\_A}$ ,  $\overline{CE1\_A}$ ,  $\overline{CE2\_A}$ , DSCK, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30)

## 7 Thermal Calculation and Measurement

For the following discussions,  $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$ , where  $P_{I/O}$  is the power dissipation of the I/O drivers.

### NOTE

The  $V_{DDSYN}$  power dissipation is negligible.

### 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature,  $T_J$ , in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$  = ambient temperature °C

$R_{\theta JA}$  = package junction-to-ambient thermal resistance (°C/W)

$P_D$  = power dissipation in package



The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity  $T_J - T_A$ ) are possible.

## 7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$  = junction-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  = junction-to-case thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta CA}$  = case-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$R_{\theta JC}$  is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. Thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$  = junction-to-board thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

$T_B$  = board temperature  $^{\circ}\text{C}$

$P_D$  = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

## 7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

## 7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$  = thermal characterization parameter

$T_T$  = thermocouple temperature on top of package

$P_D$  = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors that cooling effects of the thermocouple wire cause.

## 8 References

Semiconductor Equipment and Materials International(415) 964-5111  
805 East Middlefield Rd  
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or  
(Available from Global Engineering documents)303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, "An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module," Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. B. Joiner and V. Adams, "Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling," Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

## 9 Power Supply and Power Sequencing

This section provides design considerations for the MPC852T power supply. The MPC852T has a core voltage ( $V_{DDL}$ ) and PLL voltage ( $V_{DDSYN}$ ) that operates at a lower voltage than the I/O voltage  $V_{DDH}$ . The I/O section of the MPC852T is supplied with 3.3 V across  $V_{DDH}$  and  $V_{SS}$  (GND).

The signal PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15] PD[3:15], TDI, TDO, TCK, TRST, TMS, MII\_TXEN, MII\_MDIO are 5 V-tolerant. All inputs cannot be more than 2.5 V greater than  $V_{DDH}$ . In addition, 5 V-tolerant pins can not exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power-on reset or power down and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- $V_{DDL}$  must not exceed  $V_{DDH}$  during power-on reset or power down.
- $V_{DDL}$  must not exceed 1.9 V, and  $V_{DDH}$  must not exceed 3.465.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 2 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power-on reset, and the 1N5820 diodes regulate the maximum potential difference on power-down.

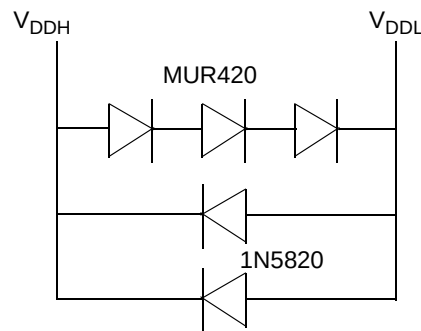


Figure 2. Example Voltage Sequencing Circuit

## 10 Mandatory Reset Configurations

The MPC852T requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, by asserting the  $\overline{RSTCONF}$  during  $\overline{HRESET}$  assertion, the HRCW[DBGC] value that is needed to be set to binary X1 in the hardware reset configuration word (HRCW) and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset.

If hardware reset configuration word (HRCW) is disabled, by negating the  $\overline{RSTCONF}$  during the  $\overline{HRESET}$  assertion, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAP, PBDIR, PCPAR, and PCDIR should be configured with the mandatory value in [Table 6](#) in the boot code after the reset deasserts.

**Table 6. Mandatory Reset Configuration of MPC852T**

| Register/Configuration                        | Field                                     | Value (binary) |
|-----------------------------------------------|-------------------------------------------|----------------|
| HRCW<br>(Hardware reset configuration word)   | HRCW[DBGC]                                | X1             |
| SIUMCR<br>(SIU module configuration register) | SIUMCR[DBGC]                              | X1             |
| MBMR<br>(Machine B mode register)             | MBMR[GPLB4DIS]                            | 0              |
| PAPAR<br>(Port A pin assignment register)     | PAPAR[4-7]<br>PAPAR[12-15]                | 0              |
| PADIR<br>(Port A Data Direction Register)     | PADIR[4-7]<br>PADIR[12-15]                | 1              |
| PBPAP<br>(Port B Pin Assignment Register)     | PBPAP[14]<br>PBPAP[16-23]<br>PBPAP[26-27] | 0              |
| PBDIR<br>(Port B Data Direction Register)     | PBDIR[14]<br>PBDIR[16-23]<br>PBDIR[26-27] | 1              |
| PCPAR<br>(Port C Pin Assignment Register)     | PCPAR[8-11]<br>PCDIR[14]                  | 0              |
| PCDIR<br>(Port C Data Direction Register)     | PCDIR[8-11]<br>PCDIR[14]                  | 1              |

## 11 Layout Practices

Each  $V_{DD}$  pin on the MPC852T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The  $V_{DD}$  power supply should be bypassed to ground using at least four 0.1  $\mu$ F by-pass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed circuit traces connecting to chip  $V_{DD}$  and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as  $V_{DD}$  and GND planes should be used.

All output pins on the MPC852T have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize undershoot and reflections that these fast output switching times cause. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances that the PC traces cause. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads, because these loads create higher transient currents in the  $V_{DD}$  and GND circuits. Pull up all unused inputs or signals that are inputs during reset. Special care should be taken to minimize the noise levels on the PLL

supply pins. For more information, please refer to *MPC866 User's Manual*, Section 14.4.3, "Clock Synthesizer Power ( $V_{DDSYN}$ ,  $V_{SSSYN}$ ,  $V_{SSSYN1}$ )."

## 12 Bus Signal Timing

The maximum bus speed that the MPC852T supports is 66 MHz. [Table 7](#) shows the frequency ranges for standard part frequencies.

**Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)**

| Part Freq | 50MHz |     | 66MHz |       |
|-----------|-------|-----|-------|-------|
|           | Min   | Max | Min   | Max   |
| Core Freq | 40    | 50  | 40    | 66.67 |
| Bus Freq  | 40    | 50  | 40    | 66.67 |

**Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)**

| Part Freq    | 50MHz |     | 66MHz |       | 80MHz |     | 100MHz |     |
|--------------|-------|-----|-------|-------|-------|-----|--------|-----|
|              | Min   | Max | Min   | Max   | Min   | Max | Min    | Max |
| Core Freq    | 40    | 50  | 40    | 66.67 | 40    | 80  | 40     | 100 |
| Bus Freq 2:1 | 20    | 25  | 20    | 33.33 | 20    | 40  | 20     | 50  |

[Table 9](#) provides the bus operation timing for the MPC852T at 33, 40, 50 and 66 MHz.

The timing for the MPC852T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay

**Table 9. Bus Operation Timings**

| Num | Characteristic                                                                                                                                                                                                                                                                                            | 33 MHz |      | 40 MHz |      | 50 MHz |      | 66 MHz |      | Unit |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------|--------|------|--------|------|--------|------|------|
|     |                                                                                                                                                                                                                                                                                                           | Min    | Max  | Min    | Max  | Min    | Max  | Min    | Max  |      |
| B1  | Bus period (CLKOUT) See <a href="#">Table 7</a>                                                                                                                                                                                                                                                           | —      | —    | —      | —    | —      | —    | —      | —    | ns   |
| B1a | EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew. | -2     | +2   | -2     | +2   | -2     | +2   | -2     | +2   | ns   |
| B1b | CLKOUT frequency jitter peak-to-peak                                                                                                                                                                                                                                                                      | —      | 1    | —      | 1    | —      | 1    | —      | 1    | ns   |
| B1c | Frequency jitter on EXTCLK <sup>1</sup>                                                                                                                                                                                                                                                                   | —      | 0.50 | —      | 0.50 | —      | 0.50 | —      | 0.50 | %    |

Table 9. Bus Operation Timings (continued)

| Num  | Characteristic                                                                                                                   | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|------|----------------------------------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|      |                                                                                                                                  | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| B1d  | CLKOUT phase jitter peak-to-peak for OSCLK $\geq$ 15 MHz                                                                         | —      | 4     | —      | 4     | —      | 4     | —      | 4     | ns   |
|      | CLKOUT phase jitter peak-to-peak for OSCLK $<$ 15 MHz                                                                            | —      | 5     | —      | 5     | —      | 5     | —      | 5     | ns   |
| B2   | CLKOUT pulse width low (MIN = $0.4 \times B1$ , MAX = $0.6 \times B1$ )                                                          | 12.1   | 18.2  | 10.0   | 15.0  | 8.0    | 12.0  | 6.1    | 9.1   | ns   |
| B3   | CLKOUT pulse width high (MIN = $0.4 \times B1$ , MAX = $0.6 \times B1$ )                                                         | 12.1   | 18.2  | 10.0   | 15.0  | 8.0    | 12.0  | 6.1    | 9.1   | ns   |
| B4   | CLKOUT rise time                                                                                                                 | —      | 4.00  | —      | 4.00  | —      | 4.00  | —      | 4.00  | ns   |
| B5   | CLKOUT fall time                                                                                                                 | —      | 4.00  | —      | 4.00  | —      | 4.00  | —      | 4.00  | ns   |
| B7   | CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3) output hold (MIN = $0.25 \times B1$ )                            | 7.60   | —     | 6.30   | —     | 5.00   | —     | 3.80   | —     | ns   |
| B7a  | CLKOUT to TSIZ(0:1), REG, RSV, BDIP, PTR output hold (MIN = $0.25 \times B1$ )                                                   | 7.60   | —     | 6.30   | —     | 5.00   | —     | 3.80   | —     | ns   |
| B7b  | CLKOUT to BR, BG, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), STS output hold (MIN = $0.25 \times B1$ )                          | 7.60   | —     | 6.30   | —     | 5.00   | —     | 3.80   | —     | ns   |
| B8   | CLKOUT to A(0:31), BADDR(28:30) RD/WR, BURST, D(0:31), DP(0:3) valid (MAX = $0.25 \times B1 + 6.3$ )                             | —      | 13.80 | —      | 12.50 | —      | 11.30 | —      | 10.00 | ns   |
| B8a  | CLKOUT to TSIZ(0:1), REG, RSV, BDIP, PTR valid (MAX = $0.25 \times B1 + 6.3$ )                                                   | —      | 13.80 | —      | 12.50 | —      | 11.30 | —      | 10.00 | ns   |
| B8b  | CLKOUT to BR, BG, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), STS Valid <sup>3</sup> (MAX = $0.25 \times B1 + 6.3$ )            | —      | 13.80 | —      | 12.50 | —      | 11.30 | —      | 10.00 | ns   |
| B9   | CLKOUT to A(0:31), BADDR(28:30), RD/WR, BURST, D(0:31), DP(0:3), TSIZ(0:1), REG, RSV, PTR High-Z (MAX = $0.25 \times B1 + 6.3$ ) | 7.60   | 13.80 | 6.30   | 12.50 | 5.00   | 11.30 | 3.80   | 10.00 | ns   |
| B11  | CLKOUT to TS, BB assertion (MAX = $0.25 \times B1 + 6.0$ )                                                                       | 7.60   | 13.60 | 6.30   | 12.30 | 5.00   | 11.00 | 3.80   | 9.80  | ns   |
| B11a | CLKOUT to TA, BI assertion (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.30^2$ )         | 2.50   | 9.30  | 2.50   | 9.30  | 2.50   | 9.30  | 2.50   | 9.80  | ns   |
| B12  | CLKOUT to TS, BB negation (MAX = $0.25 \times B1 + 4.8$ )                                                                        | 7.60   | 12.30 | 6.30   | 11.00 | 5.00   | 9.80  | 3.80   | 8.50  | ns   |
| B12a | CLKOUT to TA, BI negation (when driven by the memory controller or PCMCIA interface) (MAX = $0.00 \times B1 + 9.00$ )            | 2.50   | 9.00  | 2.50   | 9.00  | 2.50   | 9.00  | 2.50   | 9.00  | ns   |
| B13  | CLKOUT to TS, BB High-Z (MIN = $0.25 \times B1$ )                                                                                | 7.60   | 21.60 | 6.30   | 20.30 | 5.00   | 19.00 | 3.80   | 14.00 | ns   |

Table 9. Bus Operation Timings (continued)

| Num  | Characteristic                                                                                                                                                                       | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|      |                                                                                                                                                                                      | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| B13a | CLKOUT to $\overline{TA}$ , $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = $0.00 \times B1 + 2.5$ )                                        | 2.50   | 15.00 | 2.50   | 15.00 | 2.50   | 15.00 | 2.50   | 15.00 | ns   |
| B14  | CLKOUT to $\overline{TEA}$ assertion (MAX = $0.00 \times B1 + 9.00$ )                                                                                                                | 2.50   | 9.00  | 2.50   | 9.00  | 2.50   | 9.00  | 2.50   | 9.00  | ns   |
| B15  | CLKOUT to $\overline{TEA}$ High-Z (MIN = $0.00 \times B1 + 2.50$ )                                                                                                                   | 2.50   | 15.00 | 2.50   | 15.00 | 2.50   | 15.00 | 2.50   | 15.00 | ns   |
| B16  | $\overline{TA}$ , $\overline{BI}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 6.00$ )                                                                                      | 6.00   | —     | 6.00   | —     | 6.00   | —     | 6.00   | —     | ns   |
| B16a | $\overline{TEA}$ , $\overline{KR}$ , $\overline{RETRY}$ , $\overline{CR}$ valid to CLKOUT (setup time) (MIN = $0.00 \times B1 + 4.5$ )                                               | 4.50   | —     | 4.50   | —     | 4.50   | —     | 4.50   | —     | ns   |
| B16b | $\overline{BB}$ , $\overline{BG}$ , $\overline{BR}$ , valid to CLKOUT (setup time) <sup>3</sup> (4MIN = $0.00 \times B1 + .000$ )                                                    | 4.00   | —     | 4.00   | —     | 4.00   | —     | 4.00   | —     | ns   |
| B17  | CLKOUT to $\overline{TA}$ , $\overline{TEA}$ , $\overline{BI}$ , $\overline{BB}$ , $\overline{BG}$ , $\overline{BR}$ valid (hold time) (MIN = $0.00 \times B1 + 1.00$ <sup>4</sup> ) | 1.00   | —     | 1.00   | —     | 1.00   | —     | 2.00   | —     | ns   |
| B17a | CLKOUT to $\overline{KR}$ , $\overline{RETRY}$ , $\overline{CR}$ valid (hold time) (MIN = $0.00 \times B1 + 2.00$ )                                                                  | 2.00   | —     | 2.00   | —     | 2.00   | —     | 2.00   | —     | ns   |
| B18  | D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) <sup>5</sup> (MIN = $0.00 \times B1 + 6.00$ )                                                                              | 6.00   | —     | 6.00   | —     | 6.00   | —     | 6.00   | —     | ns   |
| B19  | CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) <sup>5</sup> (MIN = $0.00 \times B1 + 1.00$ <sup>6</sup> )                                                                  | 1.00   | —     | 1.00   | —     | 1.00   | —     | 2.00   | —     | ns   |
| B20  | D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) <sup>7</sup> (MIN = $0.00 \times B1 + 4.00$ )                                                                             | 4.00   | —     | 4.00   | —     | 4.00   | —     | 4.00   | —     | ns   |
| B21  | CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) <sup>7</sup> (MIN = $0.00 \times B1 + 2.00$ )                                                                              | 2.00   | —     | 2.00   | —     | 2.00   | —     | 2.00   | —     | ns   |
| B22  | CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = $0.25 \times B1 + 6.3$ )                                                                                         | 7.60   | 13.80 | 6.30   | 12.50 | 5.00   | 11.30 | 3.80   | 10.00 | ns   |
| B22a | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = $0.00 \times B1 + 8.00$ )                                                                             | —      | 8.00  | —      | 8.00  | —      | 8.00  | —      | 8.00  | ns   |
| B22b | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = $0.25 \times B1 + 6.3$ )                                                                    | 7.60   | 13.80 | 6.30   | 12.50 | 5.00   | 11.30 | 3.80   | 10.00 | ns   |
| B22c | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$ )                                                                   | 10.90  | 18.00 | 10.90  | 16.00 | 7.00   | 14.10 | 5.20   | 12.30 | ns   |
| B23  | CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = $0.00 \times B1 + 8.00$ )                                     | 2.00   | 8.00  | 2.00   | 8.00  | 2.00   | 8.00  | 2.00   | 8.00  | ns   |

Table 9. Bus Operation Timings (continued)

| Num  | Characteristic                                                                                                                                                                    | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|      |                                                                                                                                                                                   | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| B24  | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted<br>GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)                                                                          | 5.60   | —     | 4.30   | —     | 3.00   | —     | 1.80   | —     | ns   |
| B24a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted<br>GPCM ACS = 11 TRLX = 0 (MIN = 0.50 x B1 - 2.00)                                                                           | 13.20  | —     | 10.50  | —     | 8.00   | —     | 5.60   | —     | ns   |
| B25  | CLKOUT rising edge to $\overline{OE}$ ,<br>$\overline{WE}(0:3)/BS\_B[0:3]$ asserted (MAX = 0.00 x B1 + 9.00)                                                                      | —      | 9.00  |        | 9.00  |        | 9.00  |        | 9.00  | ns   |
| B26  | CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00)                                                                                                            | 2.00   | 9.00  | 2.00   | 9.00  | 2.00   | 9.00  | 2.00   | 9.00  | ns   |
| B27  | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted<br>GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)                                                                          | 35.90  | —     | 29.30  | —     | 23.00  | —     | 16.90  | —     | ns   |
| B27a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted<br>GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)                                                                          | 43.50  | —     | 35.50  | —     | 28.00  | —     | 20.70  | —     | ns   |
| B28  | CLKOUT rising edge to $\overline{WE}(0:3)/BS\_B[0:3]$<br>negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)                                                              | —      | 9.00  | —      | 9.00  | —      | 9.00  | —      | 9.00  | ns   |
| B28a | CLKOUT falling edge to $\overline{WE}(0:3)/BS\_B[0:3]$<br>negated GPCM write access TRLX = 0,1<br>CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)                                     | 7.60   | 14.30 | 6.30   | 13.00 | 5.00   | 11.80 | 3.80   | 10.50 | ns   |
| B28b | CLKOUT falling edge to $\overline{CS}$ negated GPCM<br>write access TRLX = 0,1 CSNT = 1 ACS = 10<br>or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)                                | —      | 14.30 | —      | 13.00 | —      | 11.80 | —      | 10.50 | ns   |
| B28c | CLKOUT falling edge to $\overline{WE}(0:3)/BS\_B[0:3]$<br>negated GPCM write access TRLX = 0,1<br>CSNT = 1 write access TRLX = 0,1 CSNT = 1,<br>EBDF = 1 (MAX = 0.375 x B1 + 6.6) | 10.90  | 18.00 | 10.90  | 18.00 | 7.00   | 14.30 | 5.20   | 12.30 | ns   |
| B28d | CLKOUT falling edge to $\overline{CS}$ negated GPCM<br>write access TRLX = 0,1 CSNT = 1, ACS = 10,<br>or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)                              | —      | 18.00 | —      | 18.00 | —      | 14.30 | —      | 12.30 | ns   |
| B29  | $\overline{WE}(0:3)/BS\_B[0:3]$ negated to D(0:31),<br>DP(0:3) High-Z GPCM write access, CSNT = 0,<br>EBDF = 0 (MIN = 0.25 x B1 - 2.00)                                           | 5.60   | —     | 4.30   | —     | 3.00   | —     | 1.80   | —     | ns   |
| B29a | $\overline{WE}(0:3)/BS\_B[0:3]$ negated to D(0:31),<br>DP(0:3) High-Z GPCM write access, TRLX = 0,<br>CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)                                 | 13.20  | —     | 10.50  | —     | 8.00   | —     | 5.60   | —     | ns   |



Table 9. Bus Operation Timings (continued)

| Num  | Characteristic                                                                                                                                                                                                                                                        | 33 MHz |     | 40 MHz |     | 50 MHz |     | 66 MHz |     | Unit |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|--------|-----|--------|-----|--------|-----|------|
|      |                                                                                                                                                                                                                                                                       | Min    | Max | Min    | Max | Min    | Max | Min    | Max |      |
| B29b | $\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1 - 2.00)                                                                                                                                       | 5.60   | —   | 4.30   | —   | 3.00   | —   | 1.80   | —   | ns   |
| B29c | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00)                                                                                                                     | 13.20  | —   | 10.50  | —   | 8.00   | —   | 5.60   | —   | ns   |
| B29d | $\overline{WE}(0:3)/BS\_B[0:3]$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00)                                                                                                                           | 43.50  | —   | 35.50  | —   | 28.00  | —   | 20.70  | —   | ns   |
| B29e | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)                                                                                                                     | 43.50  | —   | 35.50  | —   | 28.00  | —   | 20.70  | —   | ns   |
| B29f | $\overline{WE}(0:3)/BS\_B[0:3]$ negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30)                                                                                                                          | 5.00   | —   | 3.00   | —   | 1.10   | —   | 0.00   | —   | ns   |
| B29g | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 6.30)                                                                                                                     | 5.00   | —   | 3.00   | —   | 1.10   | —   | 0.00   | —   | ns   |
| B29h | $\overline{WE}(0:3)/BS\_B[0:3]$ negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30)                                                                                                                          | 38.40  | —   | 31.10  | —   | 24.20  | —   | 17.50  | —   | ns   |
| B29i | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30)                                                                                                                    | 38.40  | —   | 31.10  | —   | 24.20  | —   | 17.50  | —   | ns   |
| B30  | $\overline{CS}$ , $\overline{WE}(0:3)/BS\_B[0:3]$ negated to A(0:31), BADDR(28:30) Invalid GPCM write access <sup>8</sup> (MIN = 0.25 x B1 - 2.00)                                                                                                                    | 5.60   | —   | 4.30   | —   | 3.00   | —   | 1.80   | —   | ns   |
| B30a | $\overline{WE}(0:3)/BS\_B[0:3]$ negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT = 1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 - 2.00)            | 13.20  | —   | 10.50  | —   | 8.00   | —   | 5.60   | —   | ns   |
| B30b | $\overline{WE}(0:3)/BS\_B[0:3]$ negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00) | 43.50  | —   | 35.50  | —   | 28.00  | —   | 20.70  | —   | ns   |

Table 9. Bus Operation Timings (continued)

| Num  | Characteristic                                                                                                                                                                                                                                                                         | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|      |                                                                                                                                                                                                                                                                                        | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| B30c | $\overline{WE}(0:3)/\overline{BS\_B}[0:3]$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, $TRLX = 0$ , $CSNT = 1$ . $\overline{CS}$ negated to A(0:31) invalid GPCM write access, $TRLX = 0$ , $CSNT = 1$ ACS = 10, ACS == 11, EBDF = 1 (MIN = $0.375 \times B1 - 3.00$ ) | 8.40   | —     | 6.40   | —     | 4.50   | —     | 2.70   | —     | ns   |
| B30d | $\overline{WE}(0:3)/\overline{BS\_B}[0:3]$ negated to A(0:31), BADDR(28:30) invalid GPCM write access $TRLX = 1$ , $CSNT = 1$ , $\overline{CS}$ negated to A(0:31) invalid GPCM write access $TRLX = 1$ , $CSNT = 1$ , ACS = 10 or 11, EBDF = 1                                        | 38.67  | —     | 31.38  | —     | 24.50  | —     | 17.83  | —     | ns   |
| B31  | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$ )                                                                                                                                  | 1.50   | 6.00  | 1.50   | 6.00  | 1.50   | 6.00  | 1.50   | 6.00  | ns   |
| B31a | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$ )                                                                                                                                  | 7.60   | 14.30 | 6.30   | 13.00 | 5.00   | 11.80 | 3.80   | 10.50 | ns   |
| B31b | CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$ )                                                                                                                                   | 1.50   | 8.00  | 1.50   | 8.00  | 1.50   | 8.00  | 1.50   | 8.00  | ns   |
| B31c | CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.30$ )                                                                                                                                   | 7.60   | 13.80 | 6.30   | 12.50 | 5.00   | 11.30 | 3.80   | 10.00 | ns   |
| B31d | CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = $0.375 \times B1 + 6.6$ )                                                                                                                          | 13.30  | 18.00 | 11.30  | 16.00 | 9.40   | 14.10 | 7.60   | 12.30 | ns   |
| B32  | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$ )                                                                                                                                  | 1.50   | 6.00  | 1.50   | 6.00  | 1.50   | 6.00  | 1.50   | 6.00  | ns   |
| B32a | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$ )                                                                                                                        | 7.60   | 14.30 | 6.30   | 13.00 | 5.00   | 11.80 | 3.80   | 10.50 | ns   |
| B32b | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$ )                                                                                                                                   | 1.50   | 8.00  | 1.50   | 8.00  | 1.50   | 8.00  | 1.50   | 8.00  | ns   |
| B32c | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$ )                                                                                                                                   | 7.60   | 14.30 | 6.30   | 13.00 | 5.00   | 11.80 | 3.80   | 10.50 | ns   |

Table 9. Bus Operation Timings (continued)

| Num  | Characteristic                                                                                                                                                        | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|      |                                                                                                                                                                       | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| B32d | CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, $EBDF = 1$ ( $MAX = 0.375 \times B1 + 6.60$ )    | 13.30  | 18.00 | 11.30  | 16.00 | 9.40   | 14.10 | 7.60   | 12.30 | ns   |
| B33  | CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM ( $MAX = 0.00 \times B1 + 6.00$ )               | 1.50   | 6.00  | 1.50   | 6.00  | 1.50   | 6.00  | 1.50   | 6.00  | ns   |
| B33a | CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM ( $MAX = 0.25 \times B1 + 6.80$ )                | 7.60   | 14.30 | 6.30   | 13.00 | 5.00   | 11.80 | 3.80   | 10.50 | ns   |
| B34  | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM ( $MIN = 0.25 \times B1 - 2.00$ ) | 5.60   | —     | 4.30   | —     | 3.00   | —     | 1.80   | —     | ns   |
| B34a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM ( $MIN = 0.50 \times B1 - 2.00$ ) | 13.20  | —     | 10.50  | —     | 8.00   | —     | 5.60   | —     | ns   |
| B34b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM ( $MIN = 0.75 \times B1 - 2.00$ )                 | 20.70  | —     | 16.70  | —     | 13.00  | —     | 9.40   | —     | ns   |
| B35  | A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM ( $MIN = 0.25 \times B1 - 2.00$ )              | 5.60   | —     | 4.30   | —     | 3.00   | —     | 1.80   | —     | ns   |
| B35a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM ( $MIN = 0.50 \times B1 - 2.00$ )             | 13.20  | —     | 10.50  | —     | 8.00   | —     | 5.60   | —     | ns   |
| B35b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM ( $MIN = 0.75 \times B1 - 2.00$ ) | 20.70  | —     | 16.70  | —     | 13.00  | —     | 9.40   | —     | ns   |
| B36  | A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM ( $MIN = 0.25 \times B1 - 2.00$ )  | 5.60   | —     | 4.30   | —     | 3.00   | —     | 1.80   | —     | ns   |
| B37  | UPWAIT valid to CLKOUT falling edge <sup>9</sup> ( $MIN = 0.00 \times B1 + 6.00$ )                                                                                    | 6.00   | —     | 6.00   | —     | 6.00   | —     | 6.00   | —     | ns   |
| B38  | CLKOUT falling edge to UPAWAIT valid <sup>9</sup> ( $MIN = 0.00 \times B1 + 1.00$ )                                                                                   | 1.00   | —     | 1.00   | —     | 1.00   | —     | 1.00   | —     | ns   |

Table 9. Bus Operation Timings (continued)

| Num | Characteristic                                                                         | 33 MHz |     | 40 MHz |     | 50 MHz |     | 66 MHz |     | Unit |
|-----|----------------------------------------------------------------------------------------|--------|-----|--------|-----|--------|-----|--------|-----|------|
|     |                                                                                        | Min    | Max | Min    | Max | Min    | Max | Min    | Max |      |
| B39 | $\overline{AS}$ valid to CLKOUT rising edge <sup>10</sup> (MIN = 0.00 x B1 + 7.00)     | 7.00   | —   | 7.00   | —   | 7.00   | —   | 7.00   | —   | ns   |
| B40 | A(0:31), TSIZ(0:1), RD/WR, BURST, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00) | 7.00   | —   | 7.00   | —   | 7.00   | —   | 7.00   | —   | ns   |
| B41 | $\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00)      | 7.00   | —   | 7.00   | —   | 7.00   | —   | 7.00   | —   | ns   |
| B42 | CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)       | 2.00   | —   | 2.00   | —   | 2.00   | —   | 2.00   | —   | ns   |
| B43 | $\overline{AS}$ negation to memory controller signals negation (MAX = TBD)             | —      | TBD | —      | TBD | —      | TBD | —      | TBD | ns   |

<sup>1</sup> If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the maximum allowed jitter on EXTAL can be up to 2%.

<sup>2</sup> For part speeds above 50MHz, use 9.80ns for B11a.

<sup>3</sup> The timing required for  $\overline{BR}$  input is relevant when the MPC852T is selected to work with internal bus arbiter. The timing for  $\overline{BG}$  input is relevant when the MPC852T is selected to work with external bus arbiter.

<sup>4</sup> For part speeds above 50MHz, use 2ns for B17.

<sup>5</sup> The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the  $\overline{TA}$  input signal is asserted.

<sup>6</sup> For part speeds above 50MHz, use 2ns for B19.

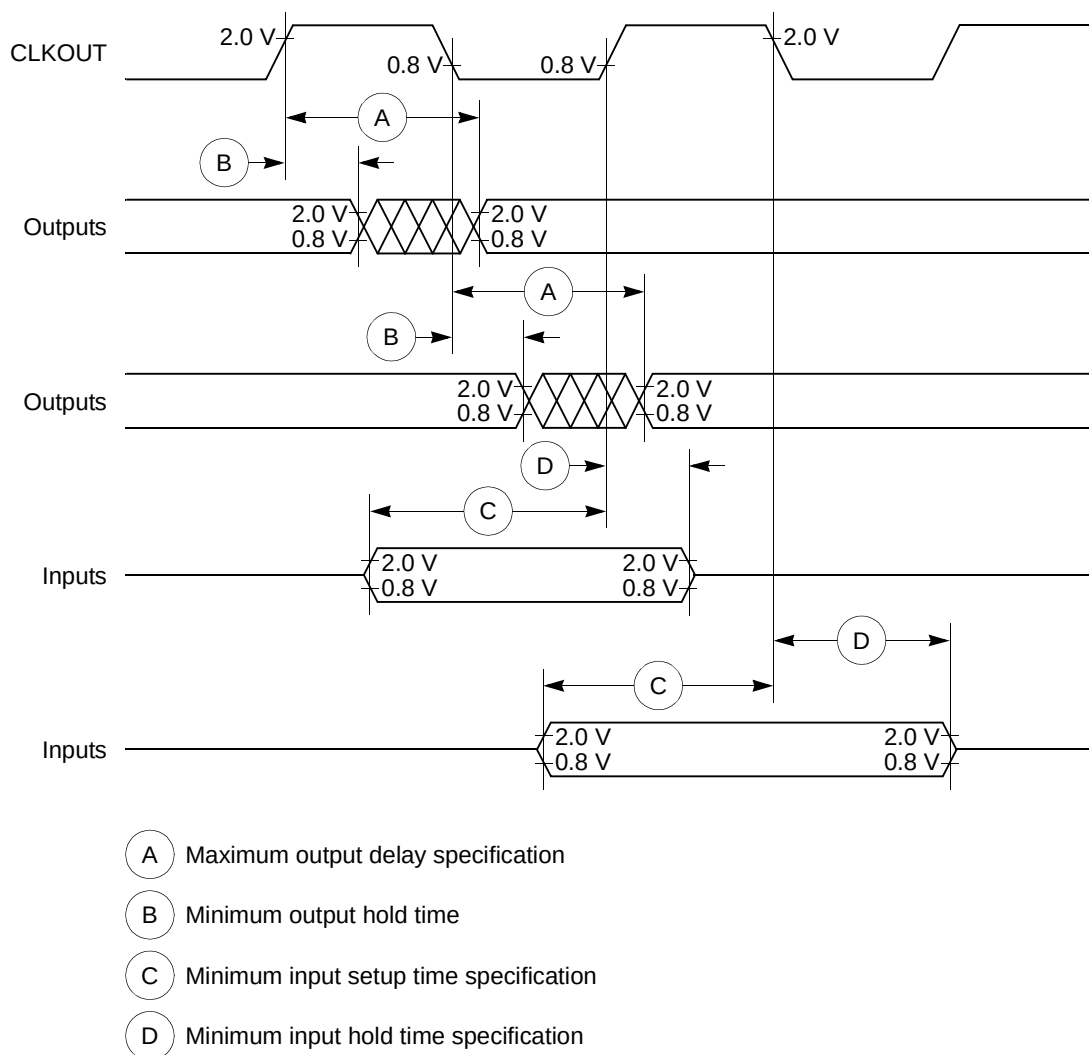
<sup>7</sup> The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

<sup>8</sup> The timing B30 refers to  $\overline{CS}$  when ACS = 00 and to  $\overline{WE}(0:3)$  when CSNT = 0.

<sup>9</sup> The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 18](#).

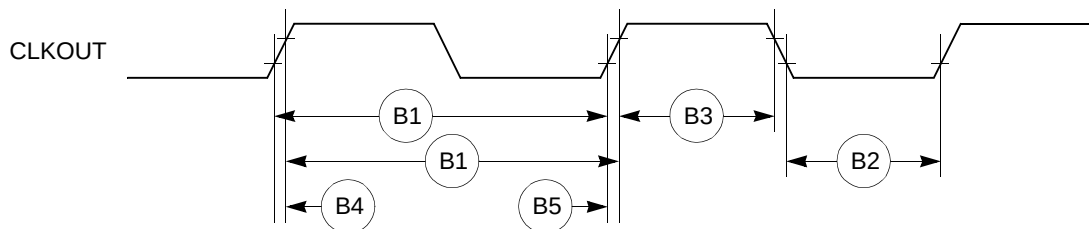
<sup>10</sup> The  $\overline{AS}$  signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 21](#).

Figure 3 is the control timing diagram.



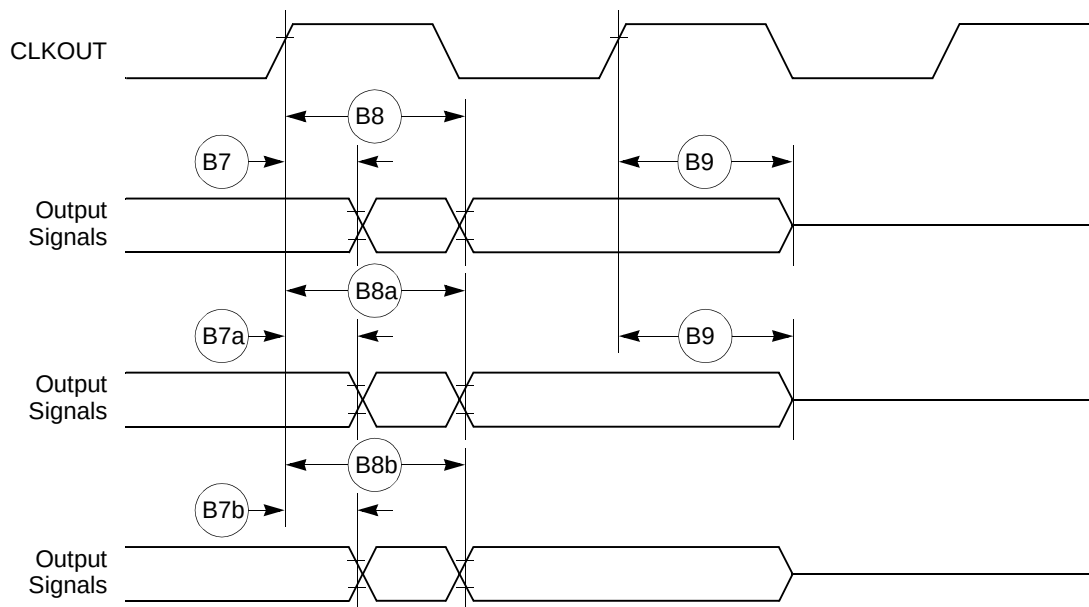
**Figure 3. Control Timing**

Figure 4 provides the timing for the external clock.



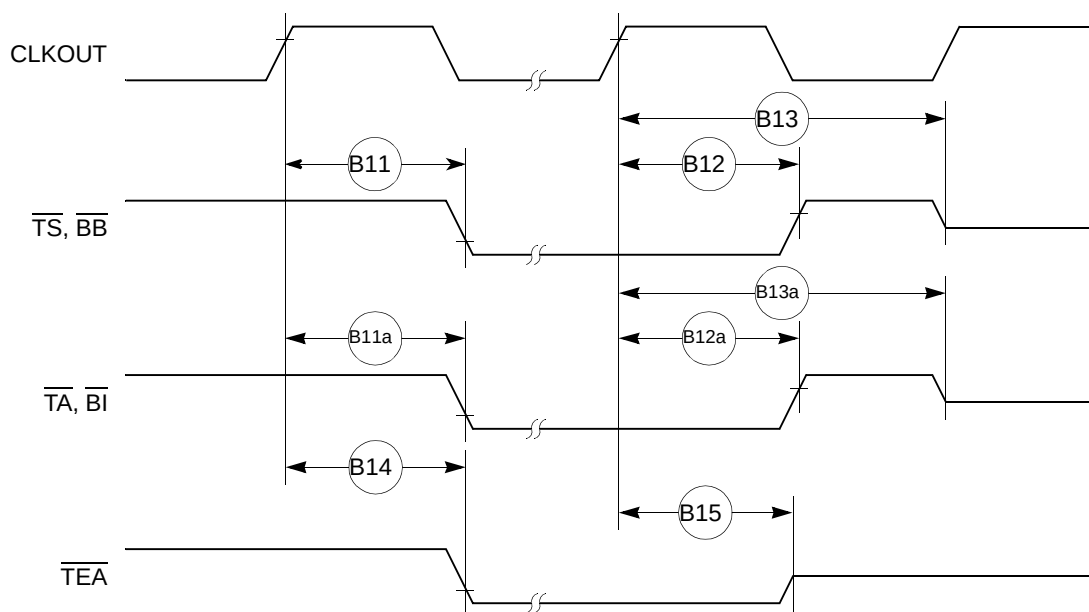
**Figure 4. External Clock Timing**

Figure 5 provides the timing for the synchronous output signals.



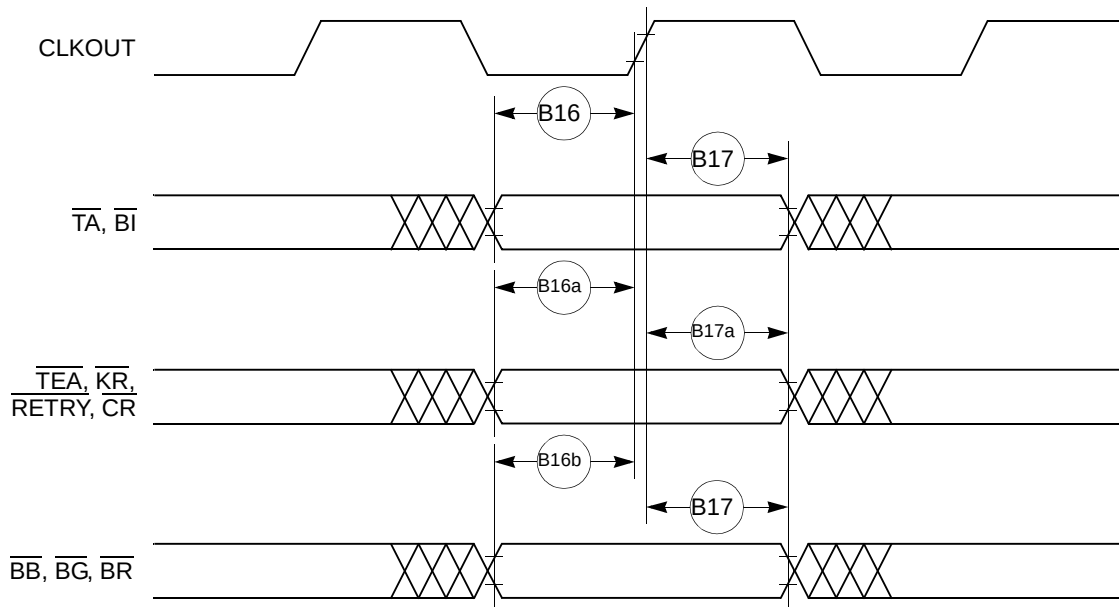
**Figure 5. Synchronous Output Signals Timing**

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.



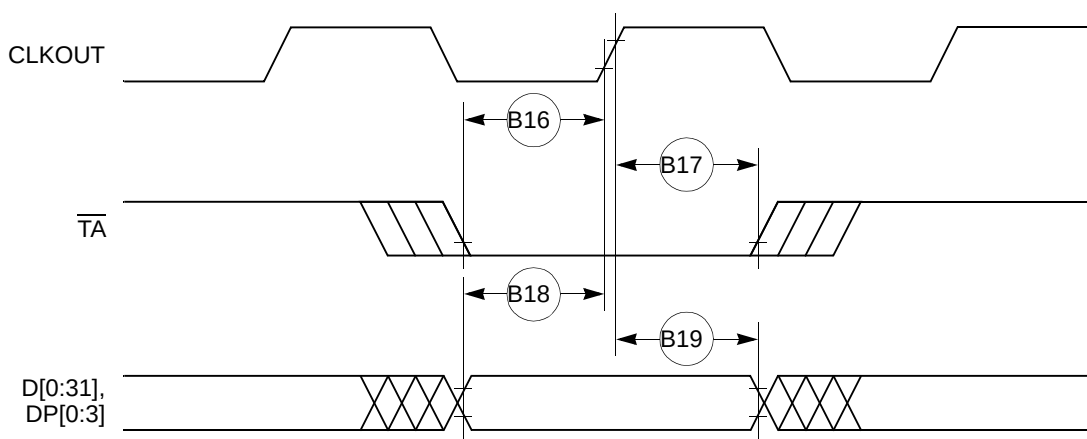
**Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing**

Figure 7 provides the timing for the synchronous input signals.



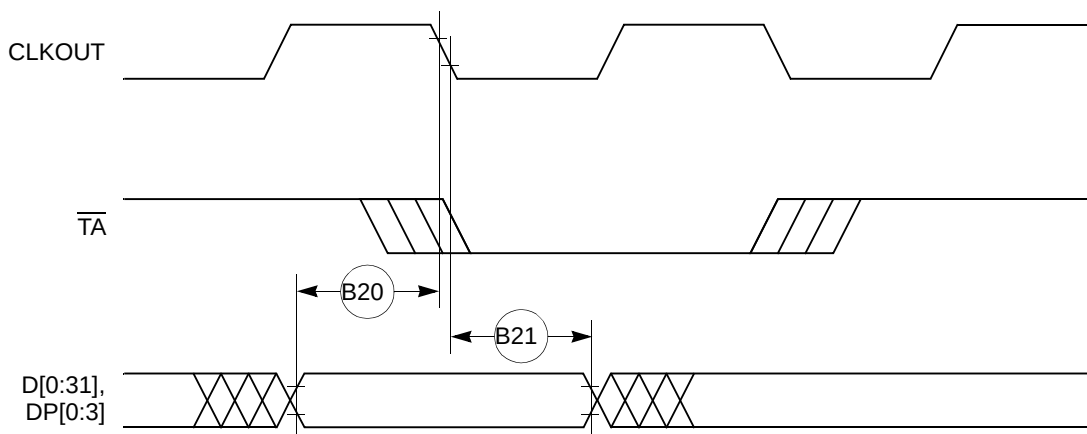
**Figure 7. Synchronous Input Signals Timing**

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.



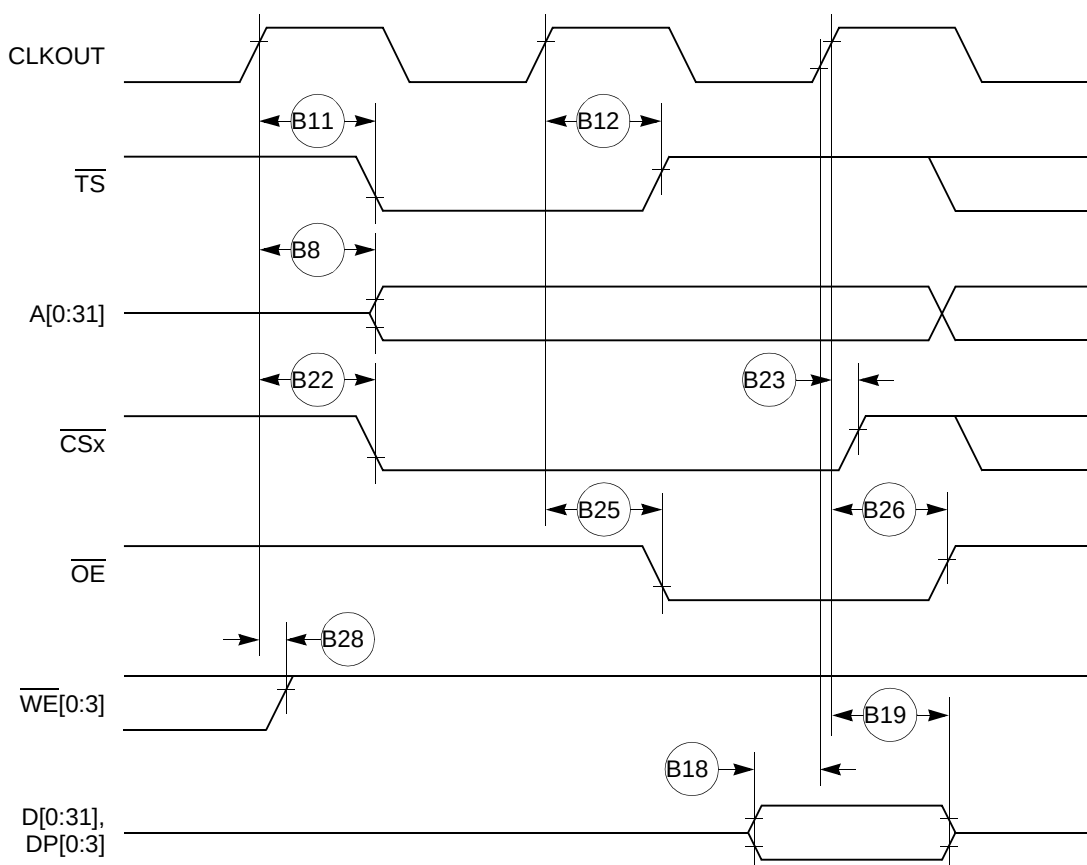
**Figure 8. Input Data Timing in Normal Case**

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)



**Figure 9. Input Data Timing When Controlled by UPM in the Memory Controller and DLT3 = 1**

Figure 10 through Figure 13 provide the timing for the external bus read that various GPCM factors control.



**Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)**



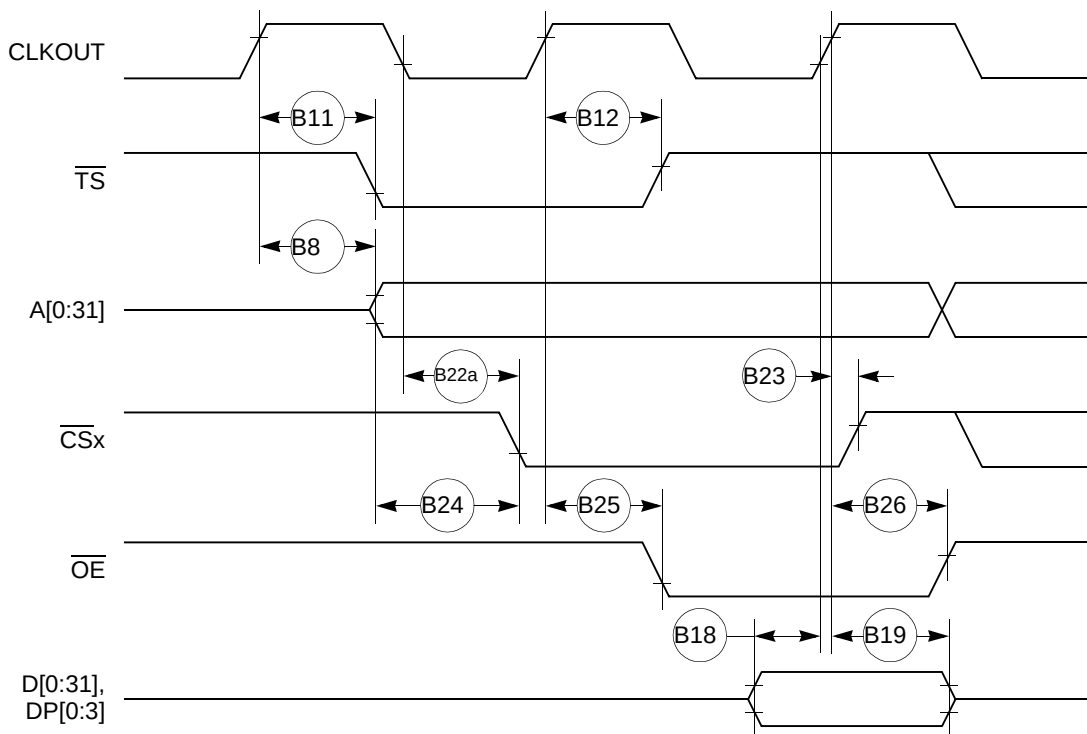


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

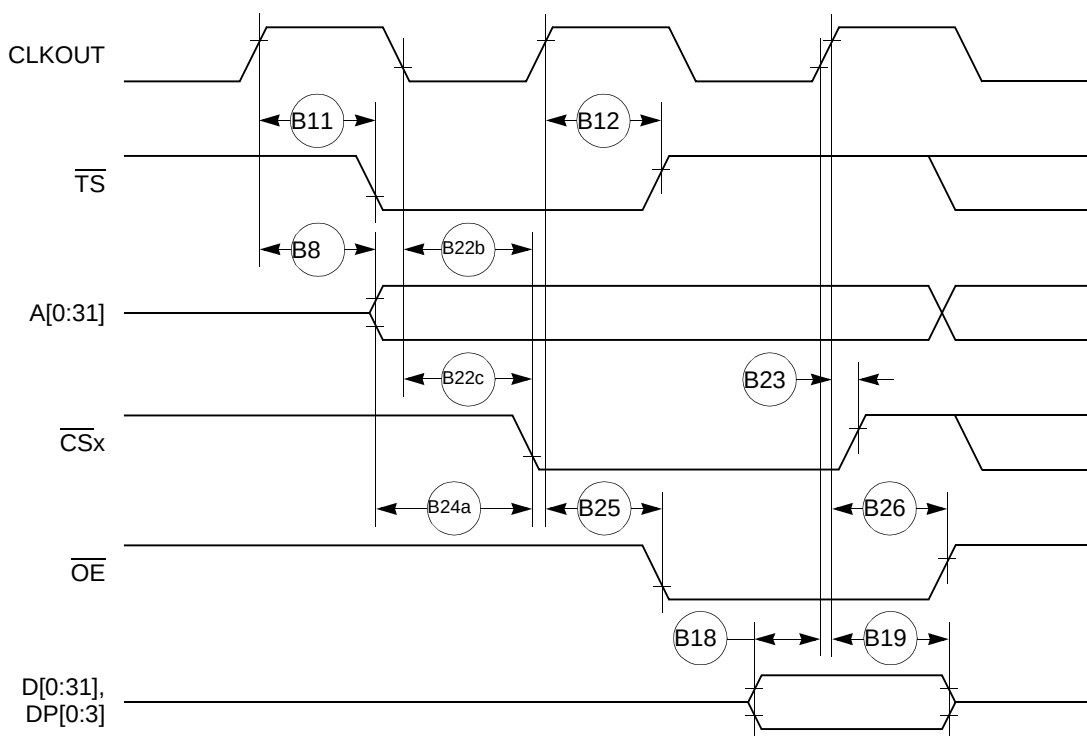


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

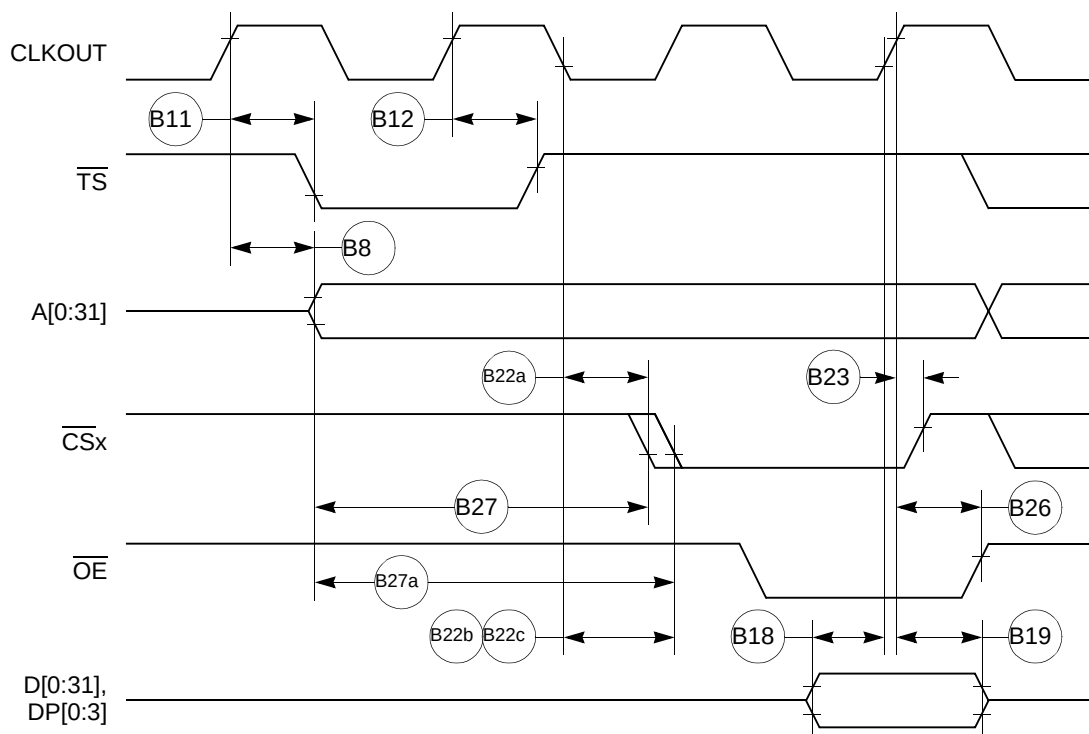


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write that various GPCM factors control.

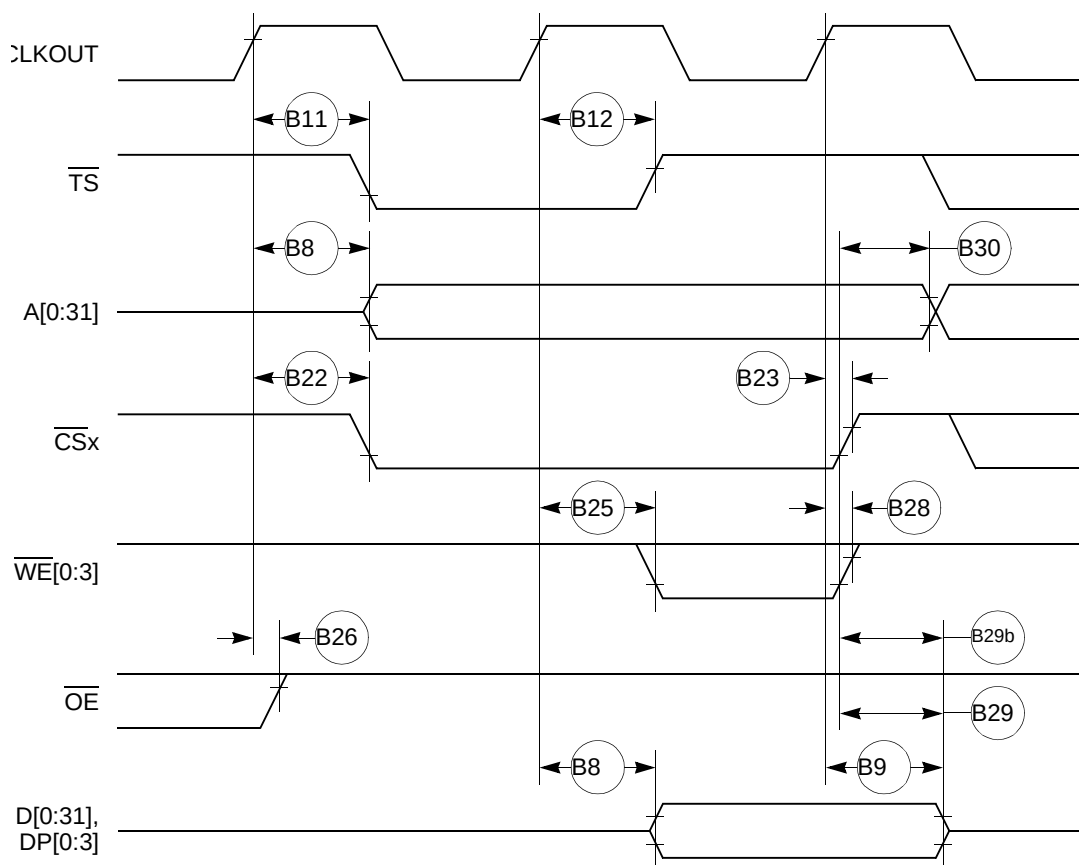


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

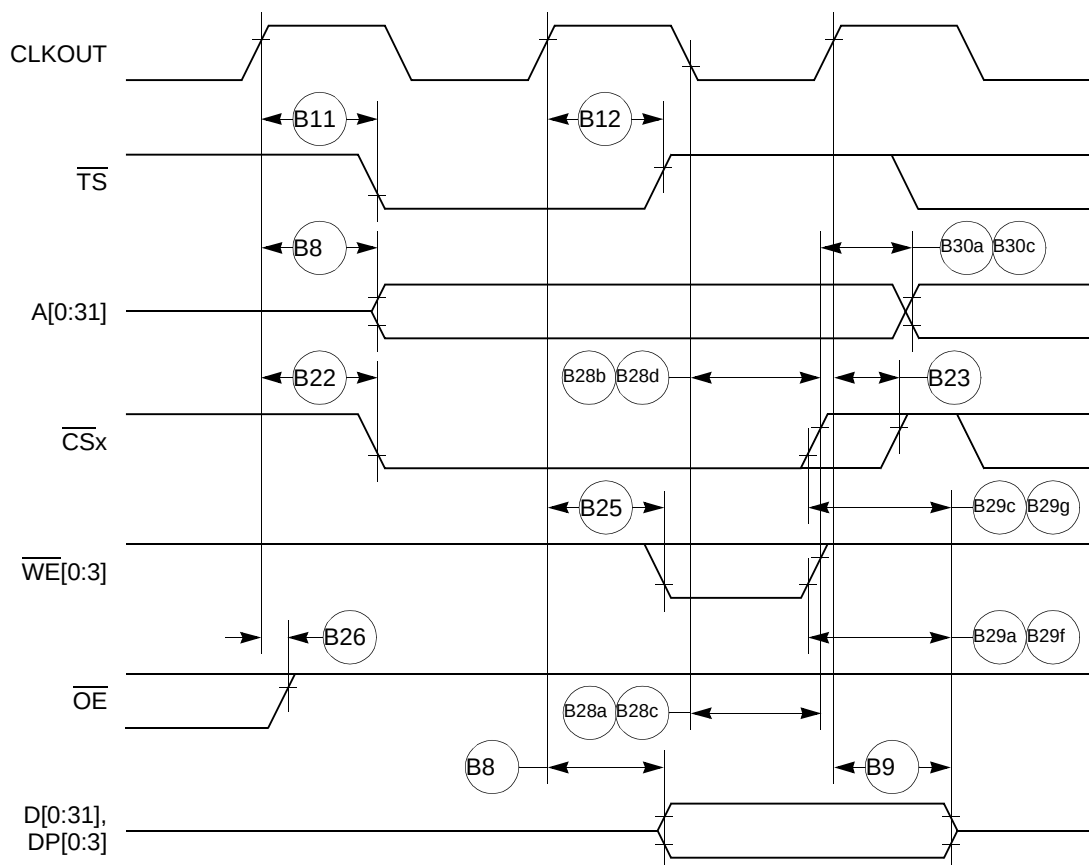


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

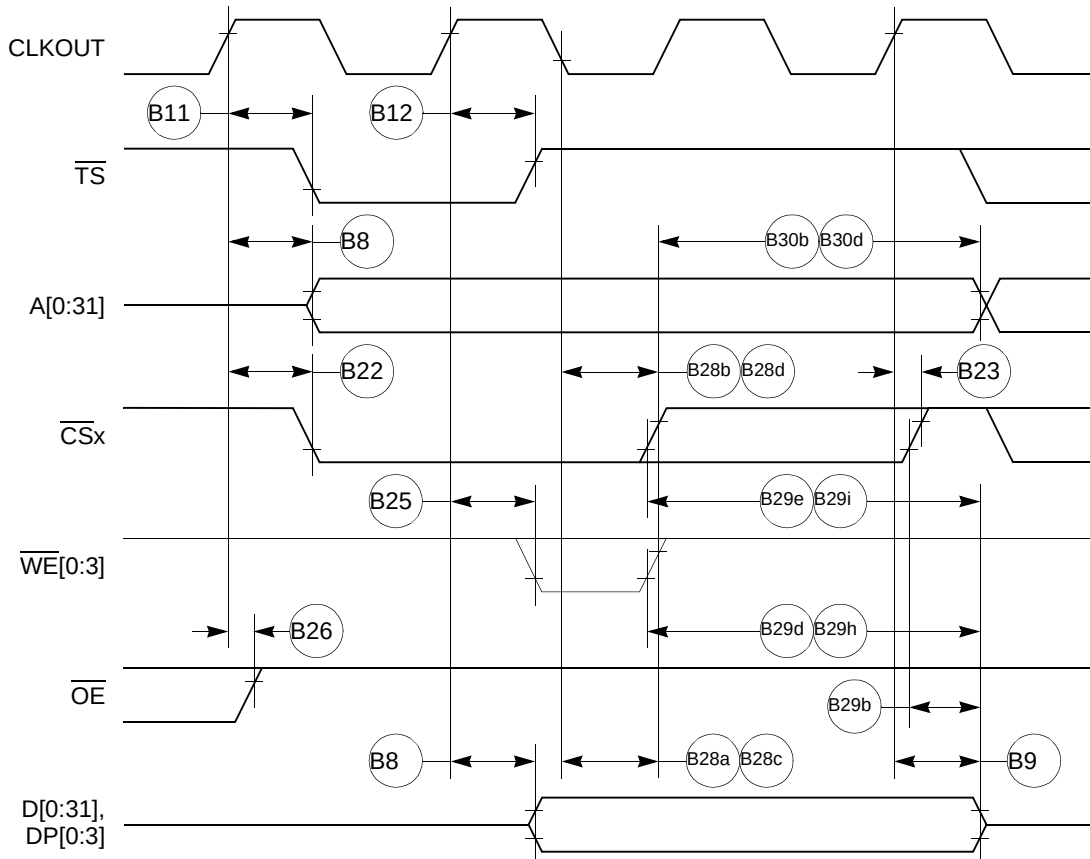


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus that the UPM controls.

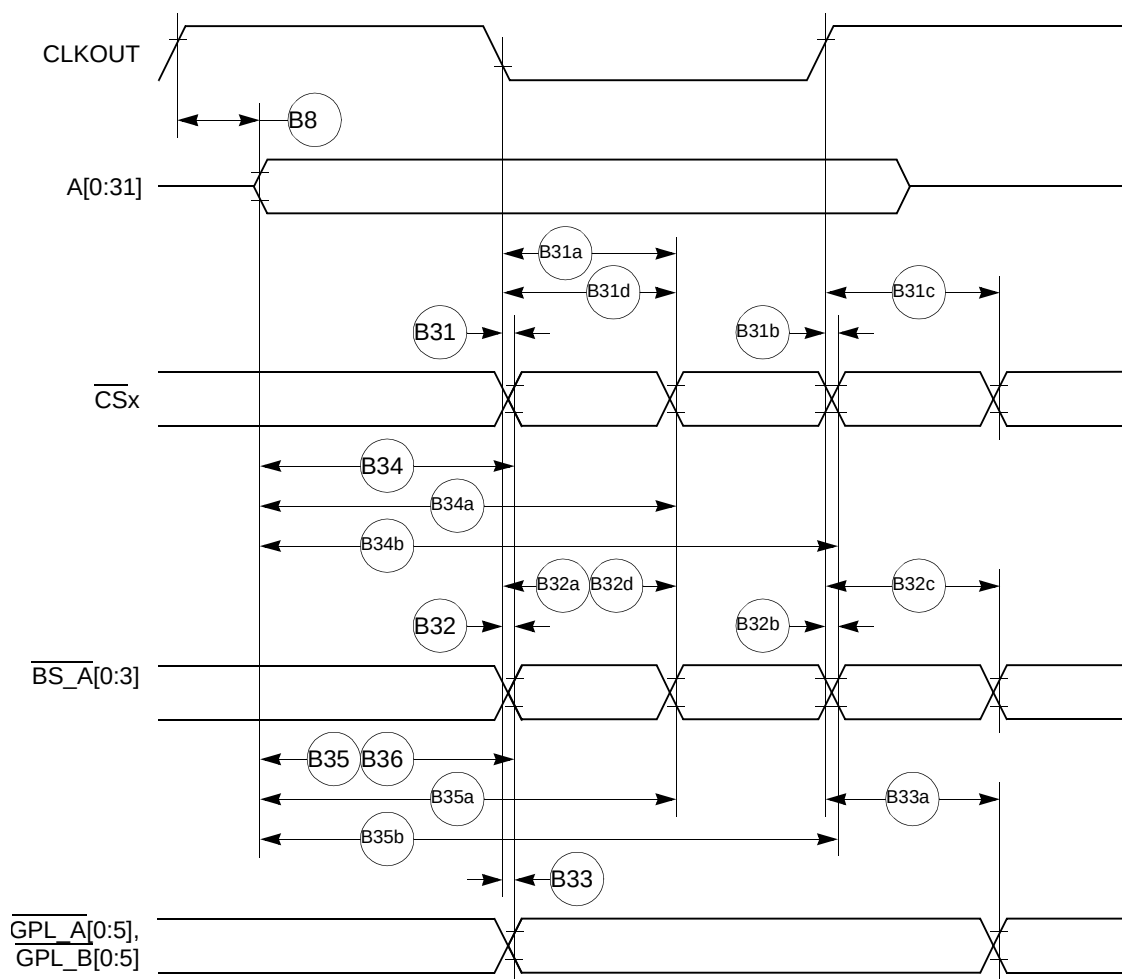
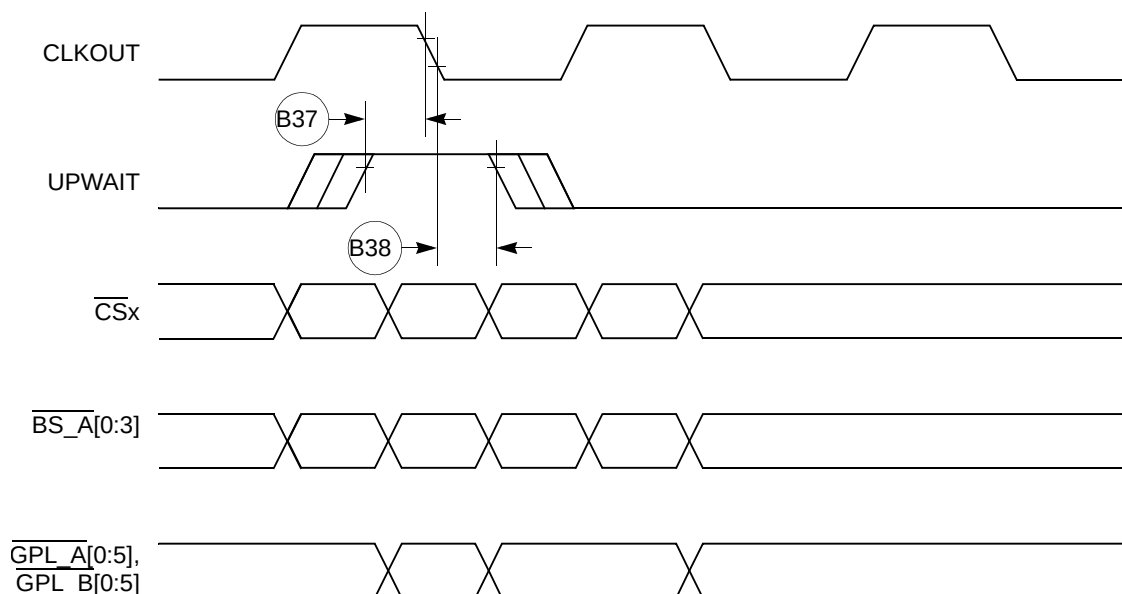


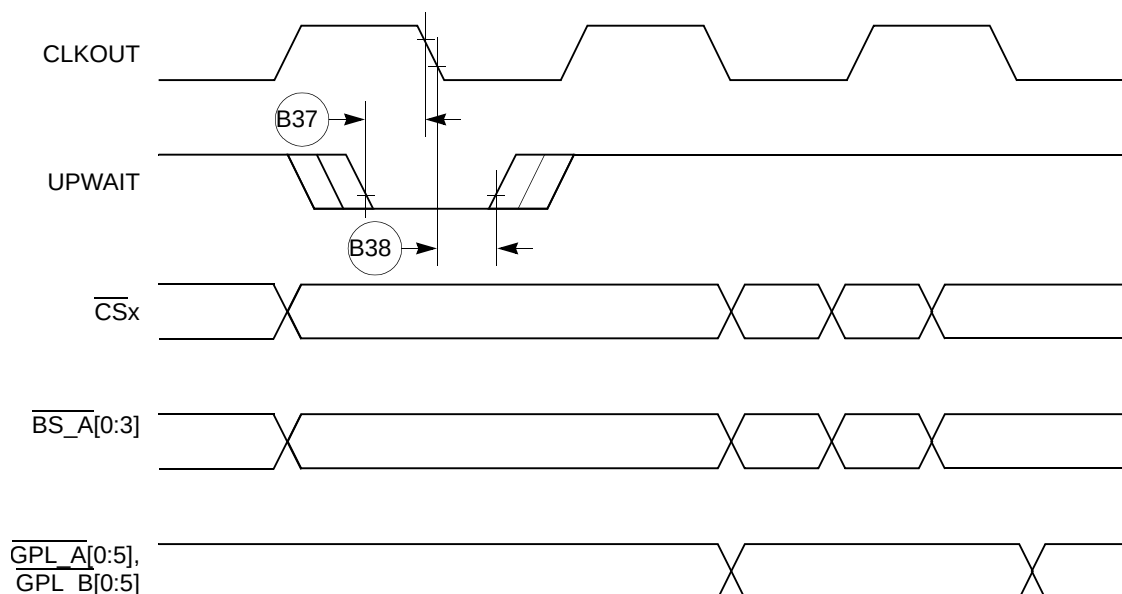
Figure 17. External Bus Timing (UPM Controlled Signals)

Figure 18 provides the timing for the asynchronous asserted UPWAIT signal that the UPM controls.



**Figure 18. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing**

Figure 19 provides the timing for the asynchronous negated UPWAIT signal that the UPM controls.



**Figure 19. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing**

Figure 20 provides the timing for the synchronous external master access that the GPCM controls.

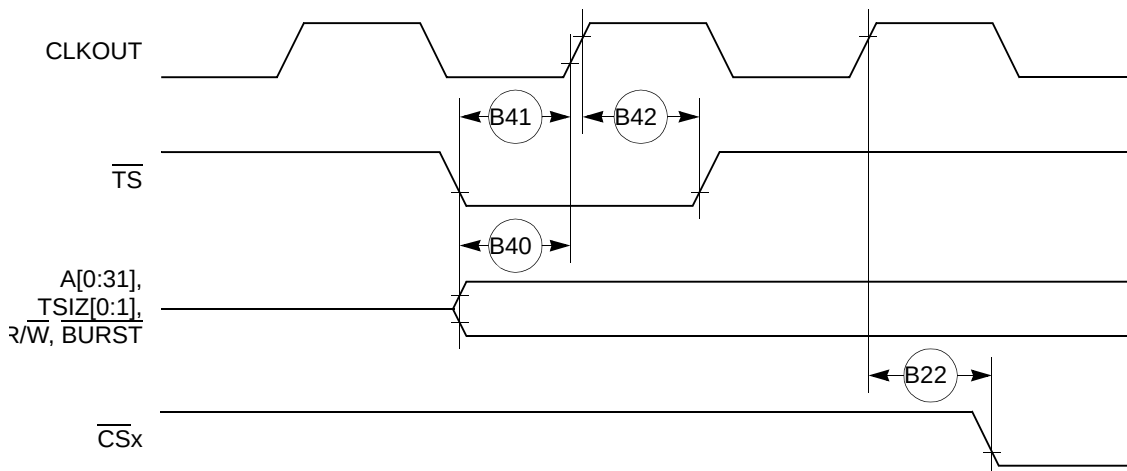


Figure 20. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access that the GPCM controls.

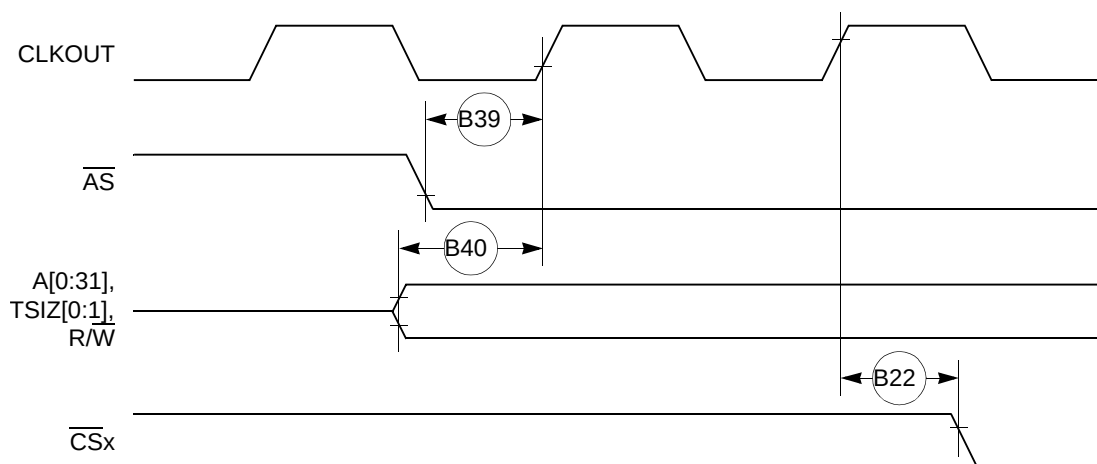


Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

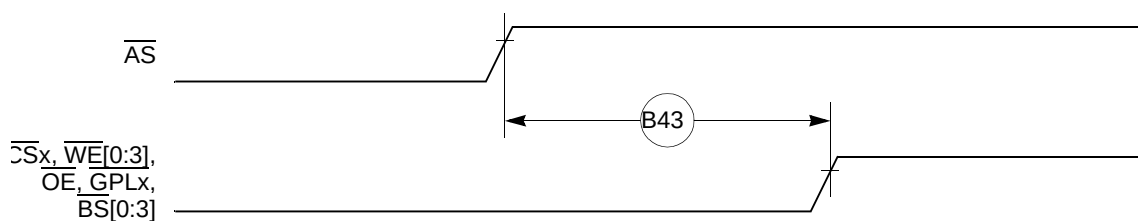


Figure 22. Asynchronous External Master—Control Signals Negation Timing



Table 10 provides interrupt timing for the MPC852T.

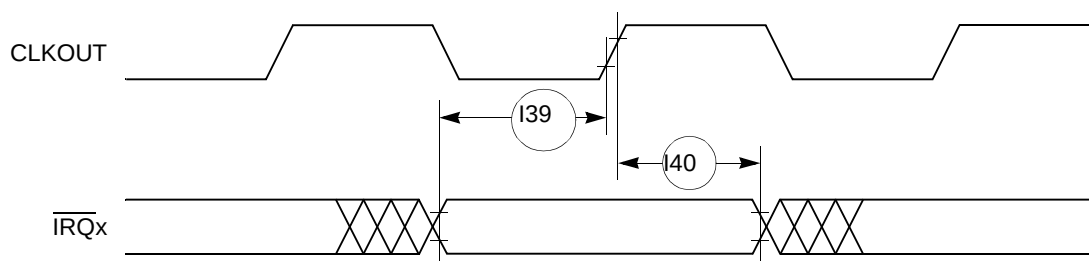
**Table 10. Interrupt Timing**

| Num | Characteristic <sup>1</sup>                                        | All Frequencies              |     | Unit |
|-----|--------------------------------------------------------------------|------------------------------|-----|------|
|     |                                                                    | Min                          | Max |      |
| I39 | $\overline{\text{IRQx}}$ valid to CLKOUT rising edge (set up time) | 6.00                         |     | ns   |
| I40 | $\overline{\text{IRQx}}$ hold time after CLKOUT                    | 2.00                         |     | ns   |
| I41 | $\overline{\text{IRQx}}$ pulse width low                           | 3.00                         |     | ns   |
| I42 | $\overline{\text{IRQx}}$ pulse width high                          | 3.00                         |     | ns   |
| I43 | $\overline{\text{IRQx}}$ edge-to-edge time                         | $4 \times T_{\text{CLKOUT}}$ |     | —    |

<sup>1</sup> The timings I39 and I40 describe the testing conditions under which the  $\overline{\text{IRQ}}$  lines are tested when being defined as level-sensitive. The  $\overline{\text{IRQ}}$  lines are synchronized internally and need not be asserted or negated with reference to the CLKOUT.

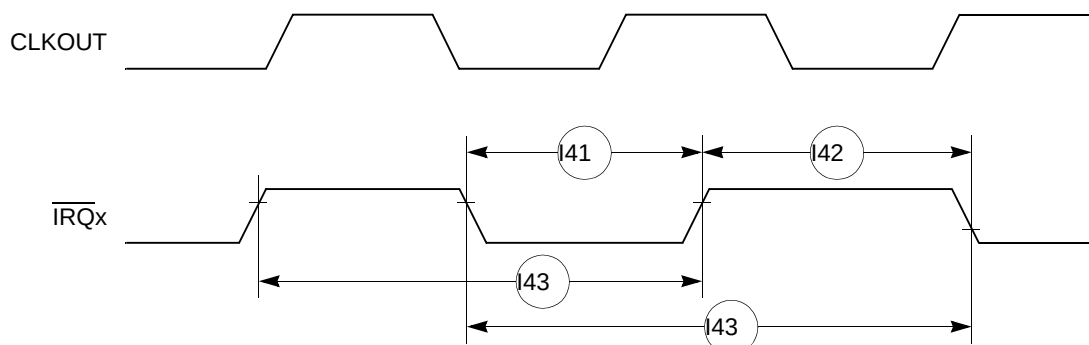
The timings I41, I42, and I43 are specified to allow the correct function of the  $\overline{\text{IRQ}}$  lines detection circuitry, and have no direct relation with the total system interrupt latency that the MPC852T is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.



**Figure 23. Interrupt Detection Timing for External Level Sensitive Lines**

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.



**Figure 24. Interrupt Detection Timing for External Edge Sensitive Lines**

Table 11 shows the PCMCIA timing for the MPC852T.

Table 11. PCMCIA Timing

| Num | Characteristic                                                                                                                                             | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|     |                                                                                                                                                            | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| J82 | A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted. <sup>1</sup> (MIN = 0.75 x B1 - 2.00)                                                    | 20.70  | —     | 16.70  | —     | 13.00  | —     | 9.40   | —     | ns   |
| J83 | A(0:31), $\overline{\text{REG}}$ valid to ALE negation. <sup>1</sup> (MIN = 1.00 x B1 - 2.00)                                                              | 28.30  | —     | 23.00  | —     | 18.00  | —     | 13.20  | —     | ns   |
| J84 | CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 x B1 + 8.00)                                                                                           | 7.60   | 15.60 | 6.30   | 14.30 | 5.00   | 13.00 | 3.80   | 11.80 | ns   |
| J85 | CLKOUT to $\overline{\text{REG}}$ Invalid. (MIN = 0.25 x B1 + 1.00)                                                                                        | 8.60   | —     | 7.30   | —     | 6.00   | —     | 4.80   | —     | ns   |
| J86 | CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ asserted. (MAX = 0.25 x B1 + 8.00)                                                             | 7.60   | 15.60 | 6.30   | 14.30 | 5.00   | 13.00 | 3.80   | 11.80 | ns   |
| J87 | CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ negated. (MAX = 0.25 x B1 + 8.00)                                                              | 7.60   | 15.60 | 6.30   | 14.30 | 5.00   | 13.00 | 3.80   | 11.80 | ns   |
| J88 | CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ assert time. (MAX = 0.00 x B1 + 11.00) | —      | 11.00 | —      | 11.00 | —      | 11.00 | —      | 11.00 | ns   |
| J89 | CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negate time. (MAX = 0.00 x B1 + 11.00) | 2.00   | 11.00 | 2.00   | 11.00 | 2.00   | 11.00 | 2.00   | 11.00 | ns   |
| J90 | CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30)                                                                                                         | 7.60   | 13.80 | 6.30   | 12.50 | 5.00   | 11.30 | 3.80   | 10.00 | ns   |
| J91 | CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00)                                                                                                         | —      | 15.60 | —      | 14.30 | —      | 13.00 | —      | 11.80 | ns   |
| J92 | $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negated to D(0:31) invalid. <sup>1</sup> (MIN = 0.25 x B1 - 2.00)                                      | 5.60   | —     | 4.30   | —     | 3.00   | —     | 1.80   | —     | ns   |
| J93 | $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge. <sup>1</sup> (MIN = 0.00 x B1 + 8.00)                                 | 8.00   | —     | 8.00   | —     | 8.00   | —     | 8.00   | —     | ns   |
| J94 | CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid. <sup>1</sup> (MIN = 0.00 x B1 + 2.00)                               | 2.00   | —     | 2.00   | —     | 2.00   | —     | 2.00   | —     | ns   |

<sup>1</sup> PSST = 1. Otherwise add PSST times cycle time.  
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the  $\overline{\text{WAITA}}$  signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The  $\overline{\text{WAITA}}$  assertion is effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC852T PowerQUICC User's Manual*.

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

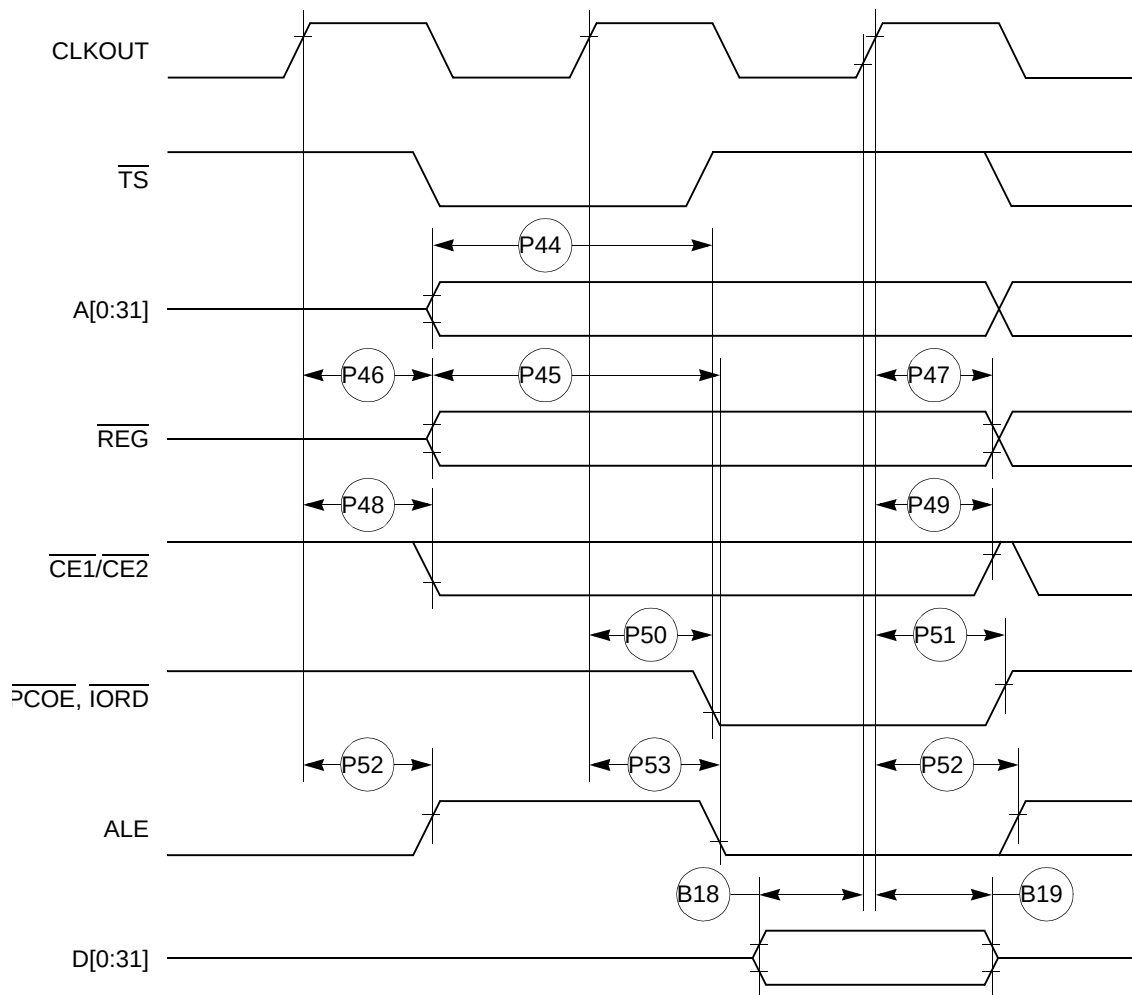


Figure 25. PCMCIA Access Cycles Timing External Bus Read

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

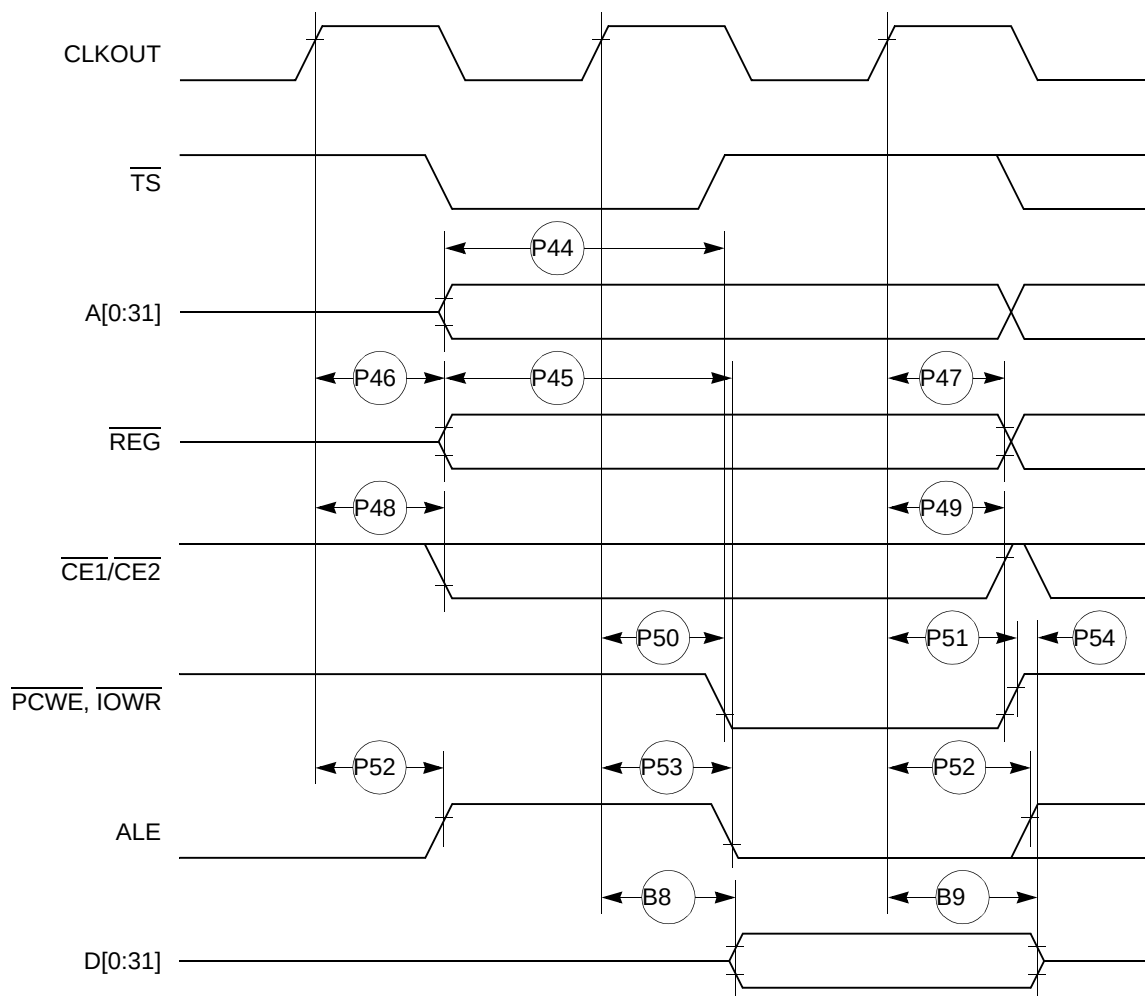


Figure 26. PCMCIA Access Cycles Timing External Bus Write

Figure 27 provides the PCMCIA  $\overline{WAITA}$  signals detection timing.

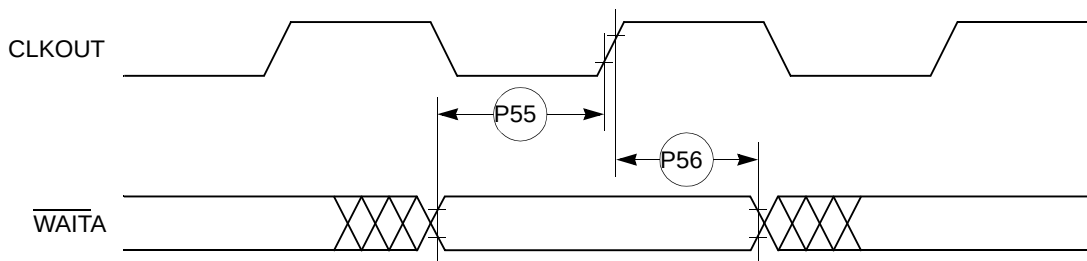


Figure 27. PCMCIA  $\overline{WAITA}$  Signals Detection Timing

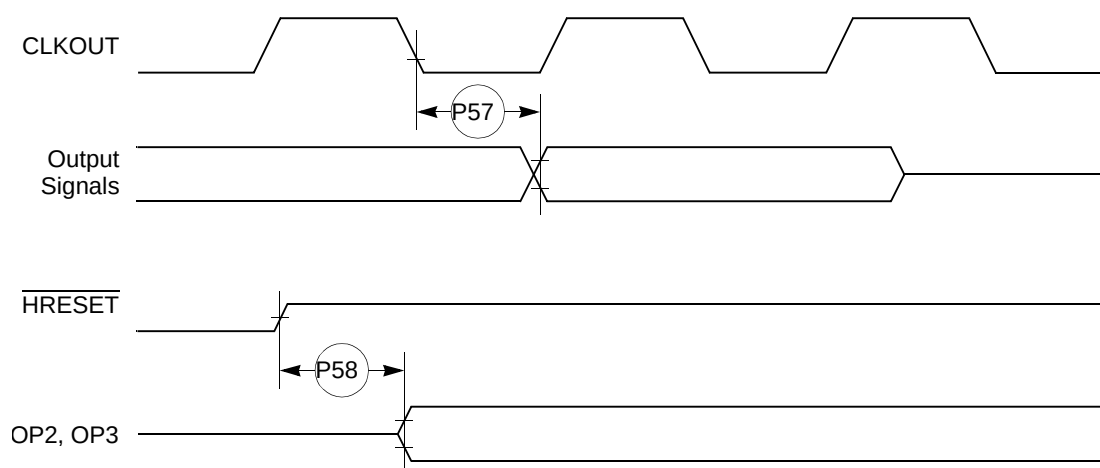
Table 12 shows the PCMCIA port timing for the MPC852T.

**Table 12. PCMCIA Port Timing**

| Num | Characteristic                                                                                        | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|-----|-------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|     |                                                                                                       | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| J95 | CLKOUT to OPx Valid ( $\text{MAX} = 0.00 \times B1 + 19.00$ )                                         | —      | 19.00 | —      | 19.00 | —      | 19.00 | —      | 19.00 | ns   |
| J96 | $\overline{\text{HRESET}}$ negated to OPx drive <sup>1</sup> ( $\text{MIN} = 0.75 \times B1 + 3.00$ ) | 25.70  | —     | 21.70  | —     | 18.00  | —     | 14.40  | —     | ns   |
| J97 | IP_Xx valid to CLKOUT rising edge ( $\text{MIN} = 0.00 \times B1 + 5.00$ )                            | 5.00   | —     | 5.00   | —     | 5.00   | —     | 5.00   | —     | ns   |
| J98 | CLKOUT rising edge to IP_Xx invalid ( $\text{MIN} = 0.00 \times B1 + 1.00$ )                          | 1.00   | —     | 1.00   | —     | 1.00   | —     | 1.00   | —     | ns   |

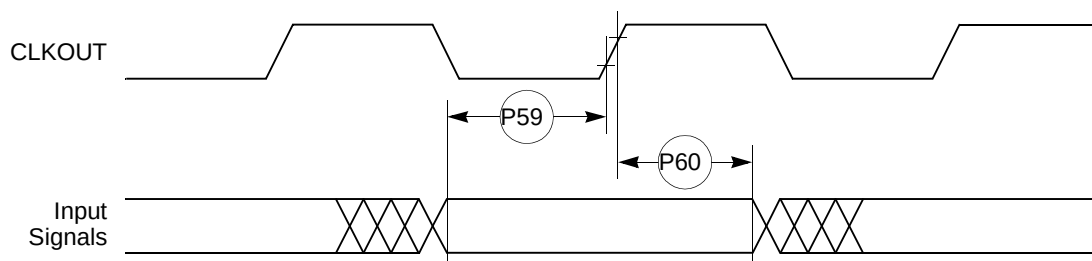
<sup>1</sup> OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC852T.



**Figure 28. PCMCIA Output Port Timing**

Figure 29 provides the PCMCIA output port timing for the MPC852T.



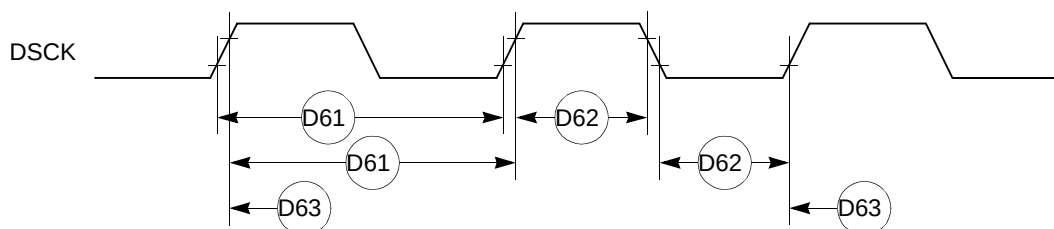
**Figure 29. PCMCIA Input Port Timing**

Table 13 shows the debug port timing for the MPC852T.

**Table 13. Debug Port Timing**

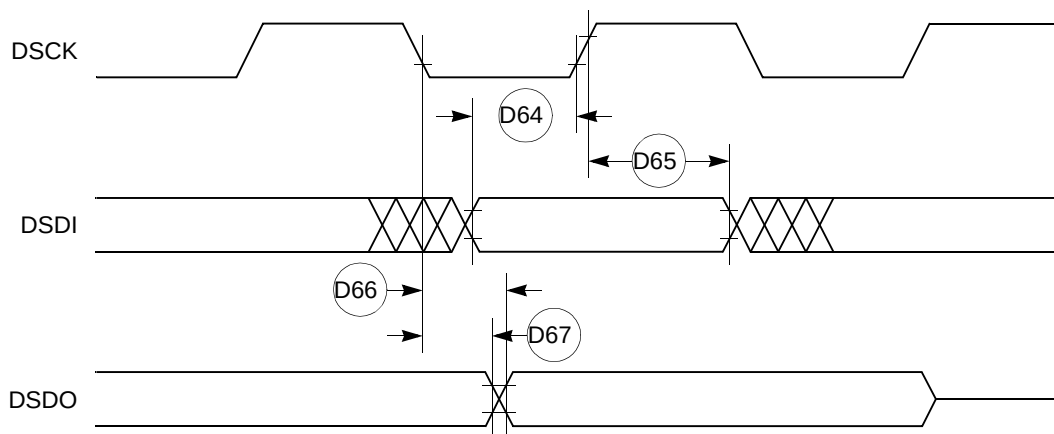
| Num | Characteristic              | All Frequencies                   |       | Unit |
|-----|-----------------------------|-----------------------------------|-------|------|
|     |                             | Min                               | Max   |      |
| J82 | DSCK cycle time             | $3 \times T_{\text{CLOCKOUT}}$    | —     | —    |
| J83 | DSCK clock pulse width      | $1.25 \times T_{\text{CLOCKOUT}}$ | —     | —    |
| J84 | DSCK rise and fall times    | 0.00                              | 3.00  | ns   |
| J85 | DSDI input data setup time  | 8.00                              | —     | ns   |
| J86 | DSDI data hold time         | 5.00                              | —     | ns   |
| J87 | DSCK low to DSDO data valid | 0.00                              | 15.00 | ns   |
| J88 | DSCK low to DSDO invalid    | 0.00                              | 2.00  | ns   |

Figure 30 provides the input timing for the debug port clock.



**Figure 30. Debug Port Clock Input Timing**

Figure 31 provides the timing for the debug port.



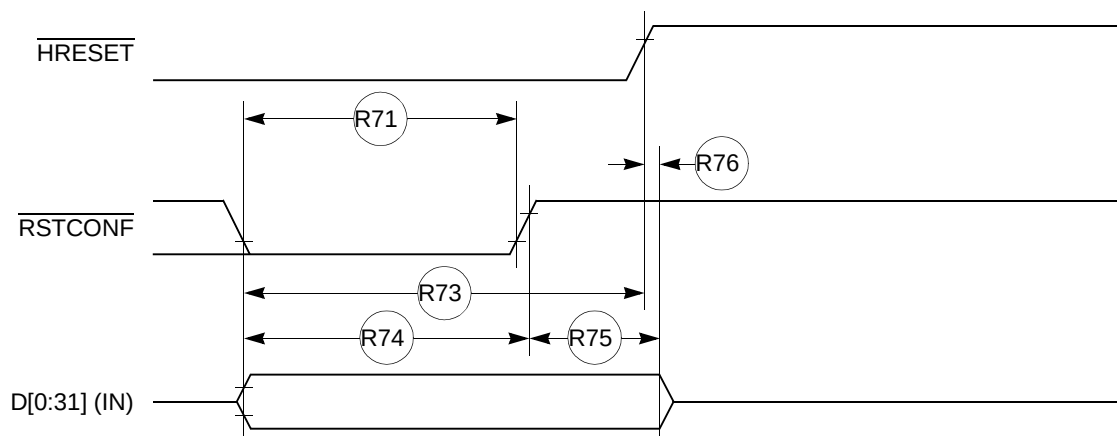
**Figure 31. Debug Port Timings**

Table 14 shows the reset timing for the MPC852T.

**Table 14. Reset Timing**

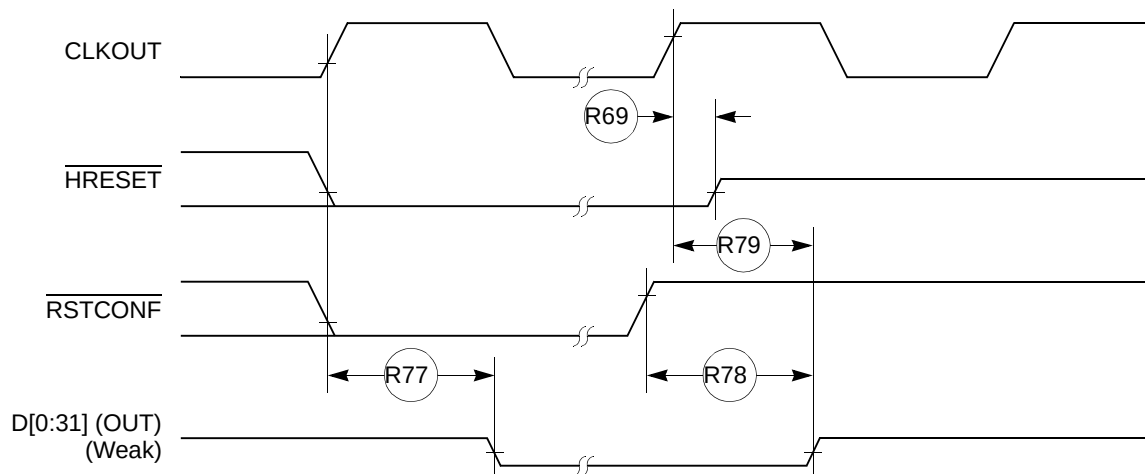
| Num | Characteristic                                                                                                                               | 33 MHz |       | 40 MHz |       | 50 MHz |       | 66 MHz |       | Unit |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------|--------|-------|--------|-------|--------|-------|--------|-------|------|
|     |                                                                                                                                              | Min    | Max   | Min    | Max   | Min    | Max   | Min    | Max   |      |
| J82 | CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$ )                                                        | —      | 20.00 | —      | 20.00 | —      | 20.00 | —      | 20.00 | ns   |
| J83 | CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$ )                                                        | —      | 20.00 | —      | 20.00 | —      | 20.00 | —      | 20.00 | ns   |
| J84 | $\overline{\text{RSTCONF}}$ pulse width (MIN = $17.00 \times B1$ )                                                                           | 515.20 | —     | 425.00 | —     | 340.00 | —     | 257.60 | —     | ns   |
| J85 | —                                                                                                                                            | —      | —     | —      | —     | —      | —     | —      | —     | —    |
| J86 | Configuration data to HRESET rising edge set up time (MIN = $15.00 \times B1 + 50.00$ )                                                      | 504.50 | —     | 425.00 | —     | 350.00 | —     | 277.30 | —     | ns   |
| J87 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = $0.00 \times B1 + 350.00$ )                                 | 350.00 | —     | 350.00 | —     | 350.00 | —     | 350.00 | —     | ns   |
| J88 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = $0.00 \times B1 + 0.00$ )                                     | 0.00   | —     | 0.00   | —     | 0.00   | —     | 0.00   | —     | ns   |
| J89 | Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = $0.00 \times B1 + 0.00$ )                                      | 0.00   | —     | 0.00   | —     | 0.00   | —     | 0.00   | —     | ns   |
| J90 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = $0.00 \times B1 + 25.00$ )                      | —      | 25.00 | —      | 25.00 | —      | 25.00 | —      | 25.00 | ns   |
| J91 | $\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = $0.00 \times B1 + 25.00$ )                                            | —      | 25.00 | —      | 25.00 | —      | 25.00 | —      | 25.00 | ns   |
| J92 | CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = $0.00 \times B1 + 25.00$ ) | —      | 25.00 | —      | 25.00 | —      | 25.00 | —      | 25.00 | ns   |
| J93 | DSDI, DSCK set up (MIN = $3.00 \times B1$ )                                                                                                  | 90.90  | —     | 75.00  | —     | 60.00  | —     | 45.50  | —     | ns   |
| J94 | DSDI, DSCK hold time (MIN = $0.00 \times B1 + 0.00$ )                                                                                        | 0.00   | —     | 0.00   | —     | 0.00   | —     | 0.00   | —     | ns   |
| J95 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = $8.00 \times B1$ )                                  | 242.40 | —     | 200.00 | —     | 160.00 | —     | 121.20 | —     | ns   |

Figure 32 shows the reset timing for the data bus configuration.



**Figure 32. Reset Timing—Configuration from Data Bus**

Figure 33 provides the reset timing for the data bus weak drive during configuration.



**Figure 33. Reset Timing—Data Bus Weak Drive during Configuration**



Figure 34 provides the reset timing for the debug port configuration.

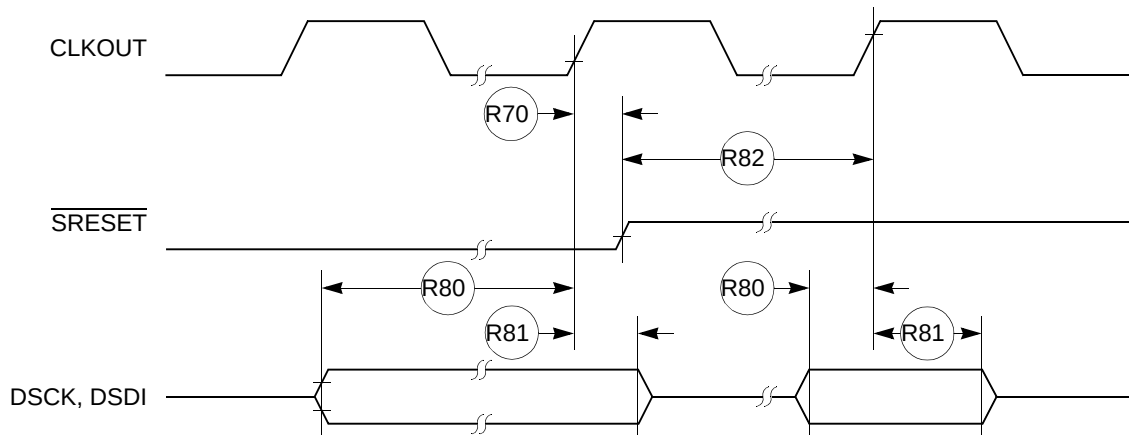


Figure 34. Reset Timing—Debug Port Configuration

## 13 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC852T shown in Figure 35 through Figure 38.

Table 15. JTAG Timing

| Num | Characteristic                                         | All Frequencies |       | Unit |
|-----|--------------------------------------------------------|-----------------|-------|------|
|     |                                                        | Min             | Max   |      |
| J82 | TCK cycle time                                         | 100.00          | —     | ns   |
| J83 | TCK clock pulse width measured at 1.5 V                | 40.00           | —     | ns   |
| J84 | TCK rise and fall times                                | 0.00            | 10.00 | ns   |
| J85 | TMS, TDI data setup time                               | 5.00            | —     | ns   |
| J86 | TMS, TDI data hold time                                | 25.00           | —     | ns   |
| J87 | TCK low to TDO data valid                              | —               | 27.00 | ns   |
| J88 | TCK low to TDO data invalid                            | 0.00            | —     | ns   |
| J89 | TCK low to TDO high impedance                          | —               | 20.00 | ns   |
| J90 | $\overline{\text{TRST}}$ assert time                   | 100.00          | —     | ns   |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low         | 40.00           | —     | ns   |
| J92 | TCK falling edge to output valid                       | —               | 50.00 | ns   |
| J93 | TCK falling edge to output valid out of high impedance | —               | 50.00 | ns   |
| J94 | TCK falling edge to output high impedance              | —               | 50.00 | ns   |
| J95 | Boundary scan input valid to TCK rising edge           | 50.00           | —     | ns   |
| J96 | TCK rising edge to boundary scan input invalid         | 50.00           | —     | ns   |

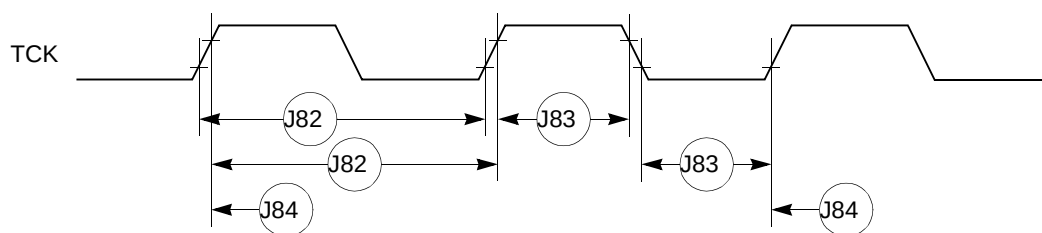


Figure 35. JTAG Test Clock Input Timing

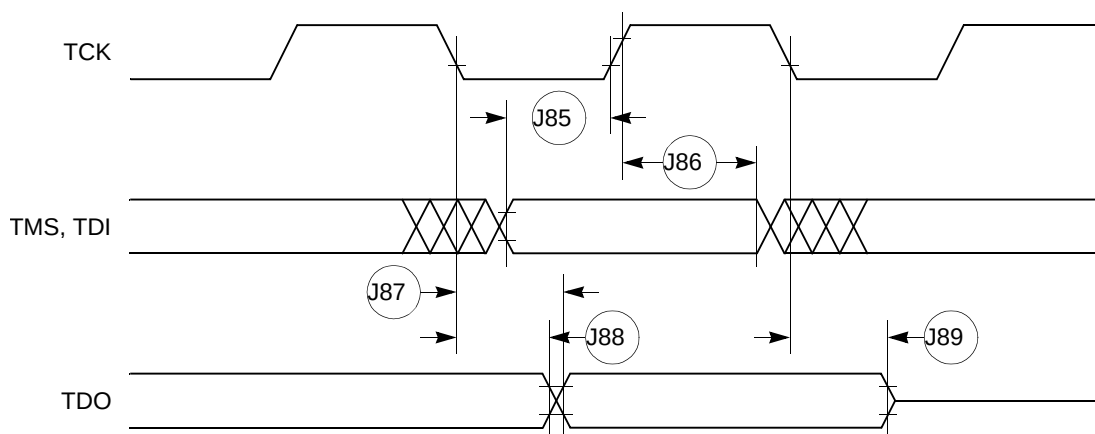
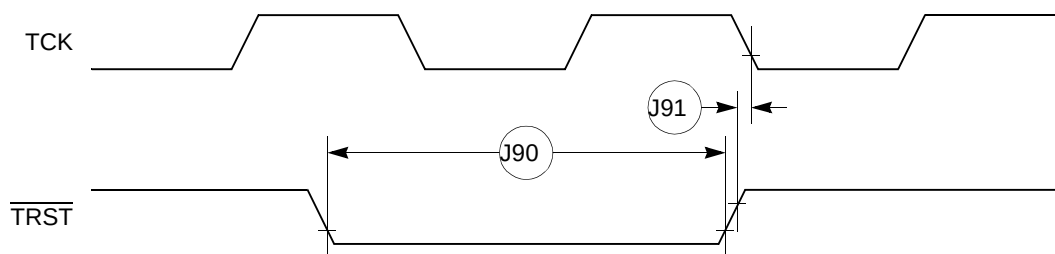


Figure 36. JTAG Test Access Port Timing Diagram

Figure 37. JTAG  $\overline{\text{TRST}}$  Timing Diagram

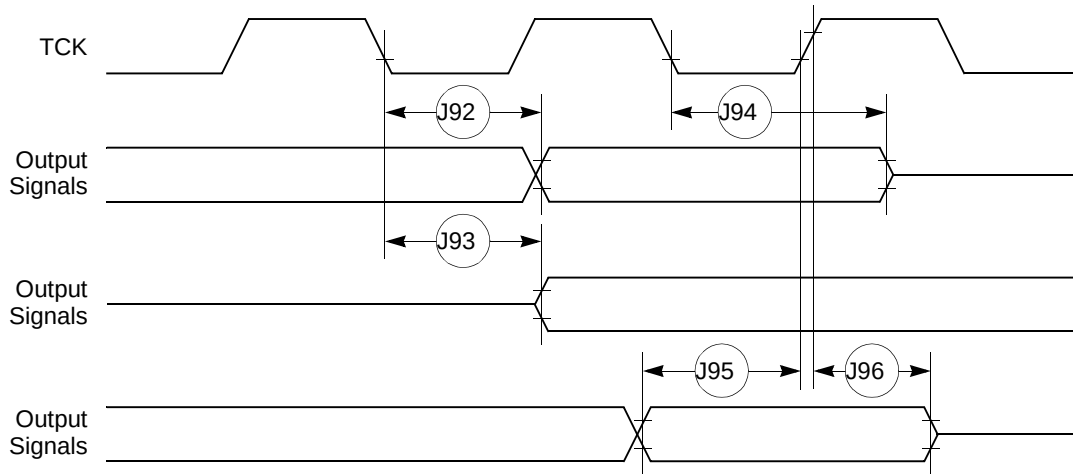


Figure 38. Boundary Scan (JTAG) Timing Diagram

## 14 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC852T.

### 14.1 Port C Interrupt AC Electrical Specifications

Table 16 provides the timings for port C interrupts.

Table 16. Port C Interrupt Timing

| Num | Characteristic                                         | 33.34 MHz |     | Unit |
|-----|--------------------------------------------------------|-----------|-----|------|
|     |                                                        | Min       | Max |      |
| 35  | Port C interrupt pulse width low (edge-triggered mode) | 55        | —   | ns   |
| 36  | Port C interrupt minimum time between active edges     | 55        | —   | ns   |

Figure 39 shows the port C interrupt detection timing.

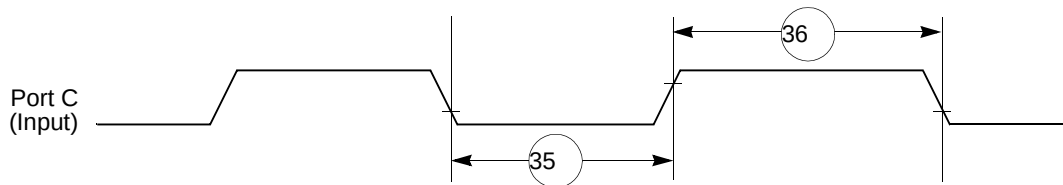


Figure 39. Port C Interrupt Detection Timing

## 14.2 IDMA Controller AC Electrical Specifications

Table 17 provides the IDMA controller timings as shown in Figure 40 through Figure 43.

Table 17. IDMA Controller Timing

| Num | Characteristic                                                                                                         | All Frequencies |     | Unit |
|-----|------------------------------------------------------------------------------------------------------------------------|-----------------|-----|------|
|     |                                                                                                                        | Min             | Max |      |
| 40  | $\overline{\text{DREQ}}$ setup time to clock high                                                                      | 7               | —   | ns   |
| 41  | $\overline{\text{DREQ}}$ hold time from clock high <sup>1</sup>                                                        | 3               | —   | ns   |
| 42  | $\overline{\text{SDACK}}$ assertion delay from clock high                                                              | —               | 12  | ns   |
| 43  | $\overline{\text{SDACK}}$ negation delay from clock low                                                                | —               | 12  | ns   |
| 44  | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low                                               | —               | 20  | ns   |
| 45  | $\overline{\text{SDACK}}$ negation delay from clock high                                                               | —               | 15  | ns   |
| 46  | $\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$ ) | 7               | —   | ns   |

<sup>1</sup> Applies to high-to-low mode (EDM=1)

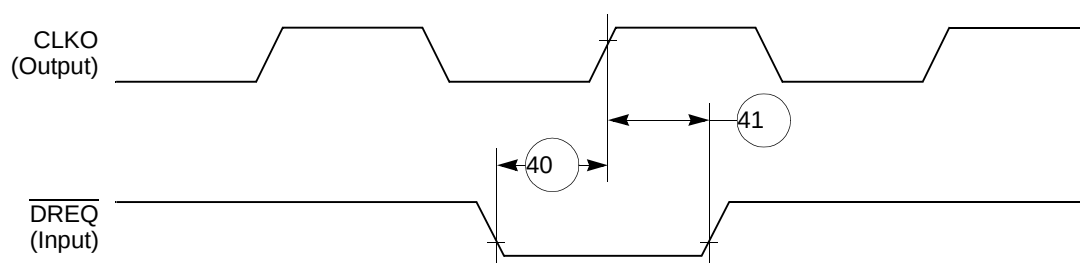


Figure 40. IDMA External Requests Timing Diagram

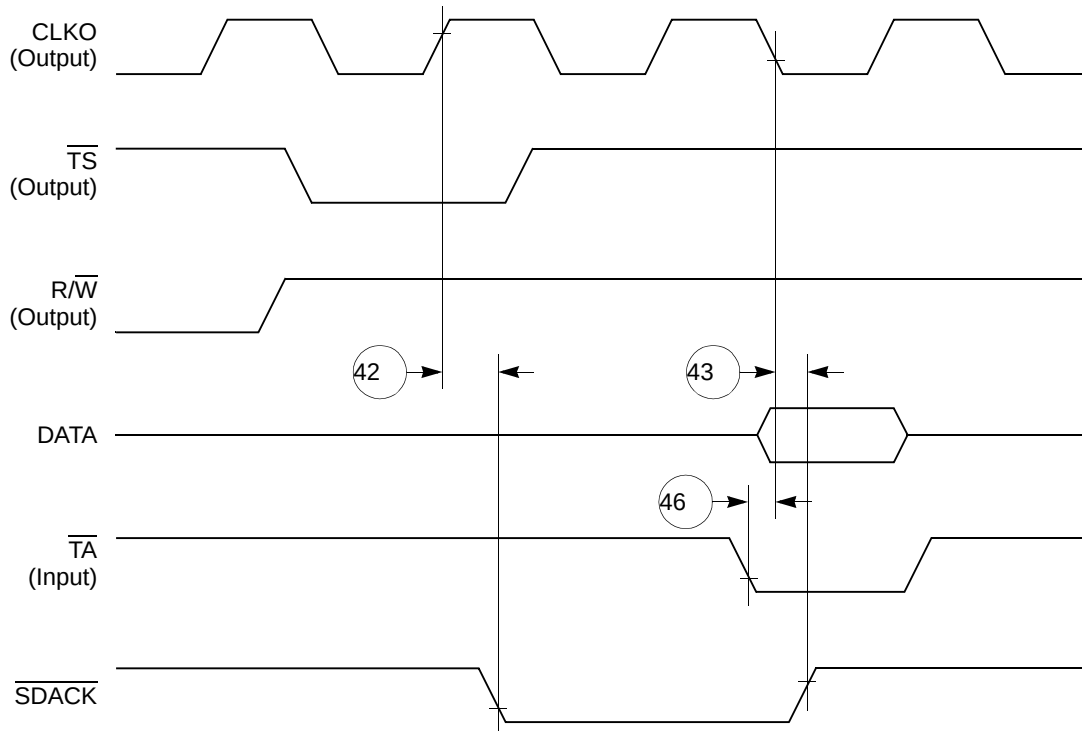


Figure 41.  $\overline{SDACK}$  Timing Diagram—Peripheral Write, Externally-Generated  $\overline{TA}$

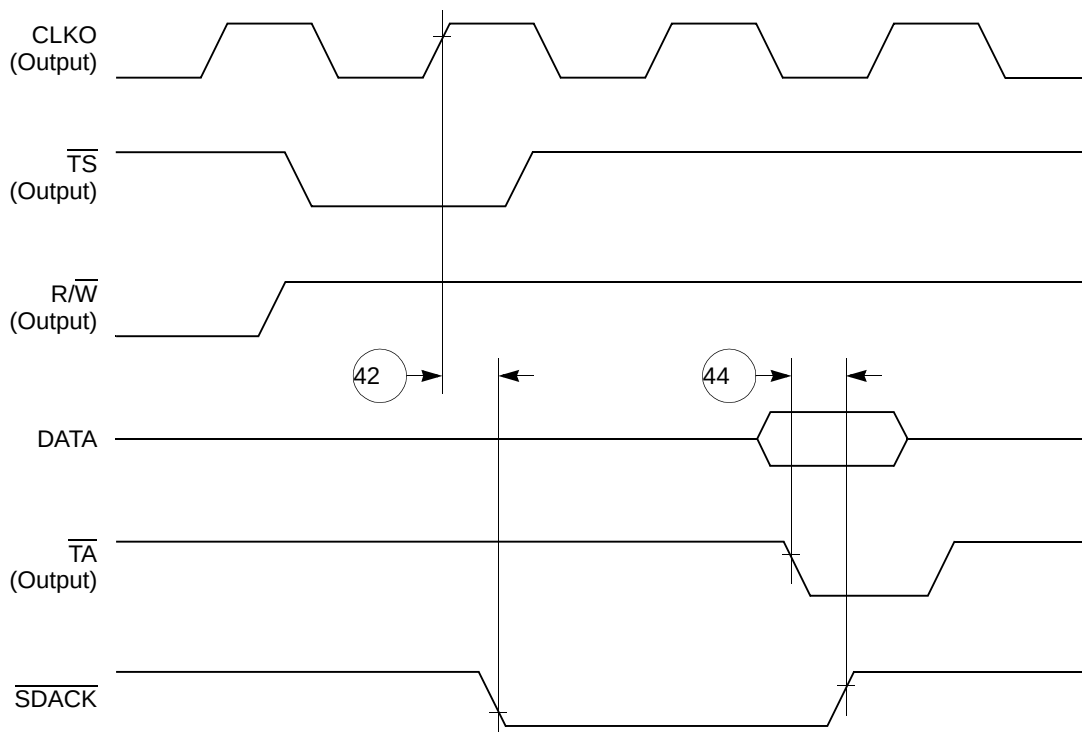


Figure 42.  $\overline{SDACK}$  Timing Diagram—Peripheral Write, Internally-Generated  $\overline{TA}$

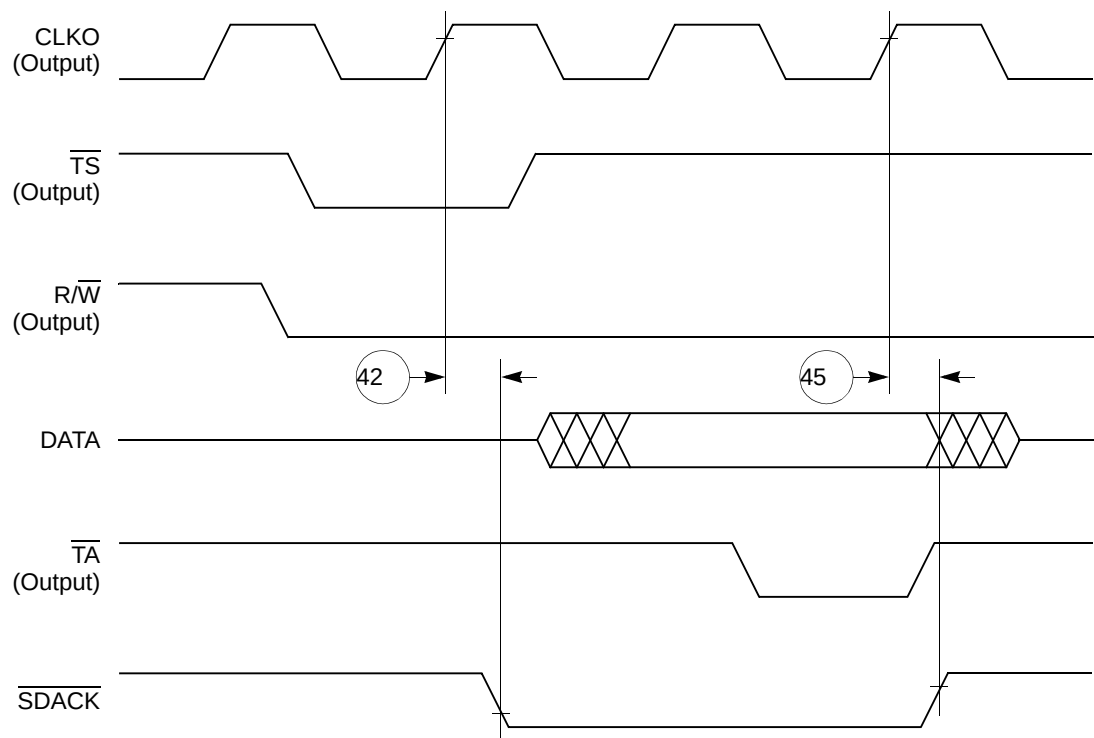


Figure 43. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

### 14.3 Baud Rate Generator AC Electrical Specifications

Table 18 provides the baud rate generator timings as shown in Figure 44.

Table 18. Baud Rate Generator Timing

| Num | Characteristic          | All Frequencies |     | Unit |
|-----|-------------------------|-----------------|-----|------|
|     |                         | Min             | Max |      |
| 50  | BRGO rise and fall time | —               | 10  | ns   |
| 51  | BRGO duty cycle         | 40              | 60  | %    |
| 52  | BRGO cycle              | 40              | —   | ns   |

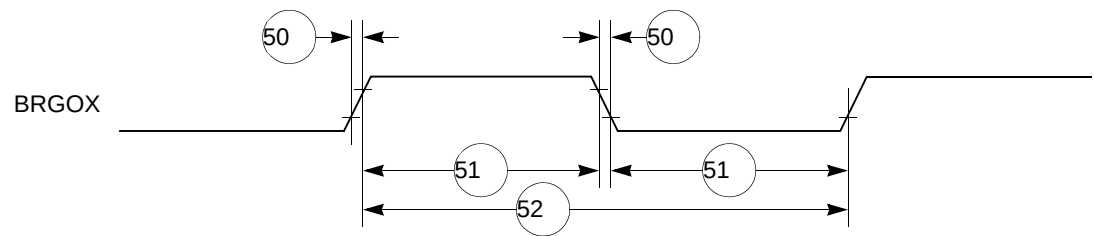


Figure 44. Baud Rate Generator Timing Diagram

## 14.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 45.

Table 19. Timer Timing

| Num | Characteristic               | All Frequencies |     | Unit |
|-----|------------------------------|-----------------|-----|------|
|     |                              | Min             | Max |      |
| 61  | TIN/TGATE rise and fall time | 10              | —   | ns   |
| 62  | TIN/TGATE low time           | 1               | —   | clk  |
| 63  | TIN/TGATE high time          | 2               | —   | clk  |
| 64  | TIN/TGATE cycle time         | 3               | —   | clk  |
| 65  | CLKO low to TOUT valid       | 3               | 25  | ns   |

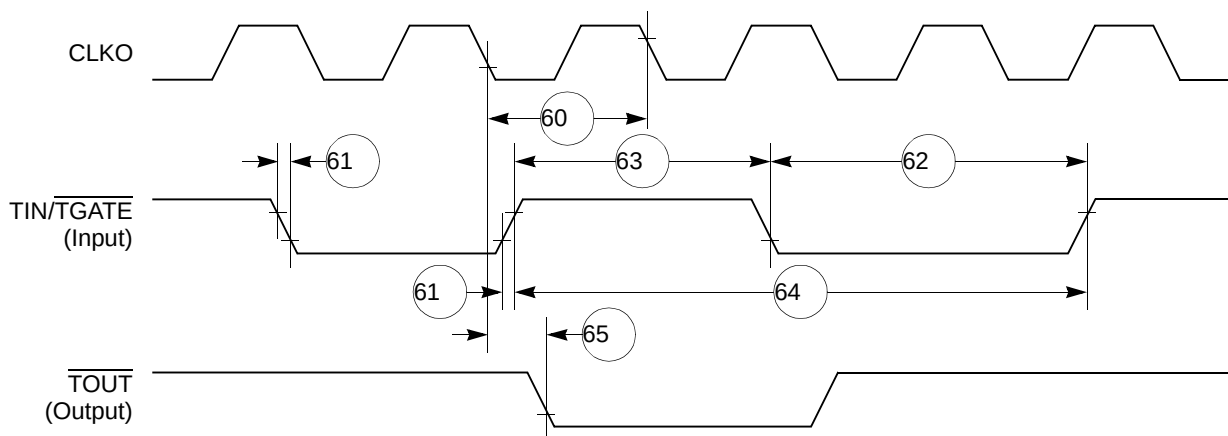


Figure 45. CPM General-Purpose Timers Timing Diagram

## 14.5 SCC in NMSI Mode Electrical Specifications

Table 20 provides the NMSI external clock timing.

Table 20. NMSI External Clock Timing

| Num | Characteristic                                       | All Frequencies |       | Unit |
|-----|------------------------------------------------------|-----------------|-------|------|
|     |                                                      | Min             | Max   |      |
| 100 | RCLK3 and TCLK3 width high <sup>1</sup>              | 1/SYNCCLK       | —     | ns   |
| 101 | RCLK3 and TCLK3 width low                            | 1/SYNCCLK +5    | —     | ns   |
| 102 | RCLK3 and TCLK3 rise/fall time                       | —               | 15.00 | ns   |
| 103 | TXD3 active delay (from TCLK3 falling edge)          | 0.00            | 50.00 | ns   |
| 104 | RTS3 active/inactive delay (from TCLK3 falling edge) | 0.00            | 50.00 | ns   |
| 105 | CTS3 setup time to TCLK3 rising edge                 | 5.00            | —     | ns   |

**Table 20. NMSI External Clock Timing (continued)**

| Num | Characteristic                                           | All Frequencies |     | Unit |
|-----|----------------------------------------------------------|-----------------|-----|------|
|     |                                                          | Min             | Max |      |
| 106 | RXD3 setup time to RCLK3 rising edge                     | 5.00            | —   | ns   |
| 107 | RXD3 hold time from RCLK3 rising edge <sup>2</sup>       | 5.00            | —   | ns   |
| 108 | $\overline{\text{CD}}$ 3 setup Time to RCLK3 rising edge | 5.00            | —   | ns   |

<sup>1</sup> The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

<sup>2</sup> Also applies to  $\overline{\text{CD}}$  and  $\overline{\text{CTS}}$  hold time when they are used as an external sync signal.

Table 21 provides the NMSI internal clock timing.

**Table 21. NMSI Internal Clock Timing**

| Num | Characteristic                                                            | All Frequencies |           | Unit |
|-----|---------------------------------------------------------------------------|-----------------|-----------|------|
|     |                                                                           | Min             | Max       |      |
| 100 | RCLK3 and TCLK3 frequency <sup>1</sup>                                    | 0.00            | SYNCCLK/3 | MHz  |
| 102 | RCLK3 and TCLK3 rise/fall time                                            | —               | —         | ns   |
| 103 | TXD3 active delay (from TCLK3 falling edge)                               | 0.00            | 30.00     | ns   |
| 104 | $\overline{\text{RTS}}$ 3 active/inactive delay (from TCLK3 falling edge) | 0.00            | 30.00     | ns   |
| 105 | $\overline{\text{CTS}}$ 3 setup time to TCLK3 rising edge                 | 40.00           | —         | ns   |
| 106 | RXD3 setup time to RCLK3 rising edge                                      | 40.00           | —         | ns   |
| 107 | RXD3 hold time from RCLK3 rising edge <sup>2</sup>                        | 0.00            | —         | ns   |
| 108 | $\overline{\text{CD}}$ 3 setup time to RCLK3 rising edge                  | 40.00           | —         | ns   |

<sup>1</sup> The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 3/1.

<sup>2</sup> Also applies to  $\overline{\text{CD}}$  and  $\overline{\text{CTS}}$  hold time when they are used as an external sync signals.



Figure 46 through Figure 48 show the NMSI timings.

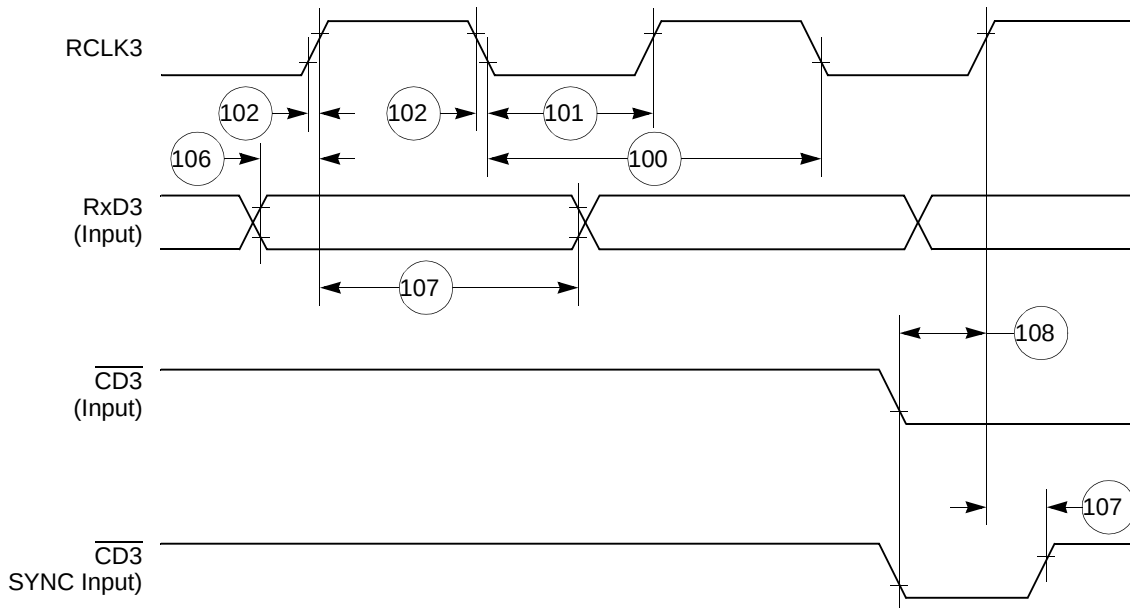


Figure 46. SCC NMSI Receive Timing Diagram

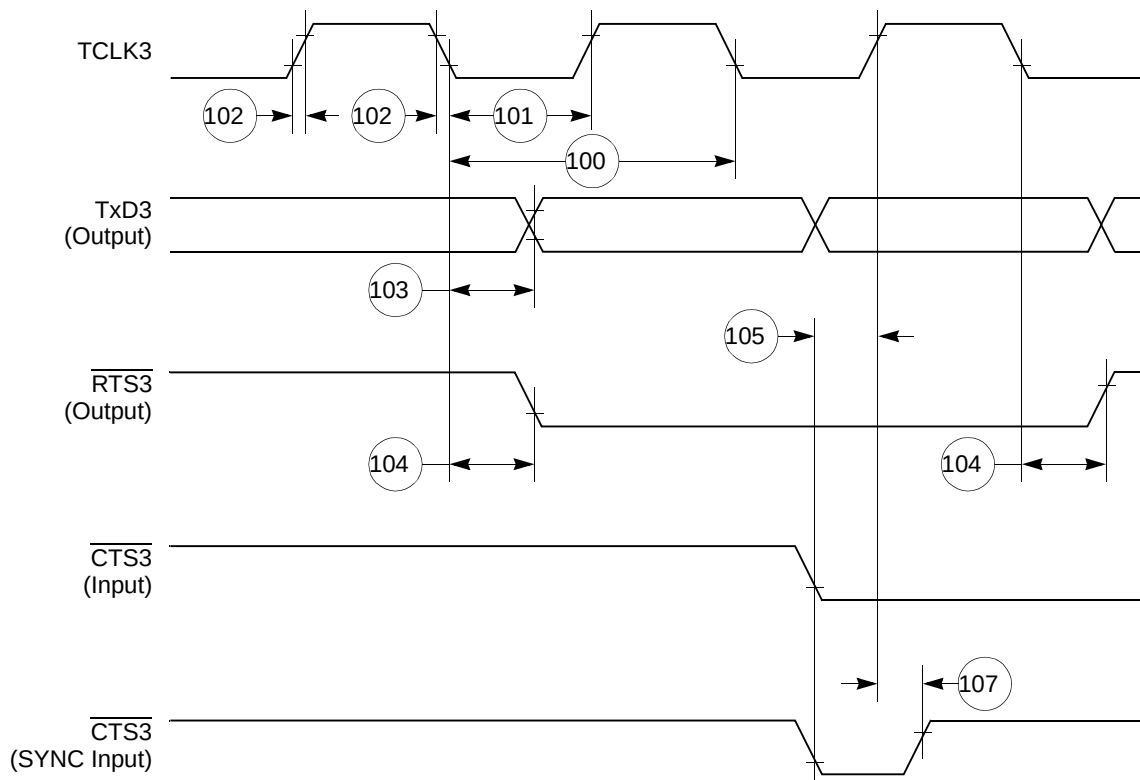


Figure 47. SCC NMSI Transmit Timing Diagram

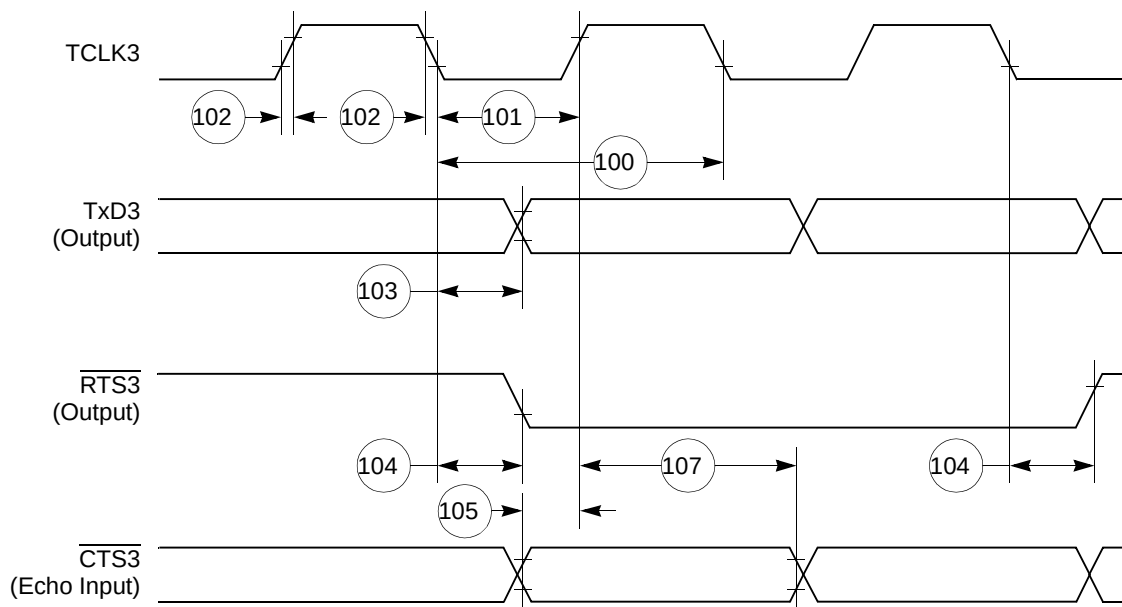


Figure 48. HDLC Bus Timing Diagram

## 14.6 Ethernet Electrical Specifications

Table 22 provides the Ethernet timings as shown in Figure 49 through Figure 53.

Table 22. Ethernet Timing

| Num | Characteristic                                                  | All Frequencies |     | Unit |
|-----|-----------------------------------------------------------------|-----------------|-----|------|
|     |                                                                 | Min             | Max |      |
| 120 | CLSN width high                                                 | 40              | —   | ns   |
| 121 | RCLK3 rise/fall time                                            | —               | 15  | ns   |
| 122 | RCLK3 width low                                                 | 40              | —   | ns   |
| 123 | RCLK3 clock period <sup>1</sup>                                 | 80              | 120 | ns   |
| 124 | RXD3 setup time                                                 | 20              | —   | ns   |
| 125 | RXD3 hold time                                                  | 5               | —   | ns   |
| 126 | RENA active delay (from RCLK3 rising edge of the last data bit) | 10              | —   | ns   |
| 127 | RENA width low                                                  | 100             | —   | ns   |
| 128 | TCLK3 rise/fall time                                            | —               | 15  | ns   |
| 129 | TCLK3 width low                                                 | 40              | —   | ns   |
| 130 | TCLK3 clock period <sup>1</sup>                                 | 99              | 101 | ns   |
| 131 | TXD3 active delay (from TCLK3 rising edge)                      | —               | 50  | ns   |
| 132 | TXD3 inactive delay (from TCLK3 rising edge)                    | 6.5             | 50  | ns   |
| 133 | TENA active delay (from TCLK3 rising edge)                      | 10              | 50  | ns   |

Table 22. Ethernet Timing (continued)

| Num | Characteristic                                                     | All Frequencies |     | Unit |
|-----|--------------------------------------------------------------------|-----------------|-----|------|
|     |                                                                    | Min             | Max |      |
| 134 | TENA inactive delay (from TCLK3 rising edge)                       | 10              | 50  | ns   |
| 135 | $\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)   | 10              | 50  | ns   |
| 136 | $\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge) | 10              | 50  | ns   |
| 137 | $\overline{\text{REJECT}}$ width low                               | 1               | —   | CLK  |
| 138 | CLKO1 low to $\overline{\text{SDACK}}$ asserted <sup>2</sup>       | —               | 20  | ns   |
| 139 | CLKO1 low to $\overline{\text{SDACK}}$ negated <sup>2</sup>        | —               | 20  | ns   |

<sup>1</sup> The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater or equal to 2/1.

<sup>2</sup>  $\overline{\text{SDACK}}$  is asserted whenever the SDMA writes the incoming frame DA into memory.

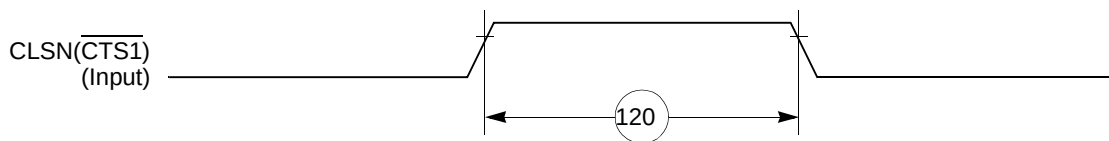


Figure 49. Ethernet Collision Timing Diagram

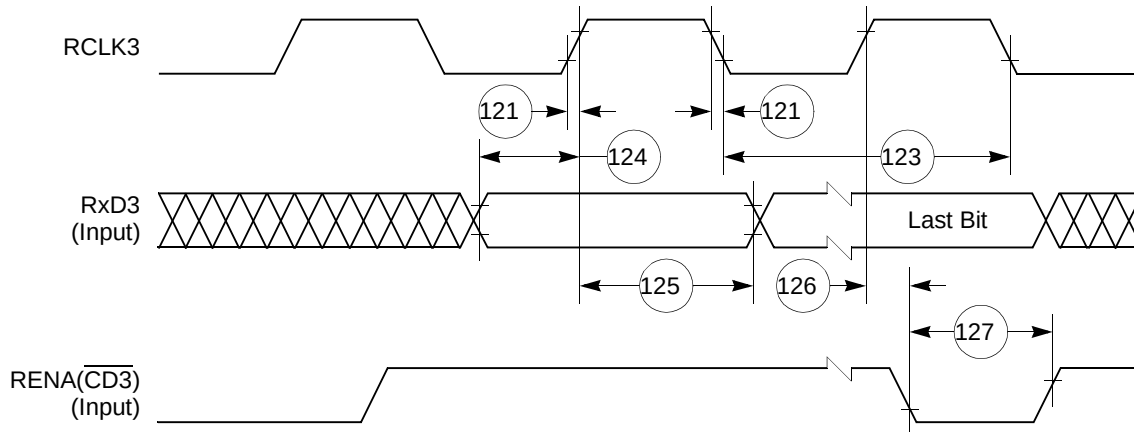
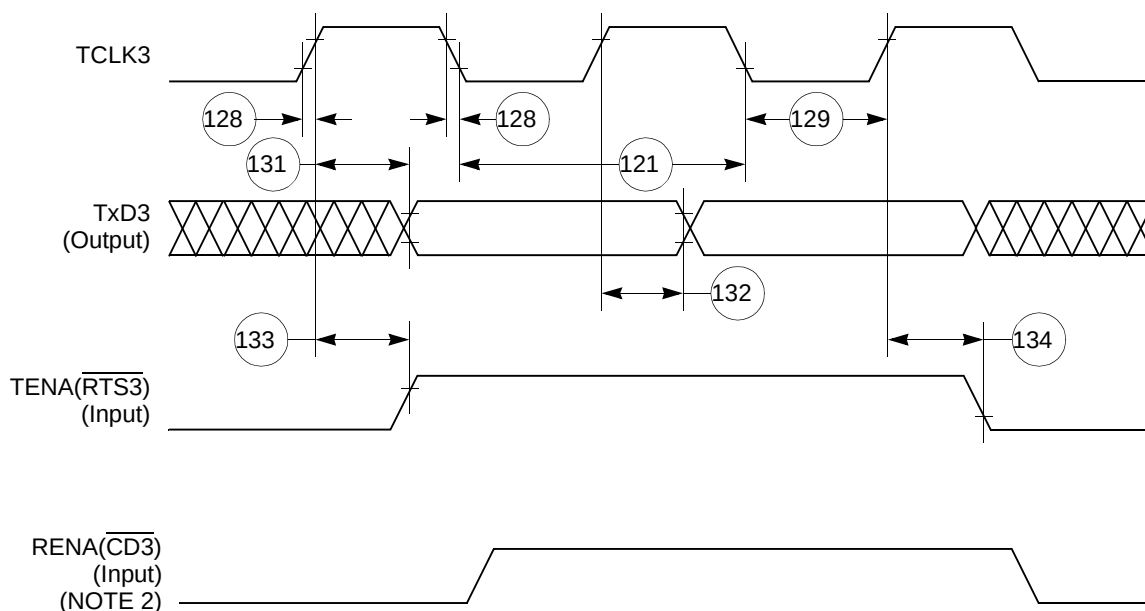


Figure 50. Ethernet Receive Timing Diagram



NOTES:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 51. Ethernet Transmit Timing Diagram

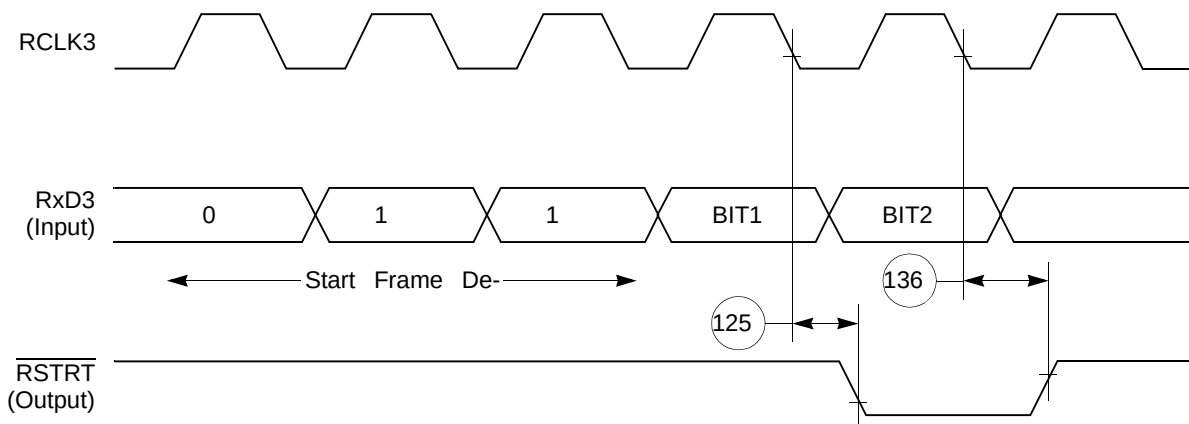


Figure 52. CAM Interface Receive Start Timing Diagram

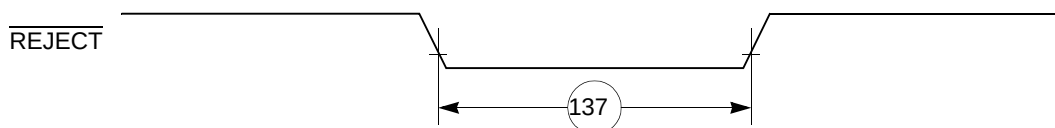


Figure 53. CAM Interface REJECT Timing Diagram

## 14.7 SPI Master AC Electrical Specifications

Table 23 provides the SPI master timings as shown in Figure 54 and Figure 55.

Table 23. SPI Master Timing

| Num | Characteristic                      | All Frequencies |      | Unit      |
|-----|-------------------------------------|-----------------|------|-----------|
|     |                                     | Min             | Max  |           |
| 160 | MASTER cycle time                   | 4               | 1024 | $t_{cyc}$ |
| 161 | MASTER clock (SCK) high or low time | 2               | 512  | $t_{cyc}$ |
| 162 | MASTER data setup time (inputs)     | 15              | —    | ns        |
| 163 | Master data hold time (inputs)      | 0               | —    | ns        |
| 164 | Master data valid (after SCK edge)  | —               | 10   | ns        |
| 165 | Master data hold time (outputs)     | 0               | —    | ns        |
| 166 | Rise time output                    | —               | 15   | ns        |
| 167 | Fall time output                    | —               | 15   | ns        |

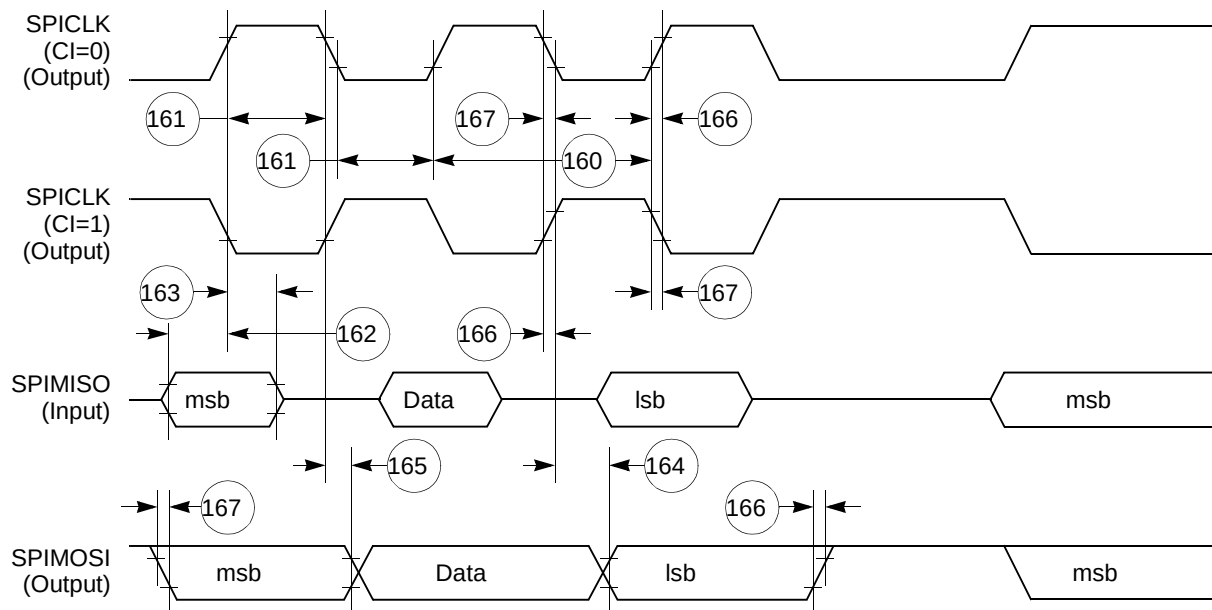


Figure 54. SPI Master (CP = 0) Timing Diagram

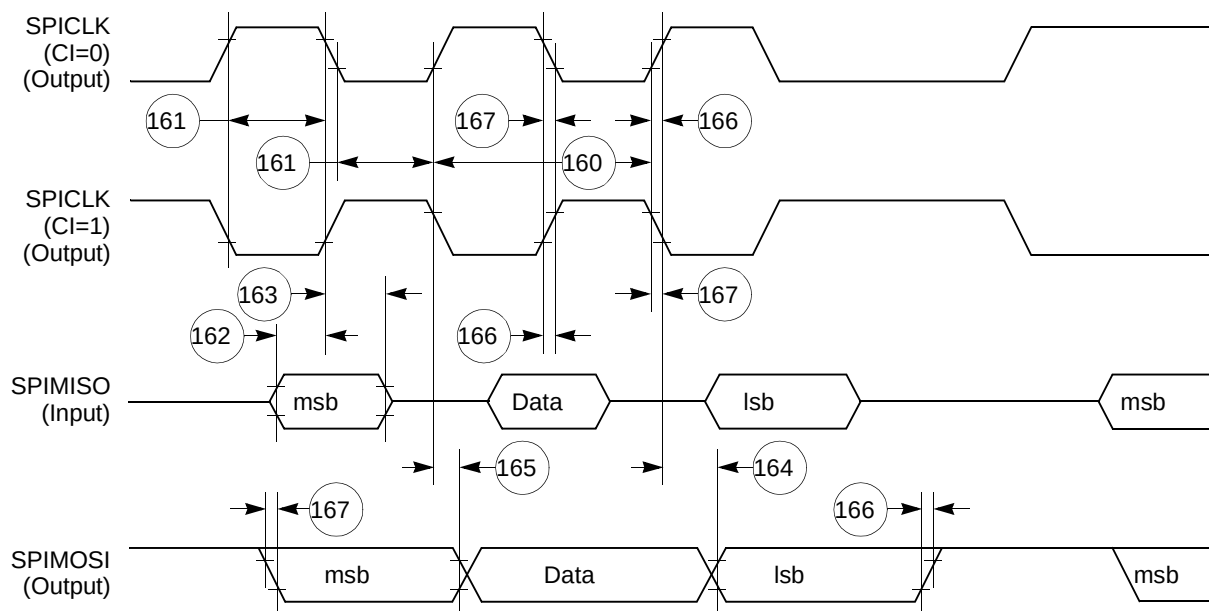


Figure 55. SPI Master (CP = 1) Timing Diagram

## 14.8 SPI Slave AC Electrical Specifications

Table 24 provides the SPI slave timings as shown in Figure 56 and Figure 57.

Table 24. SPI Slave Timing

| Num | Characteristic                                              | All Frequencies |     | Unit      |
|-----|-------------------------------------------------------------|-----------------|-----|-----------|
|     |                                                             | Min             | Max |           |
| 170 | Slave cycle time                                            | 2               | —   | $t_{cyc}$ |
| 171 | Slave enable lead time                                      | 15              | —   | ns        |
| 172 | Slave enable lag time                                       | 15              | —   | ns        |
| 173 | Slave clock (SPICLK) high or low time                       | 1               | —   | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1               | —   | $t_{cyc}$ |
| 175 | Slave data setup time (inputs)                              | 20              | —   | ns        |
| 176 | Slave data hold time (inputs)                               | 20              | —   | ns        |
| 177 | Slave access time                                           | —               | 50  | ns        |

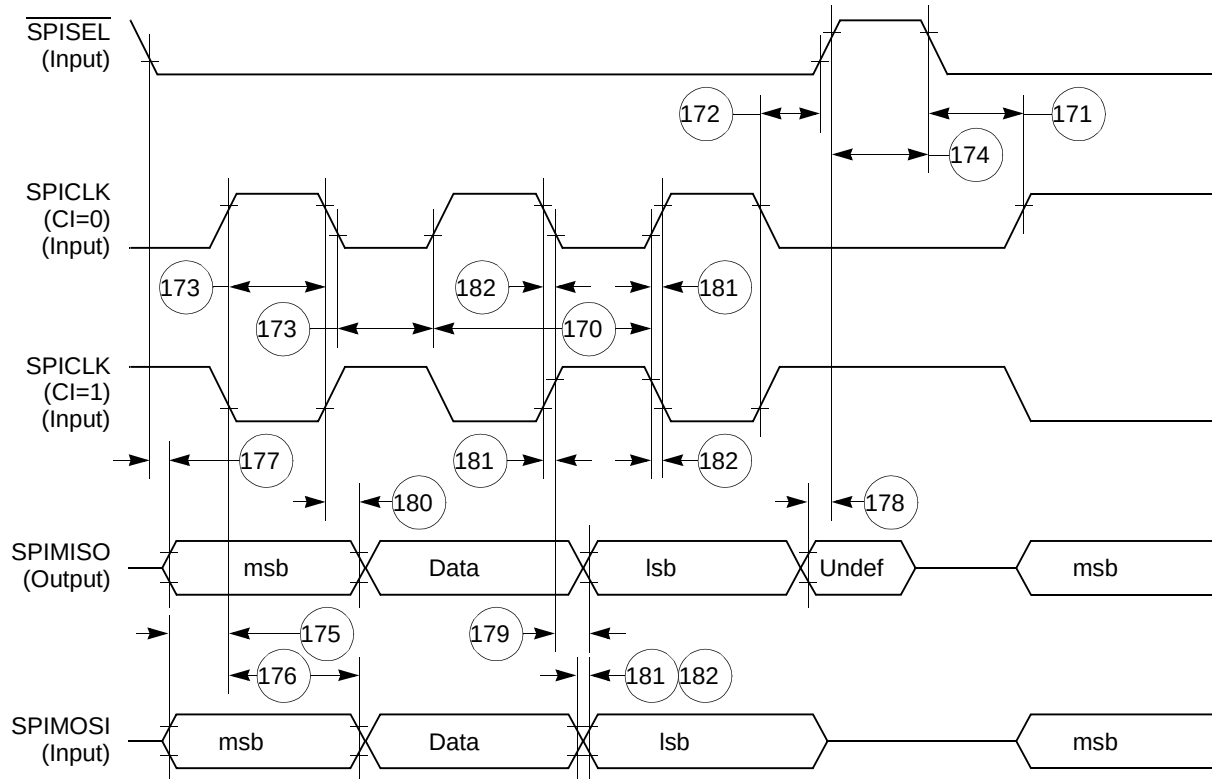


Figure 56. SPI Slave (CP = 0) Timing Diagram

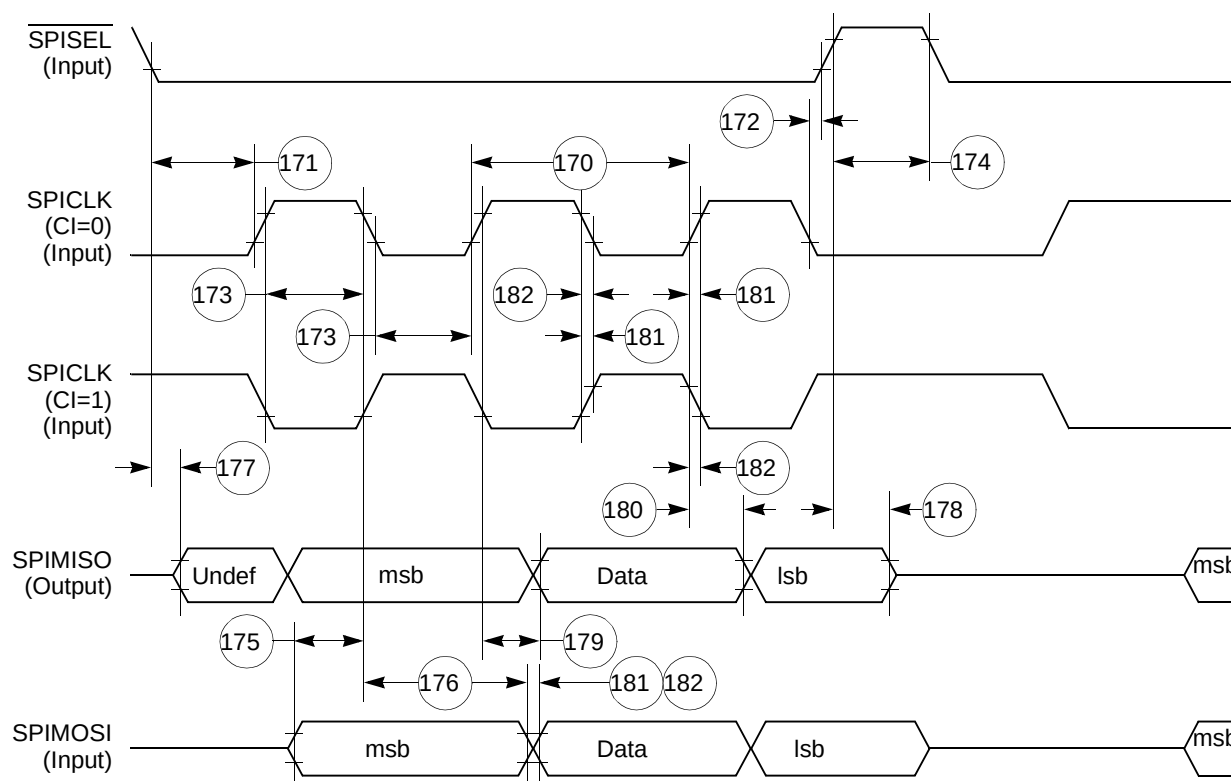


Figure 57. SPI Slave (CP = 1) Timing Diagram

## 15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

### 15.1 MII Receive Signal Timing (MII\_RXD[3:0], MII\_RX\_DV, MII\_RX\_ER, MII\_RX\_CLK)

The receiver functions correctly up to a MII\_RX\_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII\_RX\_CLK frequency - 1%.

Table 25 provides information on the MII receive signal timing.

Table 25. MII Receive Signal Timing

| Num | Characteristic                                         | Min | Max | Unit              |
|-----|--------------------------------------------------------|-----|-----|-------------------|
| M1  | MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup | 5   | —   | ns                |
| M2  | MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold  | 5   | —   | ns                |
| M3  | MII_RX_CLK pulse width high                            | 35% | 65% | MII_RX_CLK period |
| M4  | MII_RX_CLK pulse width low                             | 35% | 65% | MII_RX_CLK period |



Figure 58 shows MII receive signal timing.

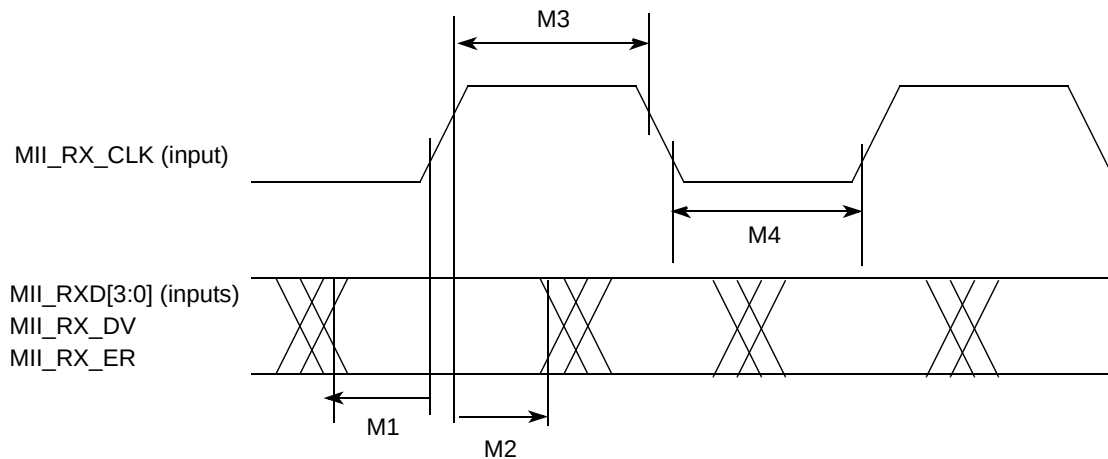


Figure 58. MII Receive Signal Timing Diagram

## 15.2 MII Transmit Signal Timing (MII\_TXD[3:0], MII\_TX\_EN, MII\_TX\_ER, MII\_TX\_CLK)

The transmitter functions correctly up to a MII\_TX\_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII\_TX\_CLK frequency - 1%.

Table 26 provides information about the MII transmit signal timing.

Table 26. MII Transmit Signal Timing

| Num | Characteristic                                           | Min | Max | Unit              |
|-----|----------------------------------------------------------|-----|-----|-------------------|
| M5  | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid | 5   | —   | ns                |
| M6  | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid   | —   | 25  | —                 |
| M7  | MII_TX_CLK pulse width high                              | 35% | 65% | MII_TX_CLK period |
| M8  | MII_TX_CLK pulse width low                               | 35% | 65% | MII_TX_CLK period |

Figure 59 shows the MII transmit signal timing diagram.

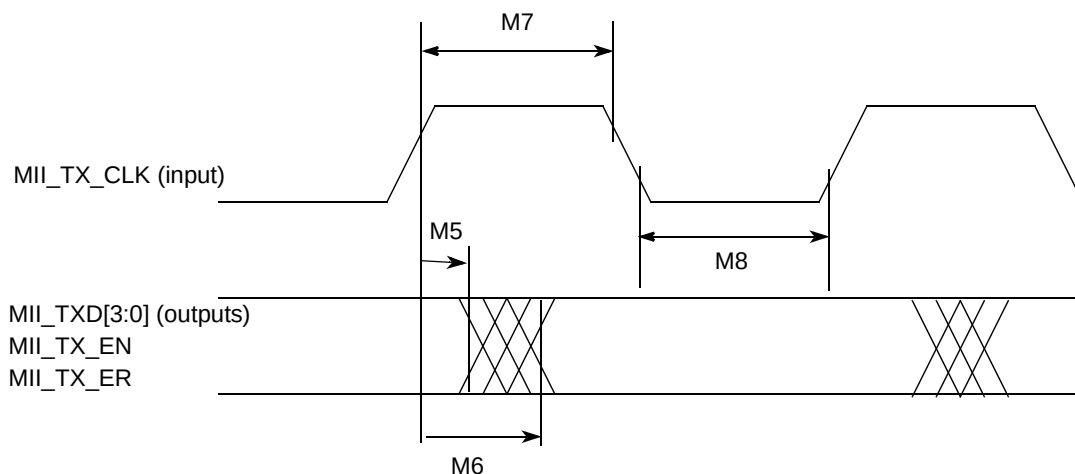


Figure 59. MII Transmit Signal Timing Diagram

### 15.3 MII Async Inputs Signal Timing (MII\_CRD, MII\_COL)

Table 27 provides information about the MII async inputs signal timing.

Table 27. MII Async Inputs Signal Timing

| Num | Characteristic                       | Min | Max | Unit              |
|-----|--------------------------------------|-----|-----|-------------------|
| M9  | MII_CRD, MII_COL minimum pulse width | 1.5 | —   | MII_TX_CLK period |

Figure 60 shows the MII asynchronous inputs signal timing diagram.

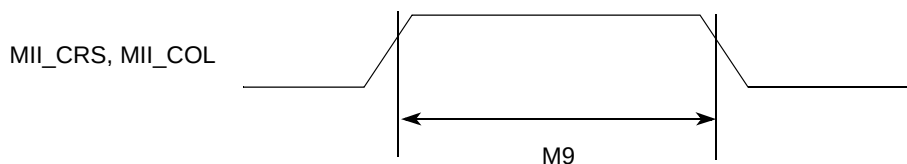


Figure 60. MII Async Inputs Timing Diagram

### 15.4 MII Serial Management Channel Timing (MII\_MDIO, MII\_MDC)

Table 28 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 28. MII Serial Management Channel Timing

| Num | Characteristic                                                              | Min | Max | Unit |
|-----|-----------------------------------------------------------------------------|-----|-----|------|
| M10 | MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay) | 0   | —   | ns   |
| M11 | MII_MDC falling edge to MII_MDIO output valid (max prop delay)              | —   | 25  | ns   |
| M12 | MII_MDIO (input) to MII_MDC rising edge setup                               | 10  | —   | ns   |
| M13 | MII_MDIO (input) to MII_MDC rising edge hold                                | 0   | —   | ns   |

Table 28. MII Serial Management Channel Timing (continued)

| Num | Characteristic           | Min | Max | Unit           |
|-----|--------------------------|-----|-----|----------------|
| M14 | MII_MDC pulse width high | 40% | 60% | MII_MDC period |
| M15 | MII_MDC pulse width low  | 40% | 60% | MII_MDC period |

Figure 61 shows the MII serial management channel timing diagram.

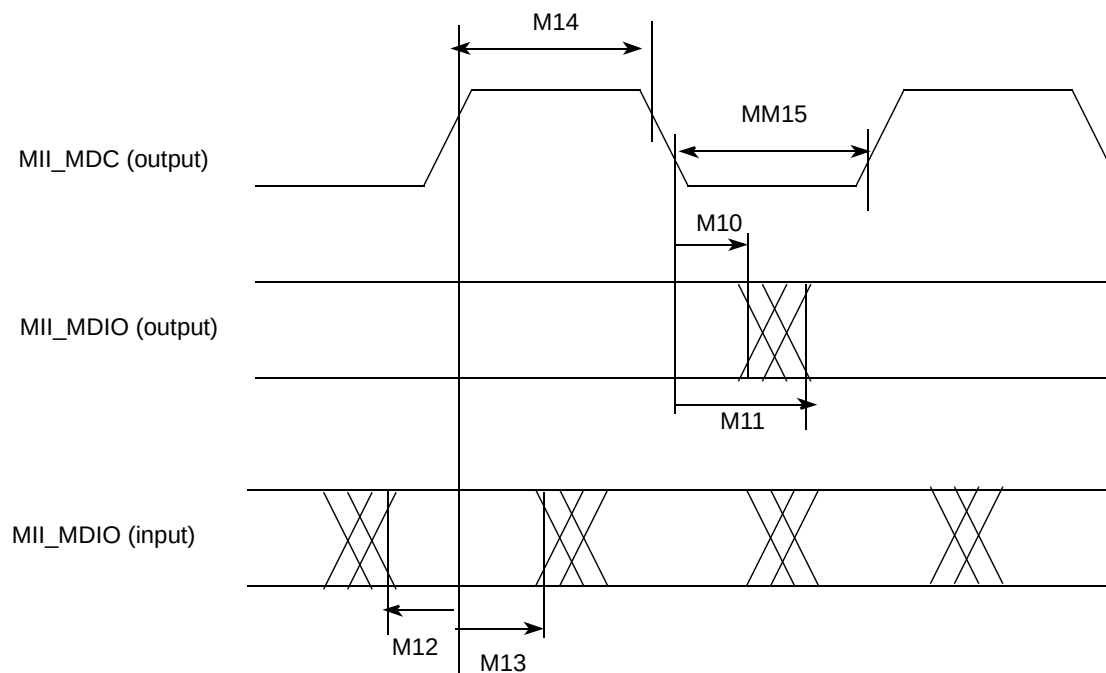


Figure 61. MII Serial Management Channel Timing Diagram

## 16 Mechanical Data and Ordering Information

Table 29 identifies the packages and operating frequencies orderable for the MPC852T.

**Table 29. MPC852T Package/Frequency Orderable**

| Package Type                                  | Temperature (Tj) | Frequency (MHz) | Order Number                 |
|-----------------------------------------------|------------------|-----------------|------------------------------|
| Plastic ball grid array<br>(VR and ZT suffix) | 0°C to 95°C      | 50              | MPC852TVR50<br>MPC852TZT50   |
|                                               |                  | 66              | MPC852TVR66<br>MPC852TZT66   |
|                                               |                  | 80              | MPC852TVR80<br>MPC852TZT80   |
|                                               |                  | 100             | MPC852TVR100<br>MPC852TZT100 |
| Plastic ball grid array<br>(CVR suffix)       | – 40°C to 100°C  | 66              | TBD                          |

### 16.1 Pin Assignments

The following sections give the pinout and pin listing for the JEDEC Compliant and the non-JEDEC versions of the 16 x 16 PBGA package.

### 16.1.1 The JEDEC Compliant Pinout

Figure 62 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

**NOTE: This is the top view of the device.**

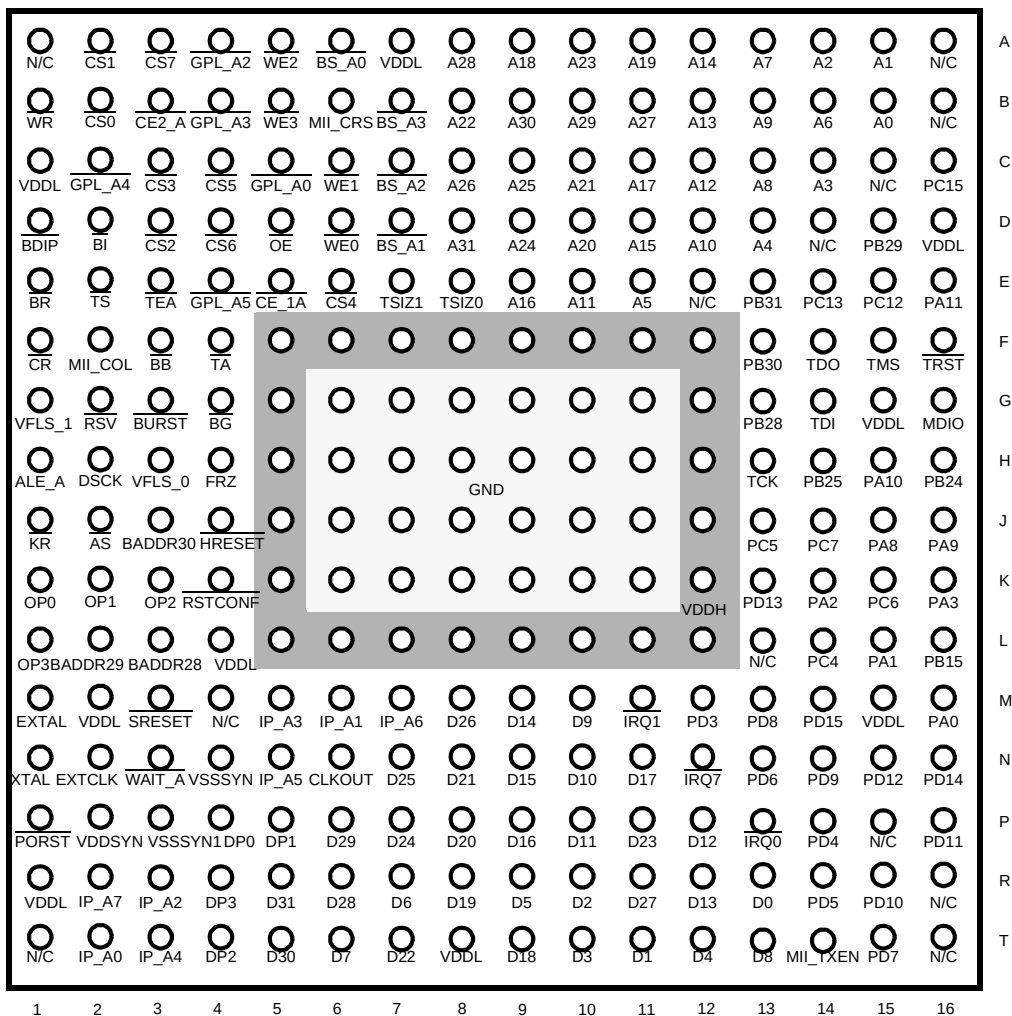


Figure 62. Pinout of the PBGA Package - JEDEC Standard

Table 30 contains a list of the MPC852T input and output signals and shows multiplexing and pin assignments.

**Table 30. Pin Assignments - JEDEC Standard**

| Name                           | Pin Number                                                                                                                                            | Type                                        |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|
| A[0:31]                        | B15, A15, A14, C14, D13, E11, B14, A13, C13, B13, D12, E10, C12, B12, A12, D11, E9, C11, A9, A11, D10, C10, B8, A10, D9, C9, C8, B11, A8, B10, B9, D8 | Bidirectional<br>Three-state (3.3V only)    |
| TSIZ0<br>REG                   | E8                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| TSIZ1                          | E7                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| RD/WR                          | B1                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| BURST                          | G3                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| BDIP<br>GPL_B5                 | D1                                                                                                                                                    | Output                                      |
| TS                             | E2                                                                                                                                                    | Bidirectional<br>Active Pull-up (3.3V only) |
| TA                             | F4                                                                                                                                                    | Bidirectional<br>Active Pull-up (3.3V only) |
| TEA                            | E3                                                                                                                                                    | Open-drain                                  |
| BI                             | D2                                                                                                                                                    | Bidirectional<br>Active Pull-up (3.3V only) |
| IRQ2<br>RSV                    | G2                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| IRQ4<br>KR<br>RETRY<br>SPKROUT | J1                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| CR<br>IRQ3                     | F1                                                                                                                                                    | Input (3.3V only)                           |
| D[0:31]                        | R13, T11, R10, T10, T12, R9, R7, T6, T13, M10, N10, P10, P12, R12, M9, N9, P9, N11, T9, R8, P8, N8, T7, P11, P7, N7, M8, R11, R6, P6, T5, R5          | Bidirectional<br>Three-state (3.3V only)    |
| DP0<br>IRQ3                    | P4                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| DP1<br>IRQ4                    | P5                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| DP2<br>IRQ5                    | T4                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| DP3<br>IRQ6                    | R4                                                                                                                                                    | Bidirectional<br>Three-state (3.3V only)    |
| BR                             | E1                                                                                                                                                    | Bidirectional (3.3V only)                   |

Table 30. Pin Assignments - JEDEC Standard (continued)

| Name                                                                                              | Pin Number             | Type                                        |
|---------------------------------------------------------------------------------------------------|------------------------|---------------------------------------------|
| $\overline{\text{BG}}$                                                                            | G4                     | Bidirectional (3.3V only)                   |
| $\overline{\text{BB}}$                                                                            | F3                     | Bidirectional<br>Active Pull-up (3.3V only) |
| $\overline{\text{FRZ}}$<br>$\overline{\text{IRQ6}}$                                               | H4                     | Bidirectional (3.3V only)                   |
| $\overline{\text{IRQ0}}$                                                                          | P13                    | Input (3.3V only)                           |
| $\overline{\text{IRQ1}}$                                                                          | M11                    | Input (3.3V only)                           |
| $\overline{\text{M\_TX\_CLK}}$<br>$\overline{\text{IRQ7}}$                                        | N12                    | Input (3.3V only)                           |
| $\overline{\text{CS}}[0:5]$                                                                       | B2, A2, D3, C3, E6, C4 | Output                                      |
| $\overline{\text{CS6}}$                                                                           | D4                     | Output                                      |
| $\overline{\text{CS7}}$                                                                           | A3                     | Output                                      |
| $\overline{\text{WE0}}$<br>$\overline{\text{BS\_B0}}$<br>$\overline{\text{IORD}}$                 | D6                     | Output                                      |
| $\overline{\text{WE1}}$<br>$\overline{\text{BS\_B1}}$<br>$\overline{\text{IOWR}}$                 | C6                     | Output                                      |
| $\overline{\text{WE2}}$<br>$\overline{\text{BS\_B2}}$<br>$\overline{\text{PCOE}}$                 | A5                     | Output                                      |
| $\overline{\text{WE3}}$<br>$\overline{\text{BS\_B3}}$<br>$\overline{\text{PCWE}}$                 | B5                     | Output                                      |
| $\overline{\text{BS\_A}}[0:3]$                                                                    | A6, D7, C7, B7         | Output                                      |
| $\overline{\text{GPL\_A0}}$<br>$\overline{\text{GPL\_B0}}$                                        | C5                     | Output                                      |
| $\overline{\text{OE}}$<br>$\overline{\text{GPL\_A1}}$<br>$\overline{\text{GPL\_B1}}$              | D5                     | Output                                      |
| $\overline{\text{GPL\_A}}[2:3]$<br>$\overline{\text{GPL\_B}}[2:3]$<br>$\overline{\text{CS}}[2-3]$ | A4, B4                 | Output                                      |
| $\overline{\text{UPWAITA}}$<br>$\overline{\text{GPL\_A4}}$                                        | C2                     | Bidirectional (3.3V only)                   |
| $\overline{\text{GPL\_A5}}$                                                                       | E4                     | Output                                      |
| $\overline{\text{PORESET}}$                                                                       | P1                     | Input (3.3V only)                           |
| $\overline{\text{RSTCONF}}$                                                                       | K4                     | Input (3.3V only)                           |
| $\overline{\text{HRESET}}$                                                                        | J4                     | Open-drain                                  |

Table 30. Pin Assignments - JEDEC Standard (continued)

| Name                  | Pin Number | Type                                                     |
|-----------------------|------------|----------------------------------------------------------|
| SRESET                | M3         | Open-drain                                               |
| XTAL                  | N1         | Analog Output                                            |
| EXTAL                 | M1         | Analog Input (1.8V only)                                 |
| CLKOUT                | N6         | Output                                                   |
| EXTCLK                | N2         | Input (1.8V only)                                        |
| ALE_A                 | H1         | Output                                                   |
| CE1_A                 | E5         | Output                                                   |
| CE2_A                 | B3         | Output                                                   |
| WAIT_A                | N3         | Input (3.3V only)                                        |
| IP_A0                 | T2         | Input (3.3V only)                                        |
| IP_A1                 | M6         | Input (3.3V only)                                        |
| IP_A2<br>IOIS16_A     | R3         | Input (3.3V only)                                        |
| IP_A3                 | M5         | Input (3.3V only)                                        |
| IP_A4                 | T3         | Input (3.3V only)                                        |
| IP_A5                 | N5         | Input (3.3V only)                                        |
| IP_A6                 | M7         | Input (3.3V only)                                        |
| IP_A7                 | R2         | Input (3.3V only)                                        |
| DSCK                  | H2         | Bidirectional<br>Three-state (3.3V only)                 |
| IWP[0:1]<br>VFLS[0:1] | H3, G1     | Bidirectional (3.3V only)                                |
| OP0                   | K1         | Bidirectional (3.3V only)                                |
| OP1                   | K2         | Output                                                   |
| OP2<br>MODCK1<br>STS  | K3         | Bidirectional (3.3V only)                                |
| OP3<br>MODCK2<br>DSDO | L1         | Bidirectional (3.3V only)                                |
| BADDR[28:29]          | L3, L2     | Output                                                   |
| BADDR30<br>REG        | J3         | Output                                                   |
| AS                    | J2         | Input (3.3V only)                                        |
| PA11<br>RXD3          | E16        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |



Table 30. Pin Assignments - JEDEC Standard (continued)

| Name                         | Pin Number | Type                                                     |
|------------------------------|------------|----------------------------------------------------------|
| PA10<br>TXD3                 | H15        | Bidirectional<br>(5V tolerant)                           |
| PA9<br>RXD4                  | J16        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |
| PA8<br>TXD4                  | J15        | Bidirectional<br>(5V tolerant)                           |
| PA3<br>CLK5<br>BRGO3<br>TIN3 | K16        | Bidirectional<br>(5V tolerant)                           |
| PA2<br>CLK6<br>TOUT3         | K14        | Bidirectional<br>(5V tolerant)                           |
| PA1<br>CLK7<br>BRGO4<br>TIN4 | L15        | Bidirectional<br>(5V tolerant)                           |
| PA0<br>CLK8<br>TOUT4         | M16        | Bidirectional<br>(5V tolerant)                           |
| PB31<br>SPISEL               | E13        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |
| PB30<br>SPICLK               | F13        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |
| PB29<br>SPIMOSI              | D15        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |
| PB28<br>SPIMISO<br>BRGO4     | G13        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |
| PB25<br>SMTXD1               | H14        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |
| PB24<br>SMRXD1               | H16        | Bidirectional<br>(Optional: Open-drain)<br>(5V tolerant) |
| PB15<br>BRGO3                | L16        | Bidirectional<br>(5V tolerant)                           |

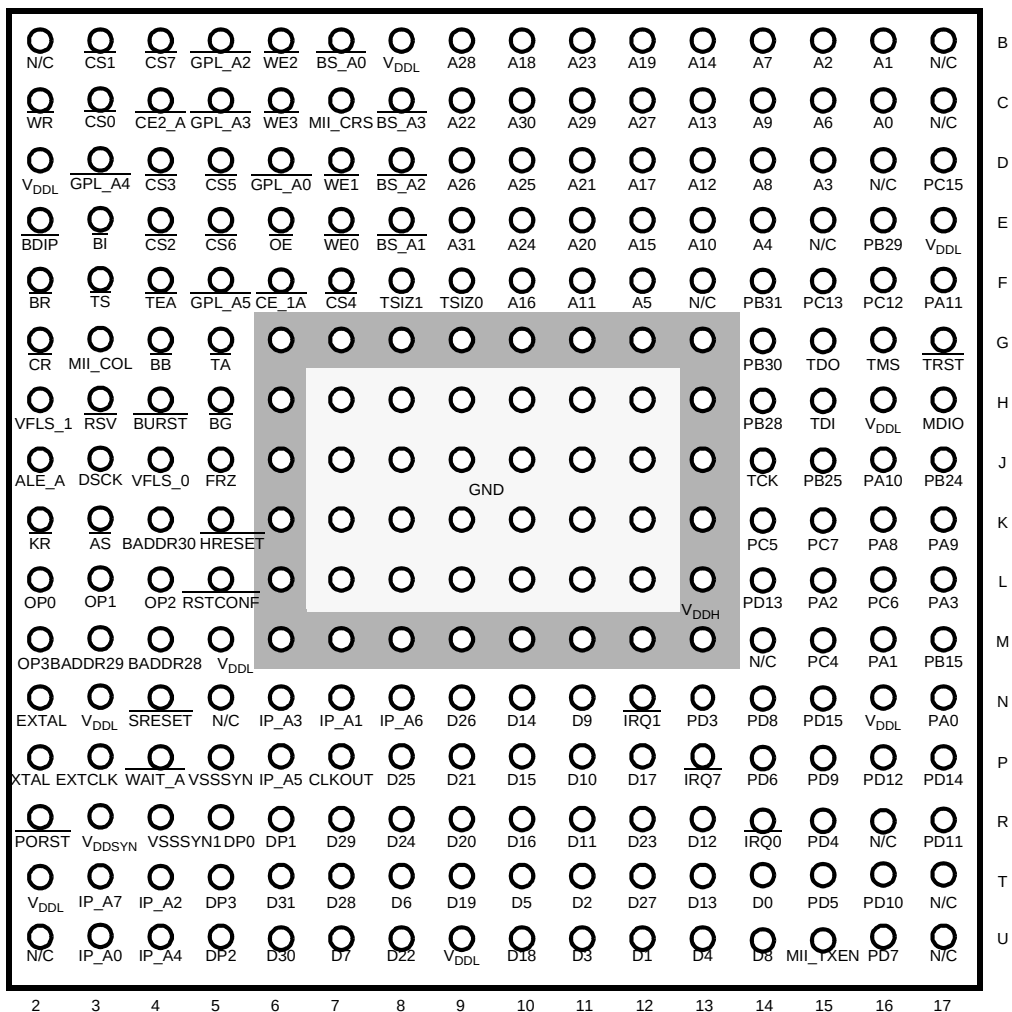
Table 30. Pin Assignments - JEDEC Standard (continued)

| Name                      | Pin Number | Type                           |
|---------------------------|------------|--------------------------------|
| PC15<br>DREQ0             | C16        | Bidirectional<br>(5V tolerant) |
| PC13<br>RTS3              | E14        | Bidirectional<br>(5V tolerant) |
| PC12<br>RTS4              | E15        | Bidirectional<br>(5V tolerant) |
| PC7<br>CTS3               | J14        | Bidirectional<br>(5V tolerant) |
| PC6<br>CD3                | K15        | Bidirectional<br>(5V tolerant) |
| PC5<br>CTS4<br>SDACK1     | J13        | Bidirectional<br>(5V tolerant) |
| PC4<br>CD4                | L14        | Bidirectional<br>(5V tolerant) |
| PD15<br>MII_RXD3          | M14        | Bidirectional<br>(5V tolerant) |
| PD14<br>MII_RXD2          | N16        | Bidirectional<br>(5V tolerant) |
| PD13<br>MII_RXD1          | K13        | Bidirectional<br>(5V tolerant) |
| PD12<br>MII_MDC           | N15        | Bidirectional<br>(5V tolerant) |
| PD11<br>RXD3<br>MII_TX_ER | P16        | Bidirectional<br>(5V tolerant) |
| PD10<br>TXD3<br>MII_RXD0  | R15        | Bidirectional<br>(5V tolerant) |
| PD9<br>RXD4<br>MII_TXD0   | N14        | Bidirectional<br>(5V tolerant) |
| PD8<br>TXD4<br>MII_RX_CLK | M13        | Bidirectional<br>(5V tolerant) |
| PD7<br>RTS3<br>MII_RX_ER  | T15        | Bidirectional<br>(5V tolerant) |

Table 30. Pin Assignments - JEDEC Standard (continued)

| Name                     | Pin Number                                                                                               | Type                           |
|--------------------------|----------------------------------------------------------------------------------------------------------|--------------------------------|
| PD6<br>RTS4<br>MII_RX_DV | N13                                                                                                      | Bidirectional<br>(5V tolerant) |
| PD5<br>MII_TXD3          | R14                                                                                                      | Bidirectional<br>(5V tolerant) |
| PD4<br>MII_TXD2          | P14                                                                                                      | Bidirectional<br>(5V tolerant) |
| PD3<br>MII_TXD1          | M12                                                                                                      | Bidirectional<br>(5V tolerant) |
| TMS                      | F15                                                                                                      | Input<br>(5V tolerant)         |
| TDI<br>DSDI              | G14                                                                                                      | Input<br>(5V tolerant)         |
| TCK<br>DSCK              | H13                                                                                                      | Input<br>(5V tolerant)         |
| TRST                     | F16                                                                                                      | Input<br>(5V tolerant)         |
| TDO<br>DSDO              | F14                                                                                                      | Output<br>(5V tolerant)        |
| MIICRS                   | B6                                                                                                       | Input                          |
| MIIMDIO                  | G16                                                                                                      | Bidirectional<br>(5V tolerant) |
| MIITXEN                  | T14                                                                                                      | Output<br>(5V tolerant)        |
| MIICOL                   | F2                                                                                                       | Input                          |
| V <sub>SSSYN</sub>       | N4                                                                                                       | PLL analog GND                 |
| V <sub>SSSYN1</sub>      | P3                                                                                                       | PLL analog GND                 |
| V <sub>DDSYN</sub>       | P2                                                                                                       | PLL analog V <sub>DD</sub>     |
| GND                      | G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11   | Power                          |
| VDDL                     | A7, C1, D16, G15, L4, M2, R1, M15, T8                                                                    | Power                          |
| VDDH                     | F5, F6, F7, F8, F9, F10, F11, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L8, L9, L10, L11, L12 | Power                          |
| N/C                      | A1, A16, B16, C15, D14, E12, L13, M4, P15, R16, T1, T16                                                  | No-connect                     |

**NOTE: This figure shows the top view of the device.**



### Figure 63. Pinout of the PBGA Package - non-JEDEC

Table 31 contains a list of the MPC852T input and output signals and shows multiplexing and pin assignments.

**Table 31. Pin Assignments - non-JEDEC**

| Name                           | Pin Number                                                                                                                                                 | Type                                         |
|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|
| A[0:31]                        | C16, B16, B15, D15, E14, F12, C15, B14, D14, C14, E13, F11, D13, C13, B13, E12, F10, D12, B10, B12, E11, D11, C9, B11, E10, D10, D9, C12, B9, C11, C10, E9 | Bidirectional<br>Three-state (3.3 V only)    |
| TSIZ0<br>REG                   | F9                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| TSIZ1                          | F8                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| RD/WR                          | C2                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| BURST                          | H4                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| BDIP<br>GPL_B5                 | E2                                                                                                                                                         | Output                                       |
| TS                             | F3                                                                                                                                                         | Bidirectional<br>Active Pull-up (3.3 V only) |
| TA                             | G5                                                                                                                                                         | Bidirectional<br>Active Pull-up (3.3 V only) |
| TEA                            | F4                                                                                                                                                         | Open-drain                                   |
| BI                             | E3                                                                                                                                                         | Bidirectional<br>Active Pull-up (3.3 V only) |
| IRQ2<br>RSV                    | H3                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| IRQ4<br>KR<br>RETRY<br>SPKROUT | K2                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| CR<br>IRQ3                     | G2                                                                                                                                                         | Input (3.3 V only)                           |
| D[0:31]                        | T14, U12, T11, U11, U13, T10, T8, U7, U14, N11, P11, R11, R13, T13, N10, P10, R10, P12, U10, T9, R9, P9, U8, R12, R8, P8, N9, T12, T7, R7, U6, T6          | Bidirectional<br>Three-state (3.3 V only)    |
| DP0<br>IRQ3                    | R5                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| DP1<br>IRQ4                    | R6                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| DP2<br>IRQ5                    | U5                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |
| DP3<br>IRQ6                    | T5                                                                                                                                                         | Bidirectional<br>Three-state (3.3 V only)    |

Table 31. Pin Assignments - non-JEDEC (continued)

| Name                                                                                              | Pin Number             | Type                                         |
|---------------------------------------------------------------------------------------------------|------------------------|----------------------------------------------|
| $\overline{\text{BR}}$                                                                            | F2                     | Bidirectional (3.3 V only)                   |
| $\overline{\text{BG}}$                                                                            | H5                     | Bidirectional (3.3 V only)                   |
| $\overline{\text{BB}}$                                                                            | G4                     | Bidirectional<br>Active Pull-up (3.3 V only) |
| FRZ<br>$\overline{\text{IRQ6}}$                                                                   | J5                     | Bidirectional (3.3 V only)                   |
| $\overline{\text{IRQ0}}$                                                                          | R14                    | Input (3.3 V only)                           |
| $\overline{\text{IRQ1}}$                                                                          | N12                    | Input (3.3 V only)                           |
| $\overline{\text{IRQ7}}$<br>M_TX_CLK                                                              | P13                    | Input (3.3 V only)                           |
| $\overline{\text{CS}}[0:5]$                                                                       | C3, B3, E4, D4, F7, D5 | Output                                       |
| $\overline{\text{CS6}}$                                                                           | E5                     | Output                                       |
| $\overline{\text{CS7}}$                                                                           | B4                     | Output                                       |
| $\overline{\text{WE0}}$<br>$\overline{\text{BS\_B0}}$<br>$\overline{\text{IORD}}$                 | E7                     | Output                                       |
| $\overline{\text{WE1}}$<br>$\overline{\text{BS\_B1}}$<br>$\overline{\text{IOWR}}$                 | D7                     | Output                                       |
| $\overline{\text{WE2}}$<br>$\overline{\text{BS\_B2}}$<br>$\overline{\text{PCOE}}$                 | B6                     | Output                                       |
| $\overline{\text{WE3}}$<br>$\overline{\text{BS\_B3}}$<br>$\overline{\text{PCWE}}$                 | C6                     | Output                                       |
| $\overline{\text{BS\_A}}[0:3]$                                                                    | B7, E8, D8, C8         | Output                                       |
| $\overline{\text{GPL\_A0}}$<br>$\overline{\text{GPL\_B0}}$                                        | D6                     | Output                                       |
| $\overline{\text{OE}}$<br>$\overline{\text{GPL\_A1}}$<br>$\overline{\text{GPL\_B1}}$              | E6                     | Output                                       |
| $\overline{\text{GPL\_A}}[2:3]$<br>$\overline{\text{GPL\_B}}[2:3]$<br>$\overline{\text{CS}}[2-3]$ | B5, C5                 | Output                                       |
| UPWAITA<br>$\overline{\text{GPL\_A4}}$                                                            | D3                     | Bidirectional (3.3 V only)                   |
| $\overline{\text{GPL\_A5}}$                                                                       | F5                     | Output                                       |
| $\overline{\text{PORESET}}$                                                                       | R2                     | Input (3.3 V only)                           |

Table 31. Pin Assignments - non-JEDEC (continued)

| Name                  | Pin Number | Type                                      |
|-----------------------|------------|-------------------------------------------|
| RSTCONF               | L5         | Input (3.3 V only)                        |
| HRESET                | K5         | Open-drain                                |
| SRESET                | N4         | Open-drain                                |
| XTAL                  | P2         | Analog Output                             |
| EXTAL                 | N2         | Analog Input (3.3 V only)                 |
| CLKOUT                | P7         | Output                                    |
| EXTCLK                | P3         | Input (3.3 V only)                        |
| ALE_A                 | J2         | Output                                    |
| CE1_A                 | F6         | Output                                    |
| CE2_A                 | C4         | Output                                    |
| WAIT_A                | P4         | Input (3.3 V only)                        |
| IP_A0                 | U3         | Input (3.3 V only)                        |
| IP_A1                 | N7         | Input (3.3 V only)                        |
| IP_A2<br>IOIS16_A     | T4         | Input (3.3 V only)                        |
| IP_A3                 | N6         | Input (3.3 V only)                        |
| IP_A4                 | U4         | Input (3.3 V only)                        |
| IP_A5                 | P6         | Input (3.3 V only)                        |
| IP_A6                 | N8         | Input (3.3 V only)                        |
| IP_A7                 | T3         | Input (3.3 V only)                        |
| DACK                  | J3         | Bidirectional<br>Three-state (3.3 V only) |
| IWP[0:1]<br>VFLS[0:1] | J4, H2     | Bidirectional (3.3 V only)                |
| OP0                   | L2         | Bidirectional (3.3 V only)                |
| OP1                   | L3         | Output                                    |
| OP2<br>MODCK1<br>STS  | L4         | Bidirectional (3.3 V only)                |
| OP3<br>MODCK2<br>DSDO | M2         | Bidirectional (3.3 V only)                |
| BADDR[28:29]          | M4, M3     | Output                                    |
| BADDR30<br>REG        | K4         | Output                                    |

Table 31. Pin Assignments - non-JEDEC (continued)

| Name                              | Pin Number | Type                                                      |
|-----------------------------------|------------|-----------------------------------------------------------|
| $\overline{AS}$                   | K3         | Input (3.3 V only)                                        |
| PA11<br>RXD3                      | F17        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PA10<br>TXD3                      | J16        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PA9<br>RXD4                       | K17        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PA8<br>TXD4                       | K16        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PA3<br>CLK5<br>BRGO3<br>TIN3      | L17        | Bidirectional<br>(5 V-tolerant)                           |
| PA2<br>CLK6<br>$\overline{TOUT3}$ | L15        | Bidirectional<br>(5 V-tolerant)                           |
| PA1<br>CLK7<br>BRGO4<br>TIN4      | M16        | Bidirectional<br>(5 V-tolerant)                           |
| PA0<br>CLK8<br>$\overline{TOUT4}$ | N17        | Bidirectional<br>(5 V-tolerant)                           |
| PB31<br>$\overline{SPISEL}$       | F14        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PB30<br>SPICLK                    | G14        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PB29<br>SPIMOSI                   | E16        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PB28<br>SPIMISO<br>BRGO4          | H14        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |



Table 31. Pin Assignments - non-JEDEC (continued)

| Name                         | Pin Number | Type                                                      |
|------------------------------|------------|-----------------------------------------------------------|
| PB25<br>SMTXD1               | J15        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PB24<br>SMRXD1               | J17        | Bidirectional<br>(Optional: Open-drain)<br>(5 V-tolerant) |
| PB15<br>BRGO3                | M17        | Bidirectional<br>(5 V-tolerant)                           |
| PC15<br><u>DREQ0</u>         | D17        | Bidirectional<br>(5 V-tolerant)                           |
| PC13<br><u>RTS3</u>          | F15        | Bidirectional<br>(5 V-tolerant)                           |
| PC12<br><u>RTS4</u>          | F16        | Bidirectional<br>(5 V-tolerant)                           |
| PC7<br><u>CTS3</u>           | K15        | Bidirectional<br>(5 V-tolerant)                           |
| PC6<br><u>CD3</u>            | L16        | Bidirectional<br>(5 V-tolerant)                           |
| PC5<br><u>CTS4</u><br>SDACK1 | K14        | Bidirectional<br>(5 V-tolerant)                           |
| PC4<br><u>CD4</u>            | M15        | Bidirectional<br>(5 V-tolerant)                           |
| PD15<br>MII_RXD3             | N15        | Bidirectional<br>(5 V-tolerant)                           |
| PD14<br>MII_RXD2             | P17        | Bidirectional<br>(5 V-tolerant)                           |
| PD13<br>MII_RXD1             | L14        | Bidirectional<br>(5 V-tolerant)                           |
| PD12<br>MII_MDC              | P16        | Bidirectional<br>(5 V-tolerant)                           |
| PD11<br>RXD3<br>MII_TX_ER    | R17        | Bidirectional<br>(5 V-tolerant)                           |
| PD10<br>TXD3<br>MII_RXD0     | T16        | Bidirectional<br>(5 V-tolerant)                           |

Table 31. Pin Assignments - non-JEDEC (continued)

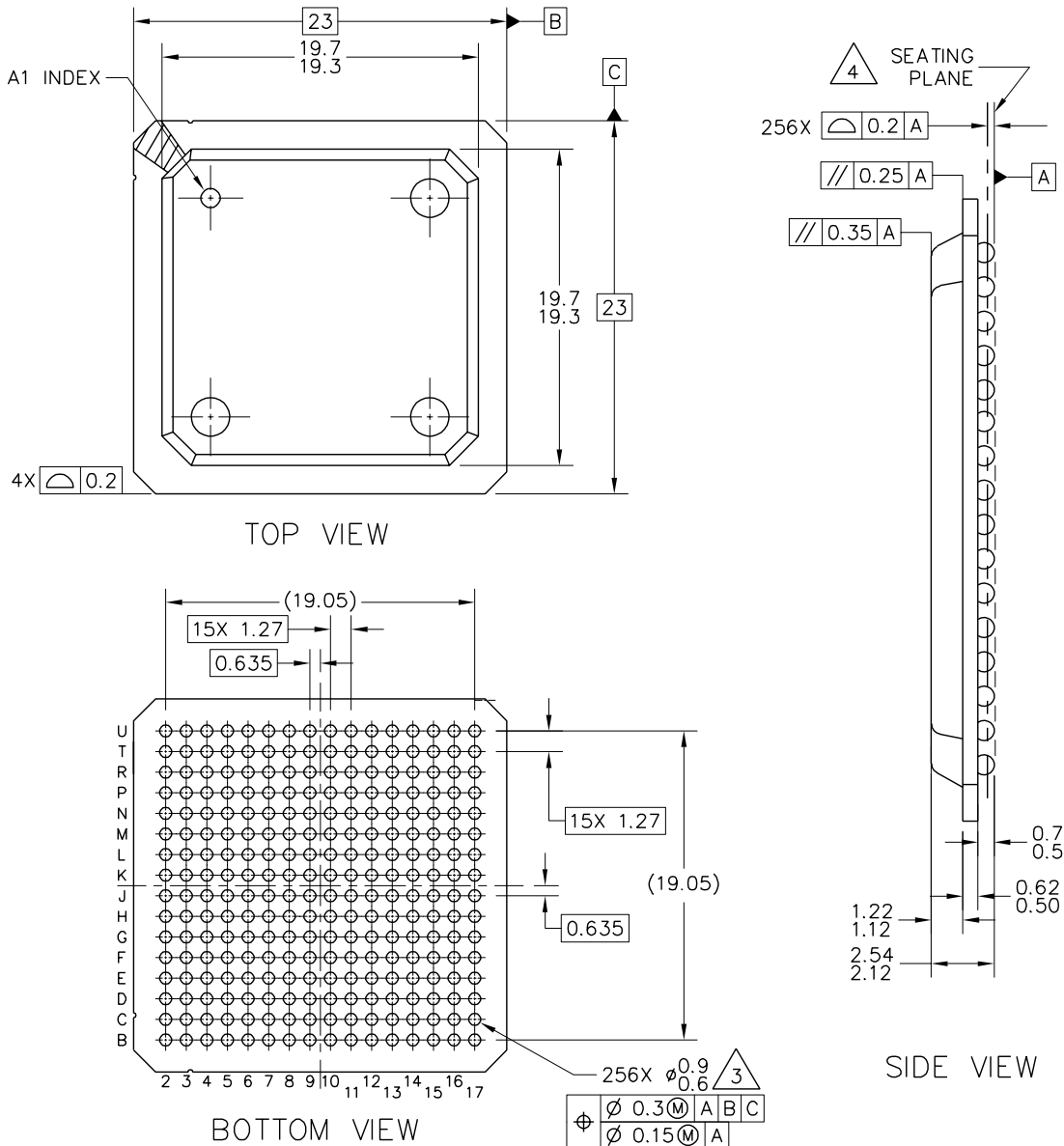
| Name                      | Pin Number | Type                            |
|---------------------------|------------|---------------------------------|
| PD9<br>RXD4<br>MII_TXD0   | P15        | Bidirectional<br>(5 V-tolerant) |
| PD8<br>TXD4<br>MII_RX_CLK | N14        | Bidirectional<br>(5 V-tolerant) |
| PD7<br>RTS3<br>MII_RX_ER  | U16        | Bidirectional<br>(5 V-tolerant) |
| PD6<br>RTS4<br>MII_RX_DV  | P14        | Bidirectional<br>(5 V-tolerant) |
| PD5<br>MII_TXD3           | T15        | Bidirectional<br>(5 V-tolerant) |
| PD4<br>MII_TXD2           | R15        | Bidirectional<br>(5 V-tolerant) |
| PD3<br>MII_TXD1           | N13        | Bidirectional<br>(5 V-tolerant) |
| TMS                       | G16        | Input<br>(5 V-tolerant)         |
| TDI<br>DSDI               | H15        | Input<br>(5 V-tolerant)         |
| TCK<br>DSCK               | J14        | Input<br>(5 V-tolerant)         |
| TRST                      | G17        | Input<br>(5 V-tolerant)         |
| TDO<br>DSDO               | G15        | Output<br>(5 V-tolerant)        |
| MII_CRS                   | C7         | Input                           |
| MII_MDIO                  | H17        | Bidirectional<br>(5 V-tolerant) |
| MII_TX_EN                 | U15        | Output<br>(5 V-tolerant)        |
| MII_COL                   | G3         | Input                           |
| V <sub>SSSYN</sub>        | P5         | PLL analog GND                  |
| V <sub>SSSYN1</sub>       | R4         | PLL analog GND                  |
| V <sub>DDSYN</sub>        | R3         | PLL analog V <sub>DD</sub>      |

**Table 31. Pin Assignments - non-JEDEC (continued)**

| Name             | Pin Number                                                                                                 | Type       |
|------------------|------------------------------------------------------------------------------------------------------------|------------|
| GND              | H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12 | Power      |
| V <sub>DDL</sub> | B8, D2, E17, H16, M5, N3, T2, N16, U9                                                                      | Power      |
| V <sub>DDH</sub> | G6, G7, G8, G9, G10, G11, G12, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M7, M8, M9, M10, M11, M12, M13 | Power      |
| N/C              | B2, B17, C17, D16, E15, F13, M14, N5, R16, T17, U2, U17                                                    | No-connect |

## 16.2 Mechanical Dimensions of the PBGA Package

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, refer to Plastic Ball Grid Array Application Note (order number: AN1231/D) that is available from your local Motorola sales office. [Figure 64](#) shows the mechanical dimensions of the PBGA package.

**NOTES:**

1. All dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M—1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.

**Note:** Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC852TVRXXX.

Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC852TZTXXX.

**Figure 64. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package**

# 17 Document Revision History

Table 32 lists significant changes between revisions of this document.

**Table 32. Document Revision History**

| Revision | Date      | Changes                                                                                                                                                                                                                                                                                                                                  |
|----------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3.1      | 1/18/2005 | Document template update.                                                                                                                                                                                                                                                                                                                |
| 3.0      | 11/2004   | <ul style="list-style-type: none"> <li>Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values</li> <li>Added a footnote to Spec 41 specifying that EDM = 1</li> <li>Broke the <a href="#">Section 16.1, "Pin Assignments,"</a> into 2 smaller sections for the JEDEC and non-JEDEC pinouts.</li> </ul> |
| 2.0      | 12/2003   | Put 852T on the 1st page in place of 8245.<br>Figure 62 on page 59 had overbars added on signals CR (pin G2) and WAIT_A (pin P4).                                                                                                                                                                                                        |
| 1.8      | 7/2003    | Changed the pinout to be JEDEC Compliant, changed timing parameters B28a through B28d, and B29d to show that TRLX can be 0 or 1.                                                                                                                                                                                                         |
| 1.7      | 5/2003    | Changed the SPI Master Timing Specs. 162 and 164                                                                                                                                                                                                                                                                                         |
| 1.6      | 4/2003    | Changed the package drawing in Figure 15-63                                                                                                                                                                                                                                                                                              |
| 1.5      | 4/2003    | Changed 5 Port C pins with interrupt capability to 7 Port C pins. Added the Note: solder sphere composition for MPC852TVR and MPC852TCVR devices is 95.5%Sn 45%Ag 0.5%Cu to Figure 15-63                                                                                                                                                 |
| 1.4      | 2/2003    | Changed Table 15-30 Pin Assignments for the PLL Pins $V_{SSYN1}$ , $V_{SSYN}$ , $V_{DDSYN}$                                                                                                                                                                                                                                              |
| 1.3      | 1/2003    | Added subscripts to timing diagrams for B1-B35, to specify memory controller settings for the specific edges.                                                                                                                                                                                                                            |
| 1.2      | 1/2003    | In Table 15-30, specified EXTCLK as 3.3 V.                                                                                                                                                                                                                                                                                               |
| 1.1      | 12/2002   | Added fast Ethernet controller to the features                                                                                                                                                                                                                                                                                           |
| 1        | 11/2002   | Added values for 80 and 100 MHz                                                                                                                                                                                                                                                                                                          |
| 0        | 10/2002   | Initial release                                                                                                                                                                                                                                                                                                                          |

**THIS PAGE INTENTIONALLY LEFT BLANK**

## **How to Reach Us:**

### **Home Page:**

www.freescale.com

### **email:**

support@freescale.com

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
(800) 521-6274  
480-768-2130  
support@freescale.com

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
support@freescale.com

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Technical Information Center  
3-20-1, Minami-Azabu, Minato-ku  
Tokyo 106-0047 Japan  
0120 191014  
+81 3 3440 3569  
support.japan@freescale.com

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate,  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
support.asia@freescale.com

### **For Literature Requests Only:**

Freescale Semiconductor  
Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
(800) 441-2447  
303-675-2140  
Fax: 303-675-2150  
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. The described product contains a PowerPC processor core. The PowerPC name is a trademark of IBM Corp. and used under license. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2005.

MPC852TEC  
Rev. 3.1  
01/2005

