DS4000
Digitally Controlled (DC)-TCXO

www.maxim-ic.com

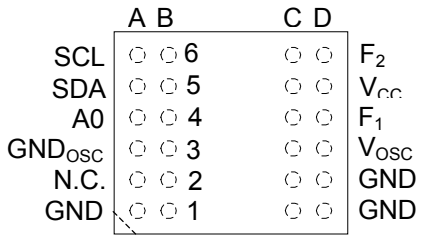
FEATURES

- Aging ≤1.0ppm per year
- Frequency stability ±1.0ppm from -40°C to +85°C
- Frequency versus supply stability of ±1.0ppm per volt
  - Base frequency is digitally tunable by ±6.0ppm
  - One fixed-frequency output and one (n + 1) or 2(n + 1) division of the base frequency output.
- Temperature measurements from -40C° to +85°C with 10-bit/+0.25°C resolution and ±3°C accuracy
- 2-wire serial interface

APPLICATIONS

- Reference Oscillators in PLL Circuits
- Global Positioning Systems
- SATCOM
- Telecom
- Wireless Base Stations

PIN ASSIGNMENT (Top View)



BGA

PIN DESCRIPTION

V_{CC}	- Power Supply
GND	- Ground
V_{OSC}	- Oscillator Power Supply
GND_{OSC}	- Oscillator Ground
SDA	- 2-Wire Serial-Data Input/Output
SCL	- 2-Wire Serial Clock
A_0	- 2-Wire Serial-Address Input
F_2, F_1	- DC-TCXO Outputs
N.C.	- No Connection (do not connect)

ORDERING INFORMATION

PART	PIN-PACKAGE	TOP MARK	FREQUENCY DESIGNATOR (MHz)
DS4000A0/BGA	12 BGA	DS4000A0	10.00000
DS4000CW/BGA	12 BGA	DS4000CW	12.80000
DS4000D0BGA	12 BGA	DS4000D0	13.00000
DS4000EC/BGA	12 BGA	DS4000EC	14.31818
DS4000G0/BGA	12 BGA	DS4000G0	16.00000
DS4000GF/BGA	12 BGA	DS4000GF	16.38400
DS4000GW/BGA	12 BGA	DS4000GW	16.80000
DS4000KI/BGA	12 BGA	DS4000KI	19.44000

DESCRIPTION

The DS4000 digitally controlled temperature-compensated crystal oscillator (DC-TCXO) features a digital temperature sensor, one fixed-frequency temperature-compensated square-wave output (F_1), one programmable temperature-compensated square-wave output (F_2), and digital communication for frequency tuning (SDA, SCL).

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://www.maxim-ic.com/errata.*

SIGNAL DESCRIPTIONS

V_{CC}, GND – DC power is provided to the device on these pins.

V_{OSC}, GND_{OSC} – DC power is provided to the oscillator on these pins.

SDA (Serial-Data Input/Output) – SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open drain and requires an external pullup resistor.

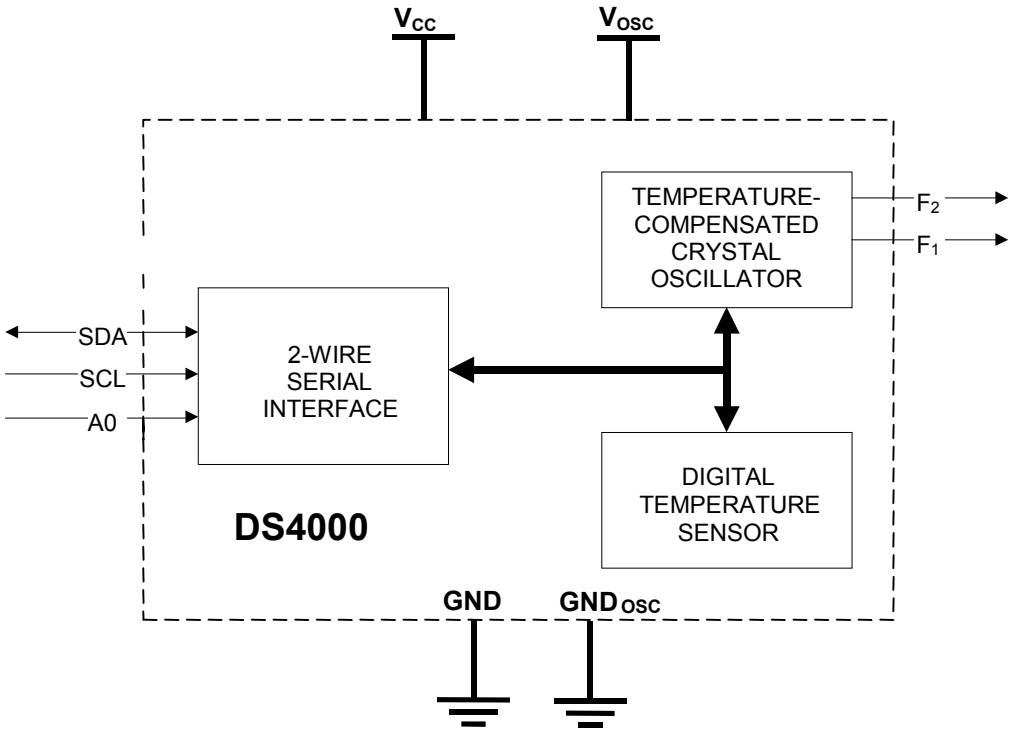
SCL (Serial-Clock Input) – SCL is used to synchronize data movement on the serial interface. The SCL pin is open drain and requires an external pullup resistor.

A_0 – 2-wire slave address input. This pin is used to configure the slave address.

F_2, F_1 – DC-TCXO frequency outputs.

N.C. – Do not connect.

Figure 1. BLOCK DIAGRAM



TEMPERATURE-COMPENSATED CRYSTAL OSCILLATOR

The DS4000 can either function as a standalone TCXO or as a digitally controlled TCXO. When used as a standalone TCXO, the only requirements needed to function properly are power, ground, and an output. However, the 2-wire interface must be used to tune (push and pull) the crystal.

The DS4000 is capable of supplying two different outputs, F_1 and F_2.

1) F_1 is the base frequency of the crystal unit inside of the device. The output type is a CMOS square wave.
2) F_2 is a programmable frequency output. The frequency select register can program this output to an integer division of the base (F_1) frequency. The duty cycle (DC) bit determines if the output is an n + 1 or a 2(n + 1) division of F_1.

F_2 FREQUENCY SELECT REGISTER (FSR) (5Dh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
D7	D6	D5	D4	D3	D2	D1	D0

$F_2 = F_1 / (FSR\ value + 1)$; with DC = 0
$F_2 = F_1 / [2 \times (FSR\ value + 1)]$; with DC = 1

TCXO CONTROL REGISTER (60h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	F_2OE	F_1OE	F_T	DC

DC – Duty Cycle Bit. If 50% duty cycle is desired, then this bit must be set to logic 1. The default condition at power-up is logic 0.

F_T – This bit must be programmed by the user to a 0.

F_1OE – F_1 Output Enable Bit. This bit allows the user to disable/enable the F_1 output.

F_2OE – F_2 Output Enable Bit. This bit allows the user to disable/enable the F_2 output.

Digital Tuning the Base Crystal Frequency

When using the 2-wire interface for tuning the base frequency, the frequency tuning register is used. The frequency tuning register contains two's complement data. The data is used to add or subtract an offset from the crystal loading register. When the tuning register is programmed with a value, the next temperature-update cycle sums the programmed value with the factory-compensated value. This allows the user/system to digitally control the base frequency by a microcontroller using the 2-wire protocol.

FREQUENCY TUNING REGISTER (66h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SIGN	FO6	FO5	FO4	FO3	FO2	FO1	FO0

FOS[6:0] – Frequency Offset. These bits are used to tune the base crystal frequency. Each bit represents approximately 0.05ppm and, therefore, for a value of 07FH, pushes or pulls the base frequency by approximately 6.35ppm.

SIGN – Sign Bit. This bit is used to determine whether to add or subtract the frequency offset from the crystal loading.

Table 1. FREQUENCY TUNING RELATIONSHIP

CALCULATED FREQUENCY OFFSET (ppm)	DIGITAL DATA (Binary)	DIGITAL DATA (hex)
+6.35	0111 1111	7Fh
+5.0	0110 0100	64h
+3.3	0100 0010	42h
+1.2	0001 0111	17h
+0.05	0000 0001	01h
0.0	0000 0000	00h
-0.05	1111 1111	FFh
-1.2	1110 1000	E8h
-3.3	1011 0011	B3h
-5.0	1001 1100	9Ch
-6.35	1000 0000	80h

DIGITAL TEMPERATURE SENSOR

The digital temperature sensor provides 10-bit temperature readings that indicate the temperature of the device. Temperature readings are communicated from the DS4000 over a 2-wire serial interface. No additional components are required. The DS4000 has an external address bit that allows a user to choose the slave address from two possible values.

Overview

The factory-calibrated temperature sensor requires no external components. Upon power-up, the DS4000 starts performing temperature conversions with a resolution of 10 bits (+0.25°C resolution). Following an 8-bit command protocol, temperature data can be read over the 2-wire interface. The host can periodically read the value in the temperature register, which contains the last completed conversion. As conversions are performed in the background, reading the temperature register does not affect the conversion in progress.

Reading Temperature

The DS4000 measures temperature through the use of an on-chip temperature-measurement technique with an operation range from -40°C to +85°C. The device performs continuous conversions with the most recent result being stored in the temperature register. The digital temperature is retrieved from the temperature register using the READ TEMPERATURE command, as described in detail in the following paragraphs.

Table 2 describes the exact relationship of output data to measured temperature. The data is transmitted serially over the 2-wire serial interface, MSB first. The MSB of the temperature register contains the "sign" (S) bit, denoting whether the temperature is positive or negative. For Fahrenheit usage, a lookup table or conversion routine must be used.

TEMPERATURE/DATA RELATIONSHIP (UNIT = °C)

MSB (**64h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

LSB (**65h)**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2^{-1}	2^{-2}	0	0	0	0	0	0

Table 2. TEMPERATURE/DATA RELATIONSHIP

TEMPERATURE (°C)	DIGITAL OUTPUT (Binary)	DIGITALOUTPUT (hex)
+85	0101 0101 0000 0000	5500h
+75	0100 1011 0000 0000	4B00h
+0.5	0000 0000 1000 0000	0080h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1000 0000	FF80h
-20	1110 1100 0000 0000	EC00h
-40	1101 1000 0000 0000	D800h

Note: *Internal power dissipation raises the temperature above the ambient. The delta between ambient and the die temperature depends on power consumption, PC board layout, and airflow.*

Read Temperature

This command reads the last temperature conversion result from the temperature register in the format described in the *Reading Temperature* section. If an application can accept temperature resolutions of +1.0°C, then the master can read the first data byte and follow with a NACK and STOP. For higher resolution, both bytes must be read.

Table 3. COMMAND SET

INSTRUCTION	FUNCTION	PROTOCOL	2-WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
Frequency Select Register	Defines F_2 output frequency	5Dh	Read or write 1 data byte	2
TCXO Control Register	Enables/disables F_1 and F_2; sets duty cycle of F_2	60h	Read or write 1 data byte	2
Read Temperature	Reads 10-bit temperature register	64h	Read 1 or 2 data bytes	1, 2
Frequency Tuning Register	Digitally adds/subtracts an offset from oscillator	66h	Read or write 1 data byte	2

NOTES:

1) If the user only desires 8-bit thermometer readings, the master can read one data byte, and follow with a NACK and STOP. If higher resolution is required, both bytes must be read.
2) The slave does not increment the internal address pointer between instructions. The address pointer must be reinitialized after each access.

2-WIRE SERIAL INTERFACE

The DS4000 supports a bidirectional 2-wire serial bus and data transmission protocol. The bus must be controlled by a master device, which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS4000 operates as a slave on the 2-wire bus. The DS4000 works in a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate), which are defined within the bus specifications. Connections to the bus are made by the open-drain I/O signals SDA and SCL.

The following bus protocol has been defined (Figure 1):

- Data transfer can be initiated only when the bus is not busy.
- During data transfer, the data signal must remain stable whenever the clock signal is HIGH. Changes in the data signal while the clock signal is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock signals remain HIGH.

Start Data Transfer: A change in the state of the data signal, from HIGH to LOW, while the clock line is HIGH, defines the START condition.

Stop Data Transfer: A change in the state of the data signal, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

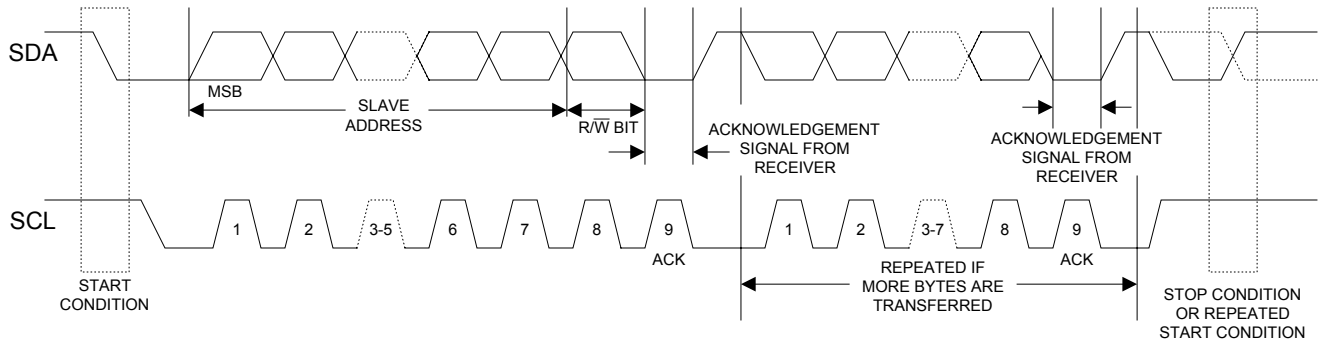
Data Valid: The state of the data signal represents valid data when, after a START condition, the data signal is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is required to generate an acknowledge after reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the serial data (SDA) signal during the acknowledge clock pulse in such a way that the SDA signal is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end-of-data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data signal HIGH to enable the master to generate the STOP condition.

Figure 1. DATA TRANSFER ON 2-WIRE SERIAL BUS



Data Transfer

Figures 2 and 3 detail how data transfer is accomplished on the 2-wire bus.

Depending on the R/$\overline{W}$ bit in the transmission protocols as shown, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

Slave Address

The slave address is the first byte received following the START condition generated by the master device. The address byte consists of a 7-bit slave address and the R/$\overline{W}$ direction bit. The DS4000 slave address is set to 100010A_0, where A_0 is externally hardwired to a HIGH or LOW state. This allows design flexibility to set the slave's address to one of two possible address locations. The last bit following the slave address is the direction bit (R/$\overline{W}$) and defines the operation to be performed by the master, transmit data (R/$\overline{W}$ = 0), or receive data (R/$\overline{W}$ = 1). Following the START condition, the DS4000 monitors the SDA bus by checking the slave address being transmitted. Upon receiving the proper slave address and R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line regardless of the operation mode.

The DS4000 can operate in the following two modes:

1) **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by the hardware after reception of the slave address and direction bit (Figure 2).

2) **Slave Transmitter Mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS4000 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure 3).

Figure 2. DATA WRITE: SLAVE RECEIVER MODE

	<SLAVE ADDRESS>	R/$\overline{W}$		<DATA ADDRESS>		<DATA (n)>		
S	100010A_0	0	A	XXXXXXXX	A	XXXXXXXX	A	P

S = START
A = ACKNOWLEDGE
P = STOP

Figure 3. DATA READ: SLAVE TRANSMITTER MODE

	<SLAVE ADDRESS>	R/$\overline{W}$		<DATA (n)>		<DATA (n + 1)>		<DATA (n + 2)>		<DATA (n + X)>		
S	100010A_0	1	A	XXXXXXXX	A	XXXXXXXX	A	XXXXXXXX	A	XXXXXXXX	$\overline{A}$	P

S = START
A = ACKNOWLEDGE
P = STOP
$\overline{A}$ = NOT ACKNOWLEDGE

ABSOLUTE MAXIMUM RATINGS*

Voltage Range on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +85°C
Soldering Temperature Range	See IPC/JEDEC J-STD-020A (2x max)

** This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS (T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	1, 2
Oscillator Supply Voltage	V_{OSC}	4.75	5.0	5.25	V	1, 2
Input Logic High	V_{IH}	2.2		V_{CC} + 0.3	V	1
Input Logic Low	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 to 5.25V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		1.5	2	mA	3, 4
Active Oscillator Supply Current	I_{OSC}		3.5	5.5	mA	3, 4
Output Logic High 2.4V	I_{OH}	-1			mA	1
Output Logic Low 0.4V	I_{OL}			4	mA	1
Input Leakage	I_{LI}			1	µA	
I/O Leakage	I_{LO}			1	µA	
Temperature Conversion Time	t_{CONVT}		250	300	ms	3

TCXO AC ELECTRICAL CHARACTERISTICS

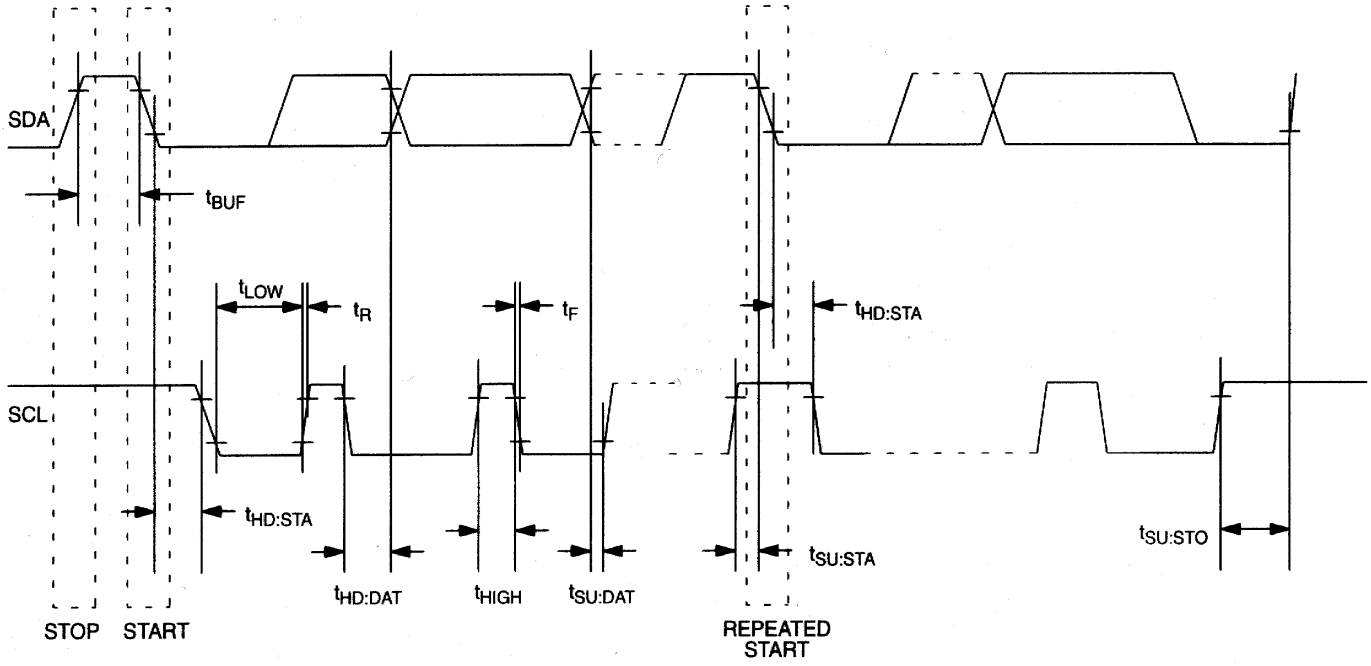
(V_{CC} = 4.75 to 5.25V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency	F_1 F_2	CMOS	10		20	MHz	5
Frequency Stability vs. Temperature	$\Delta F/T_A$		-1.0		+1.0	ppm	
Voltage	$\Delta F/V$					ppm/V	
Aging	$\Delta F/Yr$					ppm/Yr	
F_1, F_2 Rise and Fall Time, 10% to 90%	t_R, t_F			4		ns	
Max Output Capacitive Load	C_L				10	pF	
Duty Cycle	t_W / t		40	50	60	%	
Phase Noise F1 Output, 10kHz	ϕ_N			-130		dBc/Hz	6

2-WIRE SERIAL INTERFACE
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 to 5.25V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	Fast mode	0		400	kHz	
		Standard mode			100		
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast mode	1.3			µs	
		Standard mode	4.7				
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast mode	0.6			µs	7
		Standard mode	4.0				
Low Period of SCL Clock	t_{LOW}	Fast mode	1.3			µs	
		Standard mode	4.7				
High Period of SCL Clock	t_{HIGH}	Fast mode	0.6			µs	
		Standard mode	4.0				
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6			µs	
		Standard mode	4.7				
Data Hold Time	$t_{HD:DAT}$	Fast mode	0		0.9	µs	8
		Standard mode					
Data Setup Time	$t_{SU:DAT}$	Fast mode	100			ns	9
		Standard mode	250				
Rise Time of Both SDA and SCL	t_R	Fast mode	$20 + 0.1C_B$		300	ns	9
		Standard mode			1000		
Fall Time of Both SDA and SCL	t_F	Fast mode	$20 + 0.1C_B$		300	ns	10
		Standard mode			1000		
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6			µs	
		Standard mode	4.0				
Capacitive Load for Each Bus Line	C_B				400	pF	10
Input Capacitance	C_I			5		pF	

Figure 4. TIMING DIAGRAM



NOTES:

1) All voltages are referenced to ground.
2) For ±10% operating range, contact factory.
3) Typical values are at +25°C and nominal supplies.
4) These parameters are measured with the outputs disabled.
5) F_1 is the base frequency as defined by the package markings. F_2 is a programmable frequency output. The output frequency of F_2 is derived from the base frequency, F_1, by programming the F_2 frequency select register and duty cycle (DC) bit in the TCXO control register. The minimum output frequency is $F_1 / (2^8 + 1)$ with DC = 0 and $F_1 / [2 \times (2^8 + 1)]$ with DC = 1.
6) 10MHz, 5V, +25°C with one of the two outputs enabled.
7) After this period, the first clock pulse is generated.
8) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
9) A fast-mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ >250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT}$ (1000 + 250 = 1250ns) before the SCL line is released.
10) C_B: Total capacitance of one bus line in pF.

DS4000 BGA PACKAGE DRAWING

Note: *The BGA is solder-masked defined.*