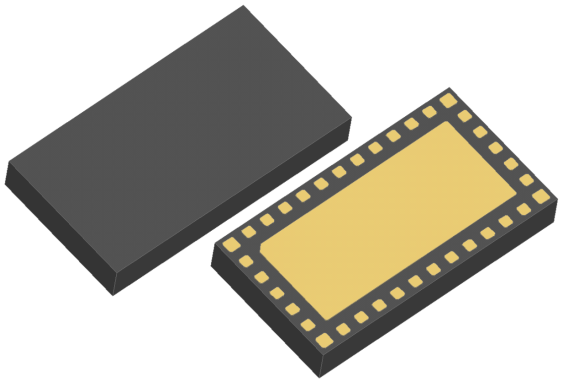
HDMI2C2-14HD

ESD protection and signal booster for HDMI™ 1.4 sink interface

Datasheet – production data



QFN 36L
3.5 X 6.5

Features

- HDMI 1.3 and 1.4 compliant: from -40 to 85 °C
- 8 kV contact ESD protection on connector side
- Supports direct connection to low-voltage HDMI ASIC and/or CEC driver (down to 1.8 V)
- High integration level in 1 package
- TMDS high bandwidth ESD protection
- DDC (I2C) link protection, bi-directional signal conditioning circuit, and dynamic pull-up
- CEC bus protection, bi-directional level-shifter, backdrive protection, and independent structure from main power supply
- HEAC/HPD link protection and line matching
- Proposed in QFN 36 leads 500 µm pitch

Benefits

- Speed-up hardware design and certification of HDMI 1.4 application
- Pin map sequence compliant with HDMI connector type A
- Minimal PCB footprint in consumer area
- Protection of ultra-sensitive HDMI ASICs
- Low power consumption in stand-by mode
- Wake-up from stand-by through CEC bus
- Improved HDMI interface ruggedness and user experience
- Long and/or poor quality cable support
- Companion chip for STMicroelectronics' STixxxx HDMI decoders.

Complies with the following standards

- HDMI 1.4 version
- IEC 61000-4-2 level 4
- JESD22-A114D level 2

Applications

- Consumer and computer electronics HDMI™ sink device such as:
  - HD set-top boxes
  - DVD and Blu-Ray Disk systems
  - Home theater
  - Game console

Description

The HDMI2C2-14HD is a fully integrated ESD protection and signal conditioning device for control links and TMDS data video channels of HDMI receivers (Sink).

The HDMI2C2-14HD is a simple solution that provides HDMI designers with an easy and fast way to reach full compliancy with the stringent HDMI 1.4 CTS on a wide temperature range.

Contents

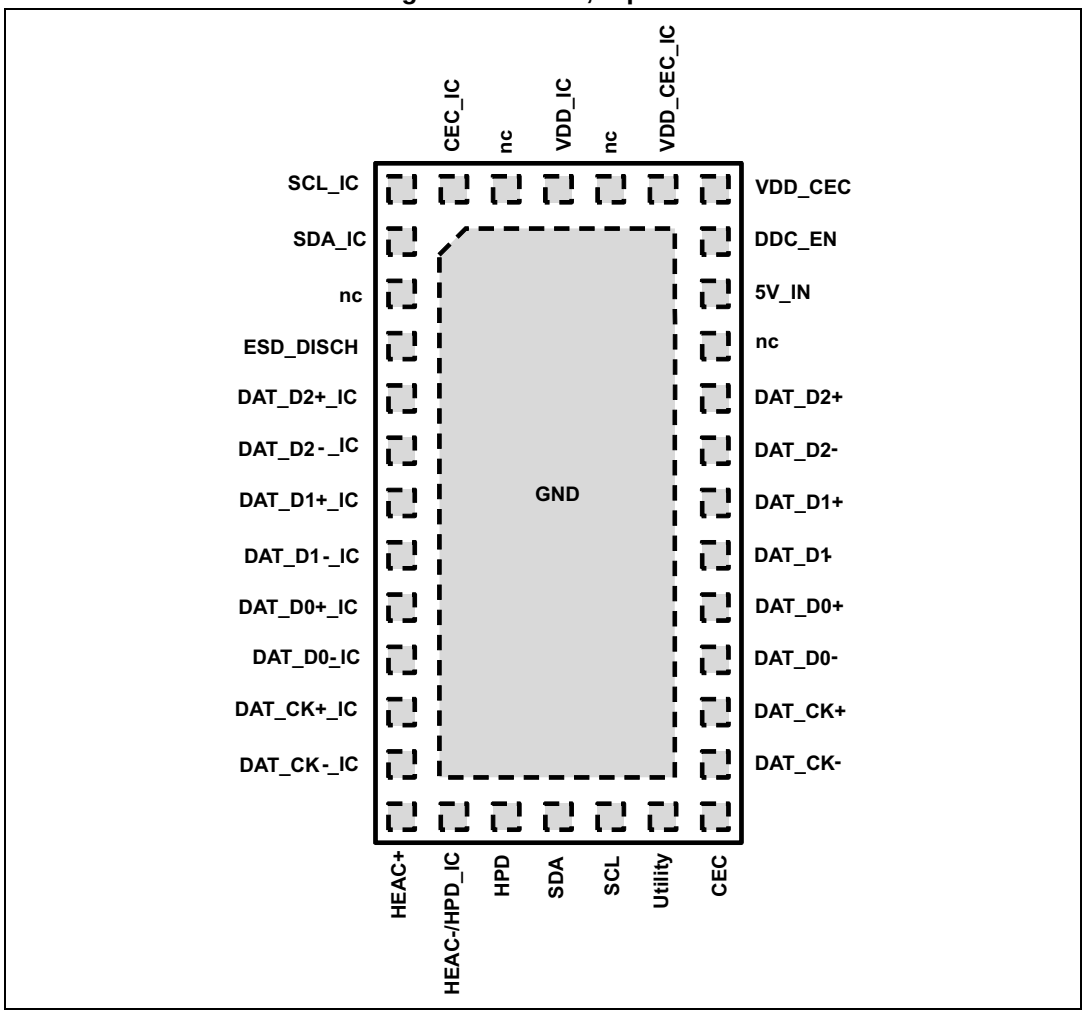
1 Functional description

The HDMI2C2-14HD is a fully integrated ESD protection and signal conditioning device for control links and TMDS data video channels of HDMI receiver (Sink).

The control stage provides a bidirectional buffer, integrating signal conditioning and dynamic pull-up on DDC bus for maximum system robustness and signal integrity. The HEAC (HDMI Ethernet and Audio return Channels) function is supported, making the component fully compliant with HDMI 1.4 version. A bidirectional CEC block is integrated, able to wake-up the application from stand-by mode (all power supply off, except the CEC power supply). The integrated TMDS links ESD protection allows a video data rate up to 10.2 Gbps, corresponding to the maximal speed specified by HDMI standard. All video format specified by HDMI standard (from 720p30 up to 1080p60 3D) are supported, giving maximum flexibility to designer. All these features are provided in a single 36 leads QFN package featuring natural PCB routing and saving space on the board.

The HDMI2C2-14HD is a simple solution that provides HDMI™ designers with an easy and fast way to reach full compliancy with the stringent HDMI 1.4 CTS on a wide temperature range. STMicroelectronics proposes a dual version dedicated for the Sources interfaces: the HDMI2C1-14HD.

Figure 1. Pin out, top view



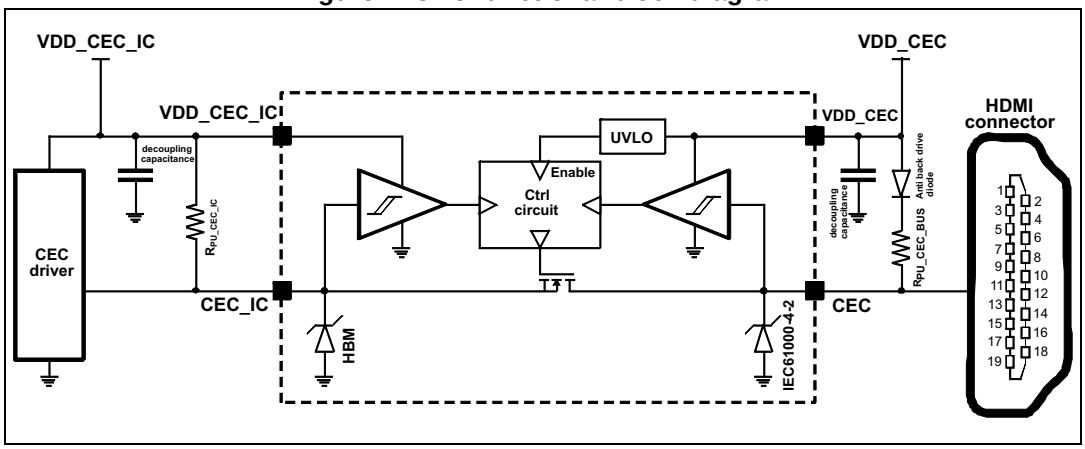
2 Application information

2.1 CEC line description

The CEC bus is described in the HDMI standard as the Consumer Electronics Control. It provides control functions between all the various audiovisual equipments chained in the user's environment.

The CEC block integrated in the HDMI2C2-14HD implements a level shifter, shifting the cable CEC +3.3 V voltage (V_{DD_CEC}) down to the ASIC power supply voltage (V_{DD_IC}) that can be as low as 1.8 V. The *Figure 2* shows the functional diagram of the integrated CEC block.

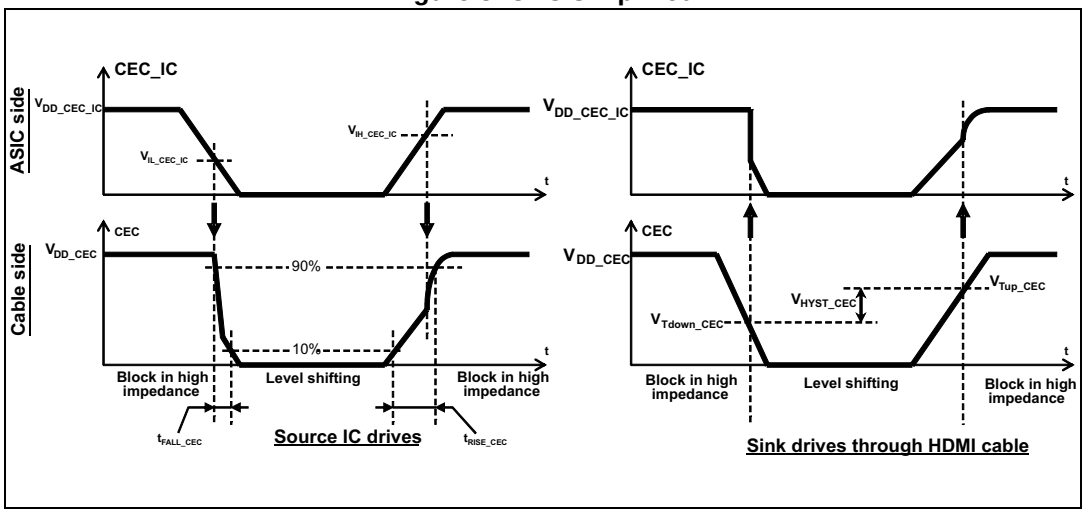
Figure 2. CEC functional block diagram



In case of no activity on the CEC bus, or if the CEC driver is off ($V_{DD\_CEC\_IC}$ = 0), the CEC pin is put in high impedance mode (open circuit) protecting the circuitry and the application against hazardous backdrive.

The *Figure 3* illustrates the normal operating mode of the CEC functional block when either the IC from the source on the sink drives the communication.

Figure 3. CEC simplified



In case the application is set in stand-by mode, the +5 V main supply of the application is generally powered off in order to reduce as much as possible the global power consumption. The CEC driver can be the only device still working in low power mode, allowing a wake up of the whole application through the CEC line. When the main power supply +5 V is switched off, and if the CEC bus is still active (V_{DD_CEC} power in on state), the HDMI2C2-14HD keeps the CEC bus working properly while all other outputs of the component are put in high impedance mode.

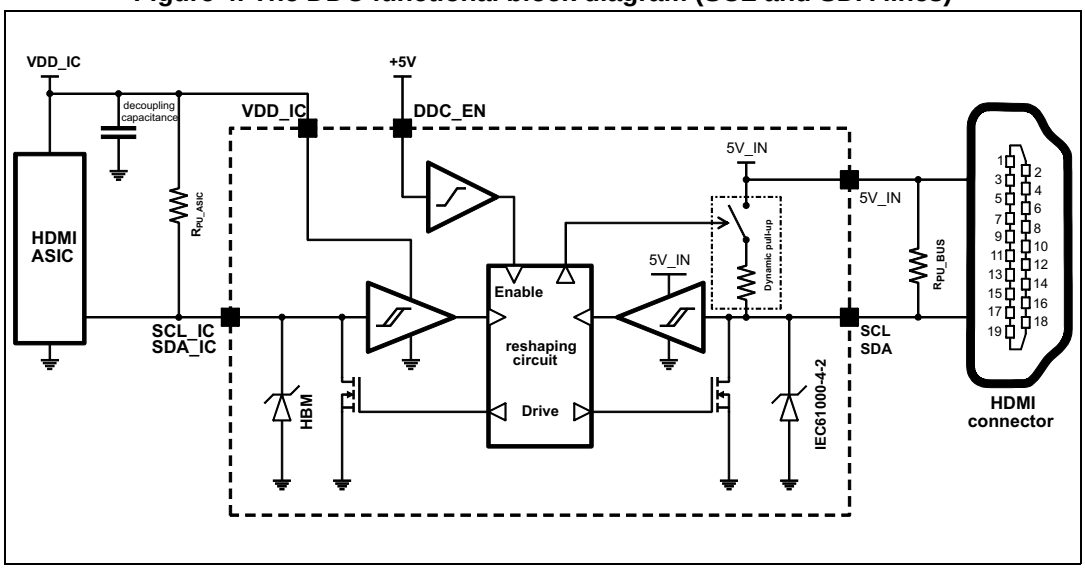
The CEC output (cable side) integrates a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8kV contact).

2.2 DDC functional block description

The DDC bus is described in the HDMI 1.4 standard as the Display Data Channel. The topology corresponds to an I2C bus that must be compliant with the I2C bus specification version 2.1 (January 2000). The DDC bus is made of 2 lines: data line (SDA) and clock line (SCL). It is used to create a point to point communication link from the source to the sink. EEDID and HDCP protocols are flowing through this link, making this I2C communication channel a critical element in the HDMI application.

The DDC block integrated in the HDMI2C2-14HD allows a bidirectional communication between the cable and the ASIC. It is fully compliant with the HDMI 1.4 standard and its CTS, but also with the I2C bus specification version 2.1. The DDC block shifts the electrical and threshold levels of SDA and SCL lines from the +5 V voltage from the cable (V_{5V_IN}) down to the ASIC voltage level (V_{DD_IC}), that can be as low as 1.8 V. The *Figure 4* shows the functional diagram of the DDC block integrated in the HDMI2C2-14HD device.

Figure 4. The DDC functional block diagram (SCL and SDA lines)

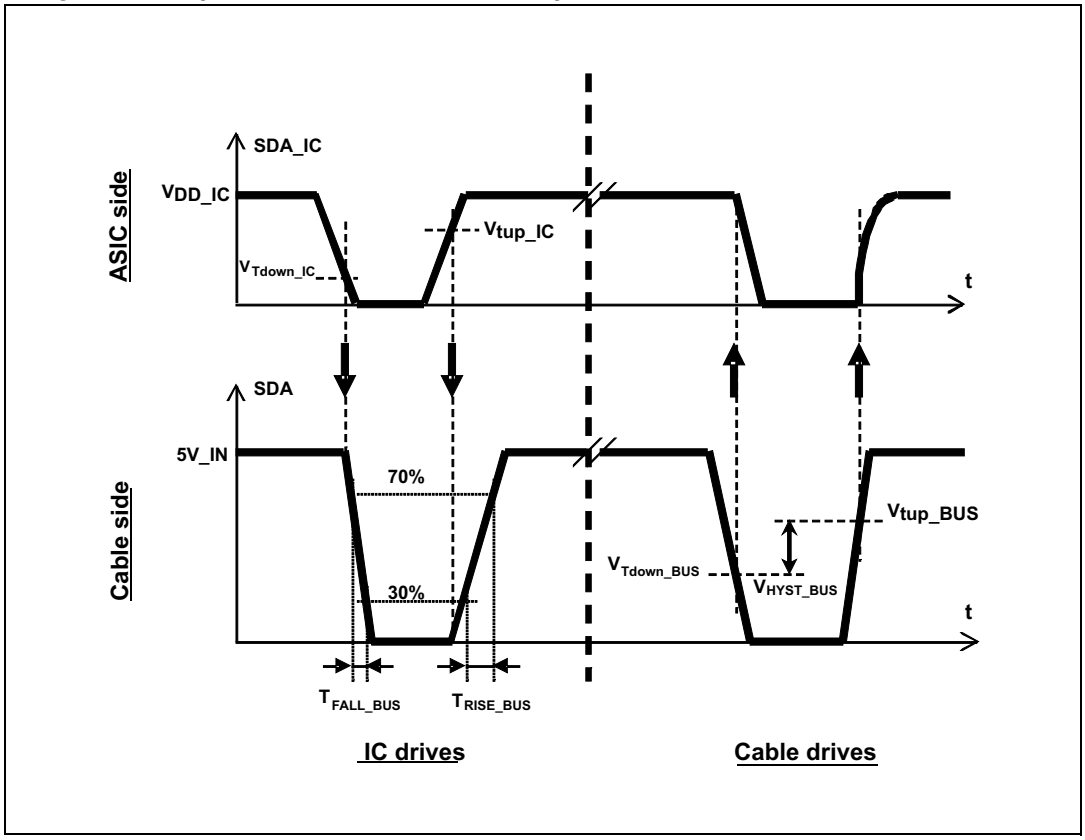


The DDC_EN allows to authorize or not a bidirectional communication through the functional block. It can be connected to the main +5V of the board, or to the ASIC power supply, detecting then if the application is ready for communication or not.

The DDC outputs (SCL and SDA on cable side) integrate a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8kV contact).

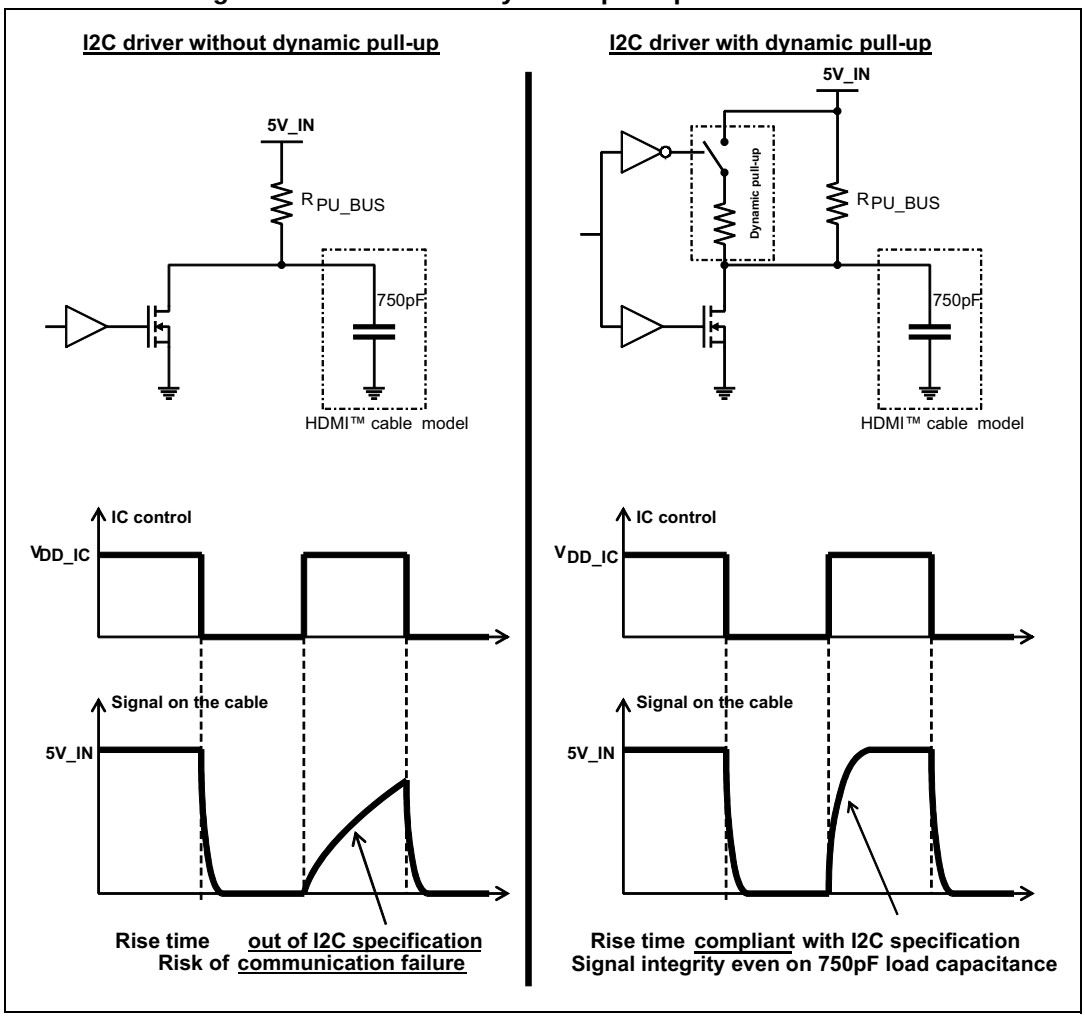
The *Figure 5* illustrates the electrical parameters of the DDC block specified in *Table 7*.

Figure 5. Simplified view of the electrical parameters of the DDC functional block



The HDMI standard specifies that the maximum capacitance of the cable can be as high as 700 pF. Knowing that the maximum capacitance of the source input can reach up to 50 pF, this means that the I2C driver must be able to drive a load capacitance up to 750pF. On the other hand, the I2C standard specifies that the maximum rise time of the signal must be lower than 1 µs in order to keep the signal integrity. Taking into account the maximum cable capacitance of 750 pF, it is not possible to guarantee a rise time lower than 1 µs in worst case. Therefore, a dynamic pull-up, synchronized with the I2C driver, has been integrated at the output of SDA and SCL lines. This signal booster accelerates for a short period the charging time of the equivalent cable capacitance, allowing to drive any HDMI cable. This dynamic pull-up is recommended by the I2C standard. The *Figure 6* illustrates the benefit of the dynamic pull-up integrated in the HDMI2C2-14HD device.

Figure 6. Benefit of the dynamic pull-up on the DDC bus



In order to activate the DDC bus, both following conditions must be respected: the V_{DD_5V} must be higher than the V_{DD_ON} threshold (see *Table 3*) and all inputs and outputs of the bidirectional level shifters (SCL, SDA, SCL_IC, SDA_IC) must be set to a high level at the same time.

The DDC outputs (SCL and SDA on cable side) integrate a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8kV contact).

2.3 HEAC link and HPD line protection

The HDMI2C2-14HD proposes a unique solution in order to manage and protect both the HEAC and the HPD links.

The HPD line is describe in the HDMI standards as a Hot Plug Defect function.This line is used by the source device in order to detect if a sink device is connected through an HDMI cable.

The HEAC link is described in the HDMI 1.4 standards as the HDMI ethernet and audio return channel. It corresponds physically to one differential wired pair made of the utility line and the HPD line. Two signals are transmitted through this link.

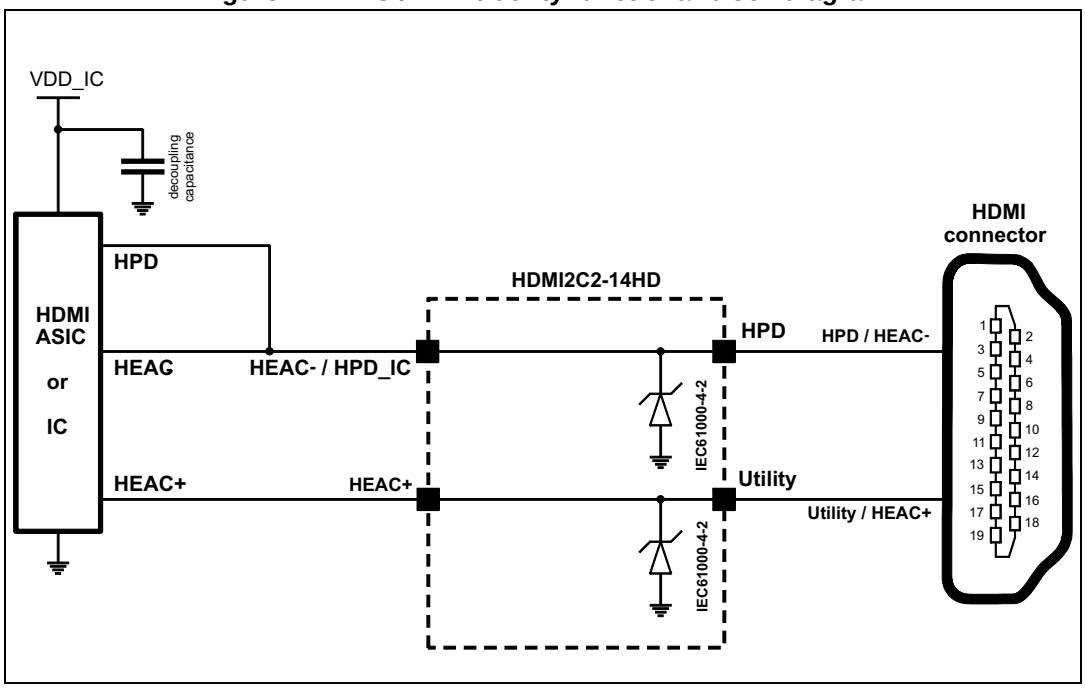
The first signal corresponds to the HDMI Ethernet Channel (HEC). The signal is transmitted in differential mode (bidirectional) through the HEAC link. It is specified by the 100Base TX IEEE 802.3 standard (Fast Ethernet 100Mbps over twisted pair). Therefore, the HEC integrates an Ethernet link into the video cable, enabling IP-based applications over the HDMI cable.

The second signal corresponds to the Audio Return Channel (ARC). The signal is transmitted in common mode (unidirectional, from sink to source) through the HEAC link. It is specified by the IEC 60958-1 standard. The ARC integrates an upstream audio capability, simplifying the cabling of the audiovisual equipments. It is no more necessary to use a coaxial cable from TV to audio amplifier.

The HDMI2C1-14HD helps the designer to implement this high added value HEAC function in the application, protecting the link against the ESD with no disturbance of the signal, thanks to the integrated matching circuitry on HEAC+ line. It provides 2 distinct outputs HEAC+ and HEAC- in order to ease as much as possible the PCB layout.

Both HPD and utility inputs (cable side) integrate a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8kV contact).

Figure 7. HEAC / HPD / utility functional block diagram



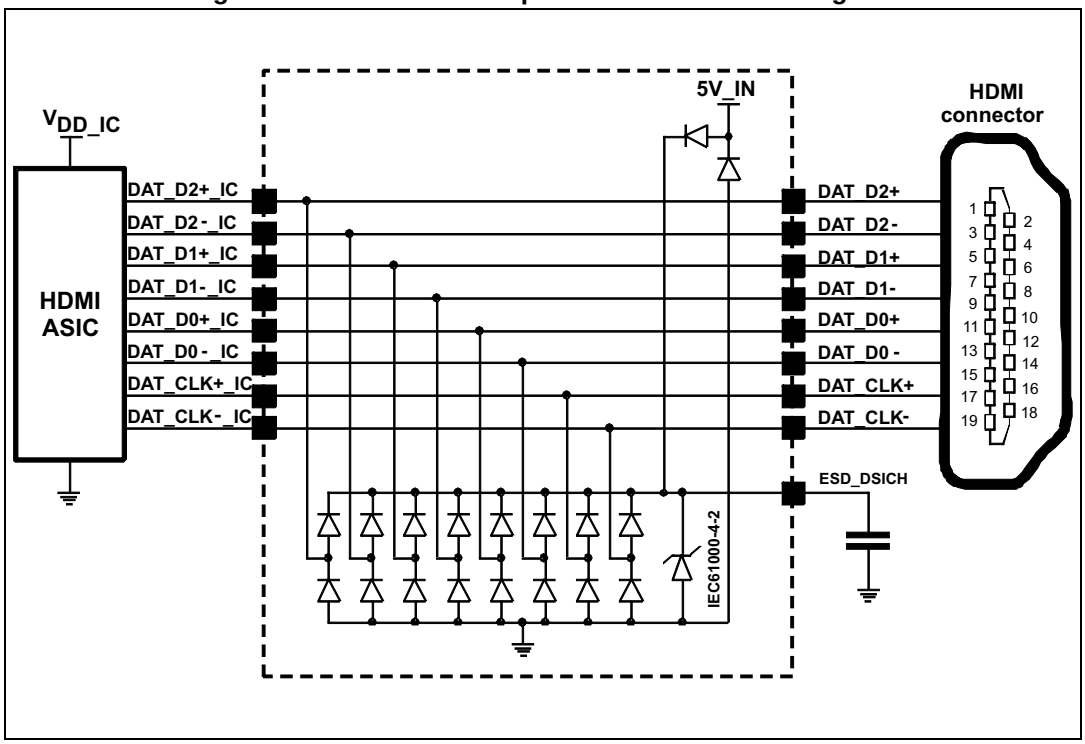
2.4 TMDS channels ESD protection

The TMDS (Transient Minimized Differential Signaling) channels are described by the HDMI 1.4 standard. A total of 4 unidirectional differential pairs are used to transmit the video data to the sink device. There are 3 channels dedicated to the video data, and 1 channel dedicated to the clock. The frequency of the TMDS clock is 1/10 of the video data frequency.

The HDMI2C2-14HD provides a simple PCB layout solution, directly compliant with HDMI connector type A. It protects the application against the ESD according the IEC61000-4-2 level 4 standard (+/-8 kV contact). The high bandwidth of this ESD protection allows to transmit HD video high speed data with no disturbance of the signal. The TDR is compliant with the HDMI specification.

A capacitor can be optionally connected to the ESD_DISCH pin in order to enhance the ESD protection performances.

Figure 8. TMDS lines ESD protection functional diagram



2.5 Application block diagrams

The *Figure 9* shows a typical application block diagram proposal implementing all the possible options. The TMDS channels are simply connected to the connector and to the HDMI ASIC. The diagram shows that the CEC driver can be totally independent from the HDMI ASIC. By this way, even if the +5 V power supply and/or if the HDMI ASIC is sleeping, the CEC bus is still active in low power mode. The designer has then all the tools to optimize the power consumption of the global application in stand-by mode, and has the possibility to implement a smart wake-up through the CEC bus enhancing the final user experience.

Figure 9. Modification of block diagram

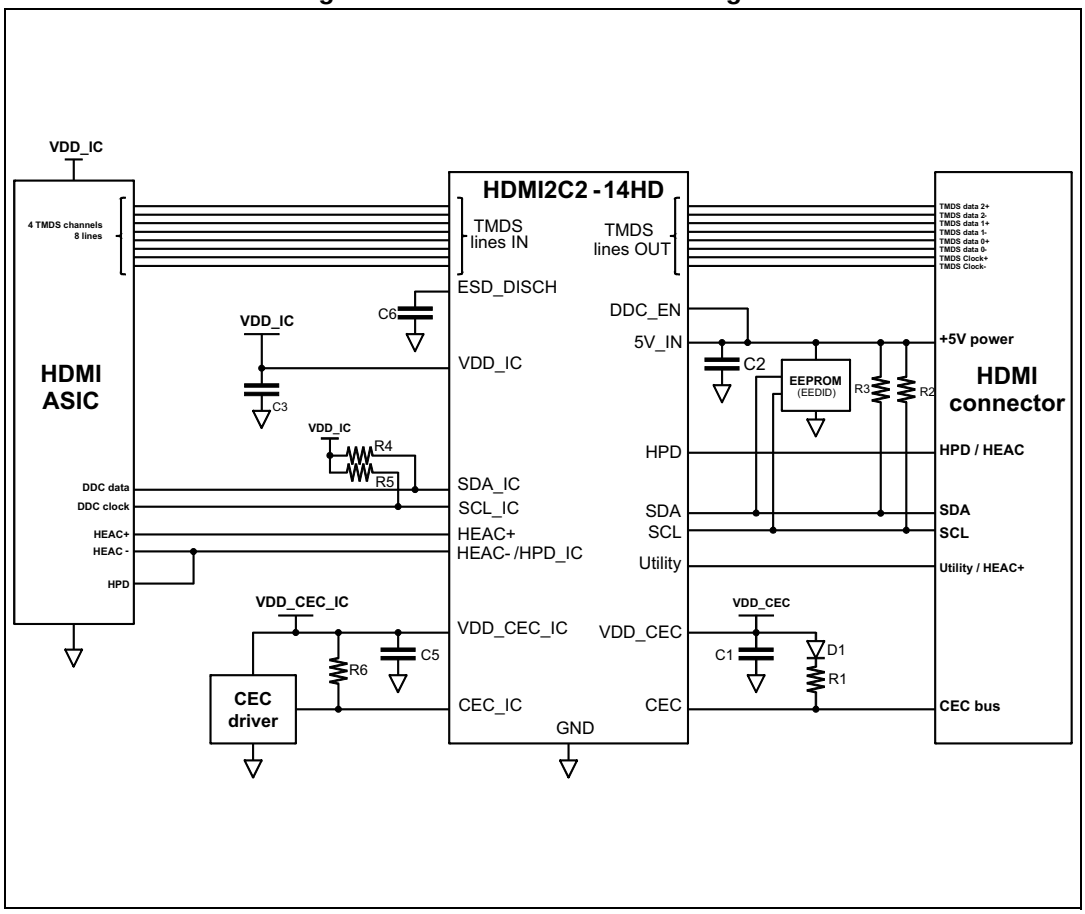


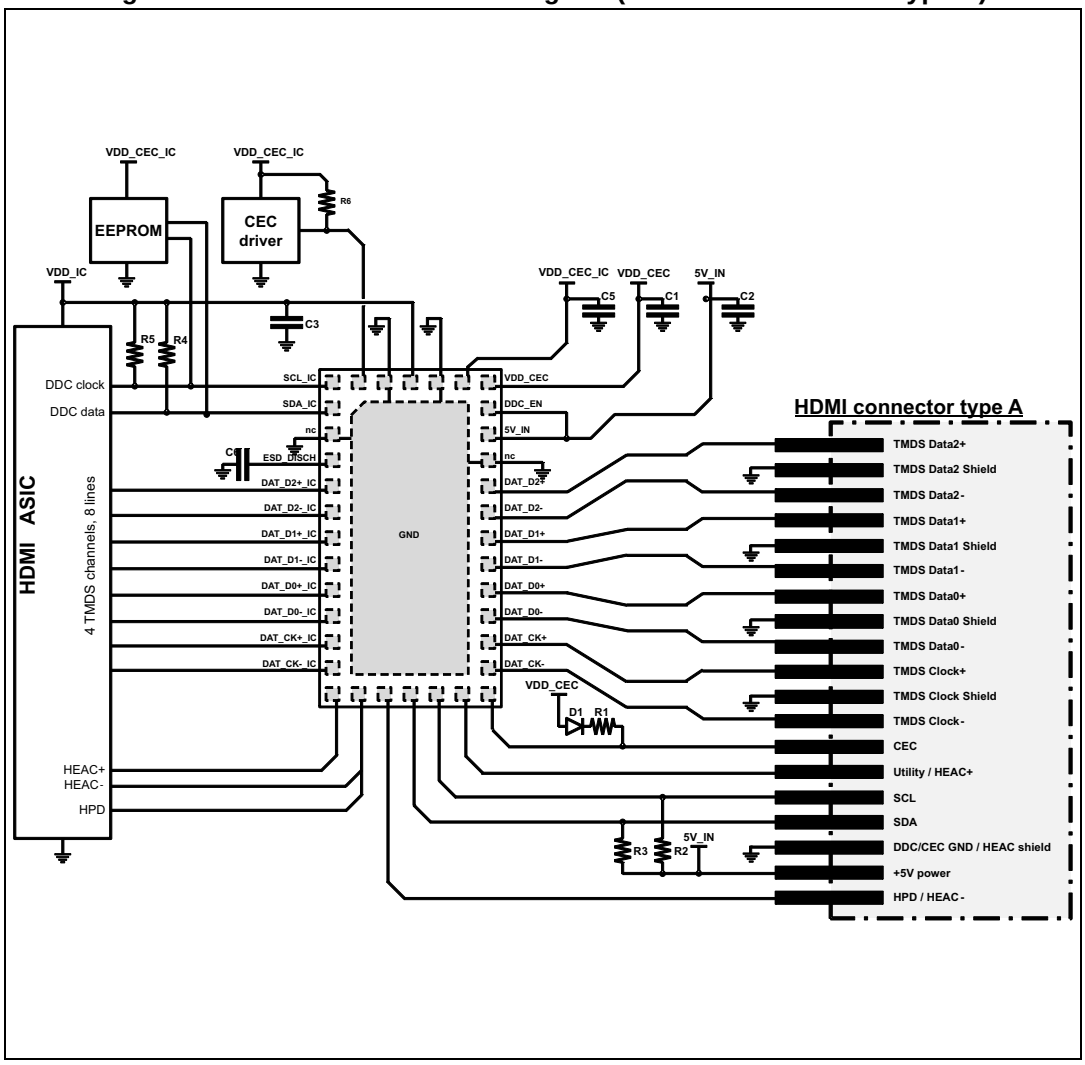
Table 1. Block diagrams references

Ref.	Typical values	Comment
R1	27 kΩ	Pull-up resistance on CEC bus, specified by the HDMI standard
R2, R3	47 kΩ	Pull-up resistances on DDC bus, specified by the HDMI standard
R4, R5	10 kΩ	Pull-up resistance on DDC bus, ASIC side, value selected to be compliant with I2C levels
R6	270 kΩ to 1 MΩ	Pull-up resistance on CEC line, ASIC side
D1	BAT54	Small schottky diode blocking backdrive current flowing toward the V_{DD_CEC} supply
C1, C2, C3 and C5	100 nF	Decoupling capacitance on power supplies
C6	1 µF	ESD protection enhancement capacitance (option)

Note: SCL_IC, SDA_IC, and CEC_IC have to be driven with an ASIC working with open drain outputs.

Note: even if not specified by HDMI standard, it is recommended to add pull-up resistance on SDA line (cable side) to avoid floating line.

Figure 10. Modification of block diagram (with HDMI connector type A)

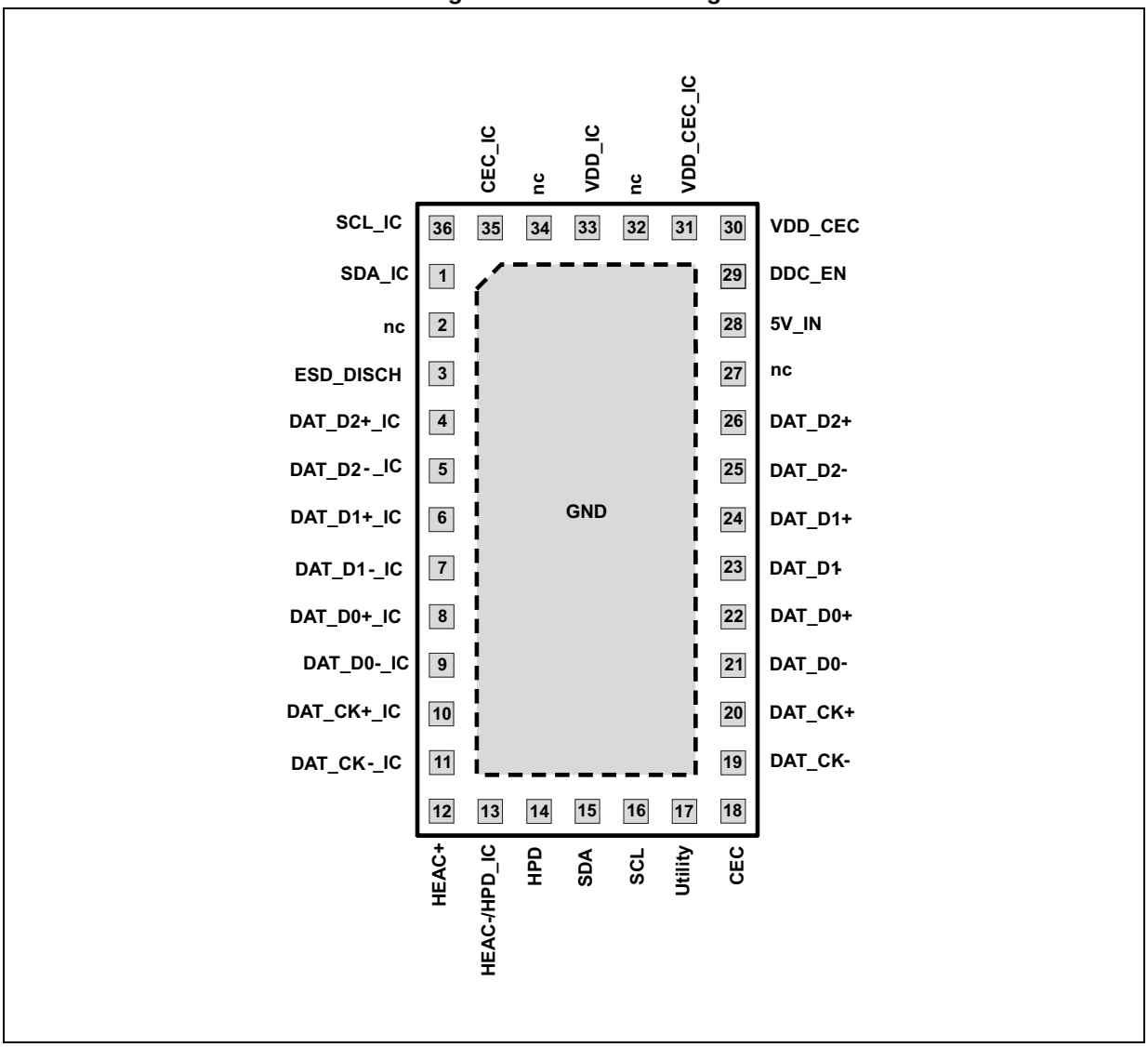


The *Figure 10* illustrates the fact that the HDMI2C2-14HD pin configuration eases and optimizes the PCB layout of the HDMI interface. The proposed pin-out sequence is directly compliant with HDMI connector type A.

Table 2. Pin description

Pin	Name	Description	Pin	Name	Description
1	SDA_IC	DDC input ASIC side	19	DAT_CK-	TMDS output Clock CK-
2	nc	not connected	20	DAT_CK+	TMDS output Clock CK+
3	ESD_DISCH	ESD protection enhancement capacitance	21	DAT_D0-	TMDS output Data D0-
4	DAT_D2+_IC	TMDS input Data D2+	22	DAT_D0+	TMDS output Data D0+
5	DAT_D2-_IC	TMDS input Data D2-	23	DAT_D1-	TMDS output Data D1-
6	DAT_D1+_IC	TMDS input Data D1+	24	DAT_D1+	TMDS output Data D1+
7	DAT_D1-_IC	TMDS input Data D1-	25	DAT_D2-	TMDS output Data D2-
8	DAT_D0+_IC	TMDS input Data D0+	26	DAT_D2+	TMDS output Data D2+
9	DAT_D0-_IC	TMDS input Data D0-	27	nc	not connected
10	DAT_CK+_IC	TMDS input Clock CK+	28	5V_IN	+5V power supply HDMI cable side
11	DAT_CK-_IC	TMDS input Clock CK-	29	5V_SYS_DETECT	SENSING OF +5V main power supply
12	HEAC+	HEAC+ output ASIC side	30	VDD_CEC	CEC supply HDMI cable side
13	HEAC-	HEAC- output ASIC side	31	VDD_CEC_IC	CEC driver power supply
14	HPD	HPD/HEAC- input HDMI cable side	32	nc	not connected
15	SDA	DDC output HDMI cable side	33	VDD_IC	HDMI ASIC power supply
16	SCL	DDC output HDMI cable side	34	nc	not connected
17	Utility	Utility/HEAC+ input HDMI cable side	35	CEC_IC	CEC input ASIC side
18	CEC	CEC output HDMI cable side	36	SCL_IC	DDC input ASIC side

Figure 11. Pin numbering



3 Electrical characteristics

Table 3. Absolute maximum ratings (limiting values)

Symbol	Parameter	Test conditions	Value	Unit
V_{pp_BUS}	ESD discharge on HDMI BUS side (pin 14 to 26, and pin 28), IEC 61000-4-2 level 4	Contact discharge	±8(1)	kV
V_{pp_IC}	ESD discharge (all pins), HBM JESD22-A114D level 2	Contact discharge	±2	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_{op}	Operating temperature range		-40 to +85	°C
T_L	Maximum lead temperature		260	°C
V_{5V_IN} V_{DD_IC} V_{DD_CEC} $V_{DD\_CEC\_IC}$	Supply voltages		6	V
Inputs	Logical input min/max voltage range		-0.3 to 6	V

1. With a 100 nF capacitor connected to the 5V_IN pin.

Table 4. Power supply characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD_CEC}	CEC supply voltage, bus side		2.97	3.3	3.63	V
$V_{DD\_CEC\_IC}$	CEC supply voltage, IC side		1.62		3.63	V
V_{DD_IC}	Low-voltage ASIC supply voltage		1.62		3.63	V
V_{5V_IN}	5 V cable supply voltage range		4.7	5.0	5.3	V
$V_{DD\_CEC\_ON}$	CEC power on reset		2.6	2.8	2.95	V
$I_{QS\_5V\_IN}$	Quiescent currents on $V_{DD\_5V\_IN}$, V_{DD_IC}, V_{DD_CEC}, $V_{DD\_CEC\_IC}$	V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, V_{DD_CEC} = 3.3 V $V_{DD\_CEC\_IC}$ = 1.8 V Idle-state on CEC and DDC links, HPD and 5V_OUT links open			500	µA
I_{QS_IC}					75	
I_{QS_CEC}					200	
$I_{QS\_CEC\_IC}$					40	
Rth	Junction to ambient thermal resistance	Copper heatsink as shown by *Figure 24*			75	°C/W
P_{TOTAL_SB}	Standby conditions	V_{DD_5V} = V_{DD_IC} = 0 V V_{DD_CEC} = 3.3 V $V_{DD\_CEC\_IC}$ = 3.3 V			0.8	mW

Table 5. CEC electrical characteristics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{Tup_CEC}	Upward input voltage threshold on bus side				1.6	V
V_{Tdown_CEC}	Downward input voltage threshold on bus side		0.8			V
V_{HYST_CEC}	Input hysteresis on bus side			0.4		V
T_{RISE_CEC}	Output rise-time (10% to 90%)	R_{UP} = 14.1 kΩ(2) ±5% $C_{CEC\ CABLE}$ = 9.7 nF			250	µs
T_{FALL_CEC}	Output fall-time (90% to 10%)				50	µs
I_{OFF_CEC}	Leakage current in powered-off state	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, V_{DD_CEC} = 3.3 V			1.8	µA
$V_{IL\_CEC\_IC}$	Input low level on IC side		0.5			$\%V_{DD\_IC}$
$V_{IH\_CEC\_IC}$	Input high level on IC side				70	$\%V_{DD\_IC}$
R_{ON_CEC}	On resistance across CEC and CEC_IC pins	CEC pin to 0 V		115	160	Ω
C_{IN_CEC}	Input capacitance on CEC link	V_{DD_5V} = 0 V V_{DD_CEC} = 0 V V_{DD_IC} = 0 V V_{BIAS} = 0 V, f = 1 MHz, V_{OSC} = 30 mV			40(3)	pF

1. T_{amb} = 25 °C, V_{DD_CEC} = 3.3 V, $V_{DD\_CEC\_IC}$ = 1.8 V, unless otherwise specified
2. Test conditions are compliant with worst case CEC specification:

- Correspond to two 27 kΩ +5% pull-up resistances in parallel (compliant with HDMI CTS)
- Max capacitance corresponding to 9 equipment chained on the CEC bus

3. Maximum capacitance allowed at connector output is 200 pF in HDMI 1.4 specification

Table 6. HPD, HEAC, and utility line electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
CIN_HPD CIN_UTILITY	Input capacitance	V_{DD_5V} = 0 V, V_{BIAS} = 0 V f = 100 kHz, V_{OSC} = 30 mV		9		pF
f_{CUT_HEAC}	Cut-off frequency of HEAC bus			500		MHz

1. T_{amb} = 25°C, V_{DD_5V} = 5 V, unless otherwise specified.

Table 7. DDC bus (SDA and SCL lines) electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_BUS}	Upward input voltage threshold on bus side				3.5	V
V_{Tdown_BUS}	Downward input voltage threshold on bus side		1.5			V
V_{HYST_BUS}	Input hysteresis on bus side		1.0		1.3	V
V_{OL_BUS}	Output low level	Current sunk by SDA and SCL pin is 3 mA			0.35	V
T_{RISE_BUS}	Output rise-time (30% to 70%)	C_{BUS} = 750 pF(2) R_{UP} = 2 KΩ //47 KΩ + 10%(3)			500	ns
T_{FALL_BUS}	Output fall-time (30% to 70%)				50	ns
V_{Tup_IC}	Upward input voltage threshold on IC side		55	60	65	$\%V_{DD\_IC}$
V_{Tdown_IC}	Downward input voltage thresholds IC side		35	40	45	$\%V_{DD\_IC}$
V_{OL_IC}	Output low level on IC side	Current sunk by SDA_IC or SCL_IC pins is 500 µA			20	mV
C_{IN_DDC}	Input capacitance on DDC link	V_{DD_5V} = 0 V V_{DD_IC} = 0 V V_{DD_CEC} = 0 V V_{BIAS} = 0 V, f = 1 MHz V_{OSC} = 30 mV		9	17(4)	pF
V_{EN_DCC}(5)	DCC enabling		4.1			V

1. T_{amb} = 25 °C, V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, unless otherwise specified
2. Maximum load capacitance allowed on I2C entire link (cable + connector) is 750 pF in HDMI 1.4 specification.
3. Two pull-up resistors in parallel (sink 47 kΩ + source 2 kΩ).
4. Maximum capacitance allowed at connector output is 50 pF in HDMI 1.4 specification
5. In order to activate the DCC lines, the level on DCC_EN pin has to reach the V_{EN_DCC} min value. The inputs and ouputs of the bidirectional level shifters must be set to a high level after the power-on, and the HPD line has to be activated one time.

Table 8. TMDS links electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
f_{CUT_TMDS}	Bandwidth at -3 dB	Single ended mode		4.7(2)		GHz
		Differential mode		6.5		
V_{BR}	Breakdown voltage		6			V
I_{RM}	Leakage current	V_{RM} = 3.3 V			100	nA
$C_{I/O-GND}$	Capacitance input/output to ground	$V_{I/O}$ =0 V, f = 1 MHz, V_{OSC} = 30 mV			1.5	pF
$\Delta C_{I/O-GND}$	Capacitance variation	$V_{I/O}$ = 0 V, f = 1 MHz, V_{OSC} = 30 mV		50		pF
Z_{DIFF}	Differential impedance	tr = 200ps (10%-90%) $Z0_{DIFF}$=100 Ω	85	100	115	Ω

1. T_{amb} =25°C, V_{DD_5V} = 5V, unless otherwise specified
2. The bandwidth is large enough to operate up to 340 MHz as HDMI clock frequency, corresponding to 10.2 Gbps total data rate, 3.4 Gbps on each lane

Figure 12. TMDS line S_{21} frequency curve

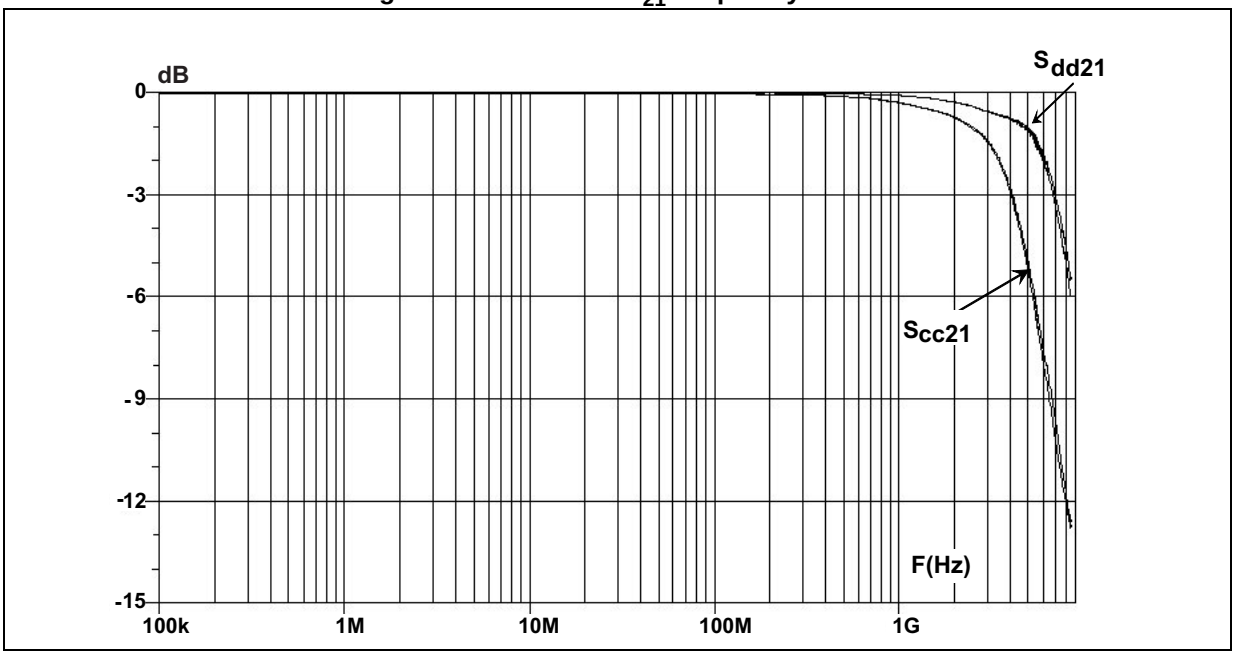


Figure 13. TMDS line differential far end crosstalk curve

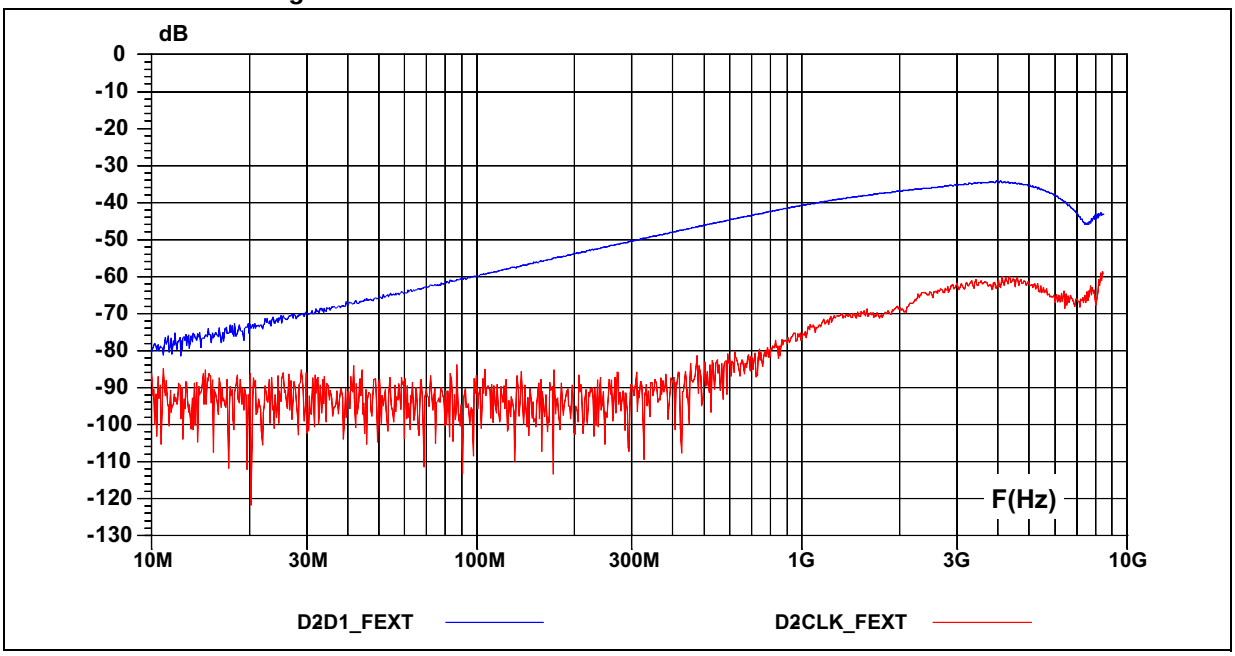


Figure 14. TMDS line: remaining voltage when positive 8 kV ESD surge applied

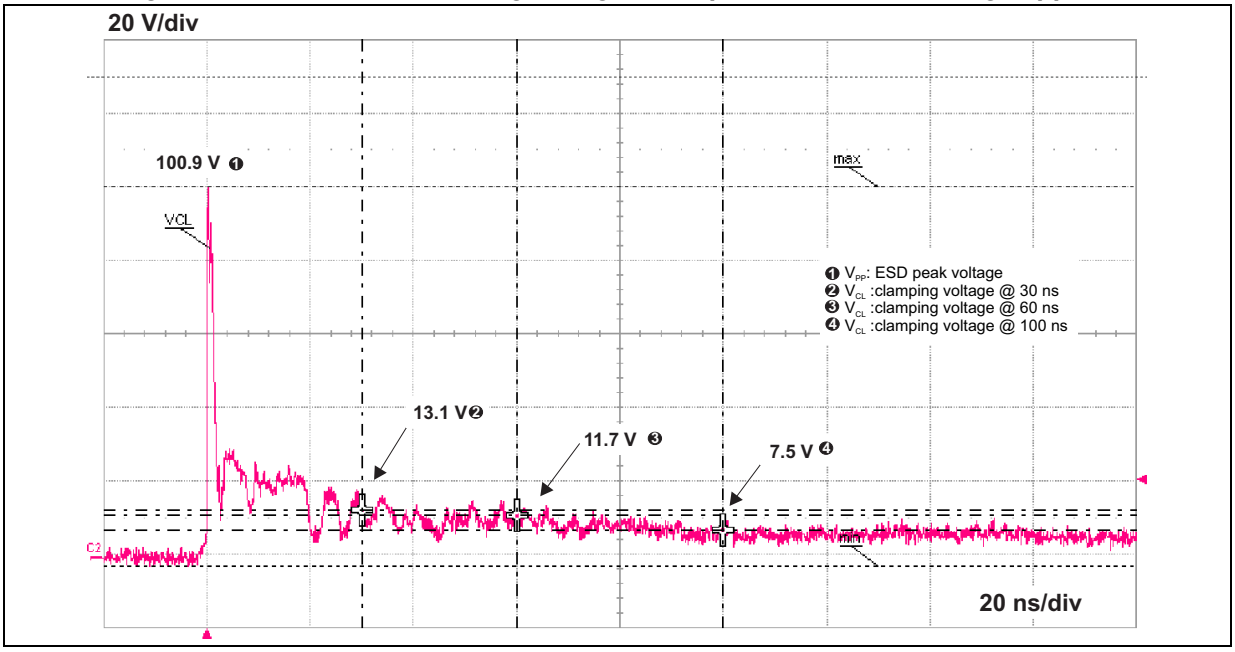


Figure 15. TMDS line: remaining voltage when negative 8 kV ESD surge applied

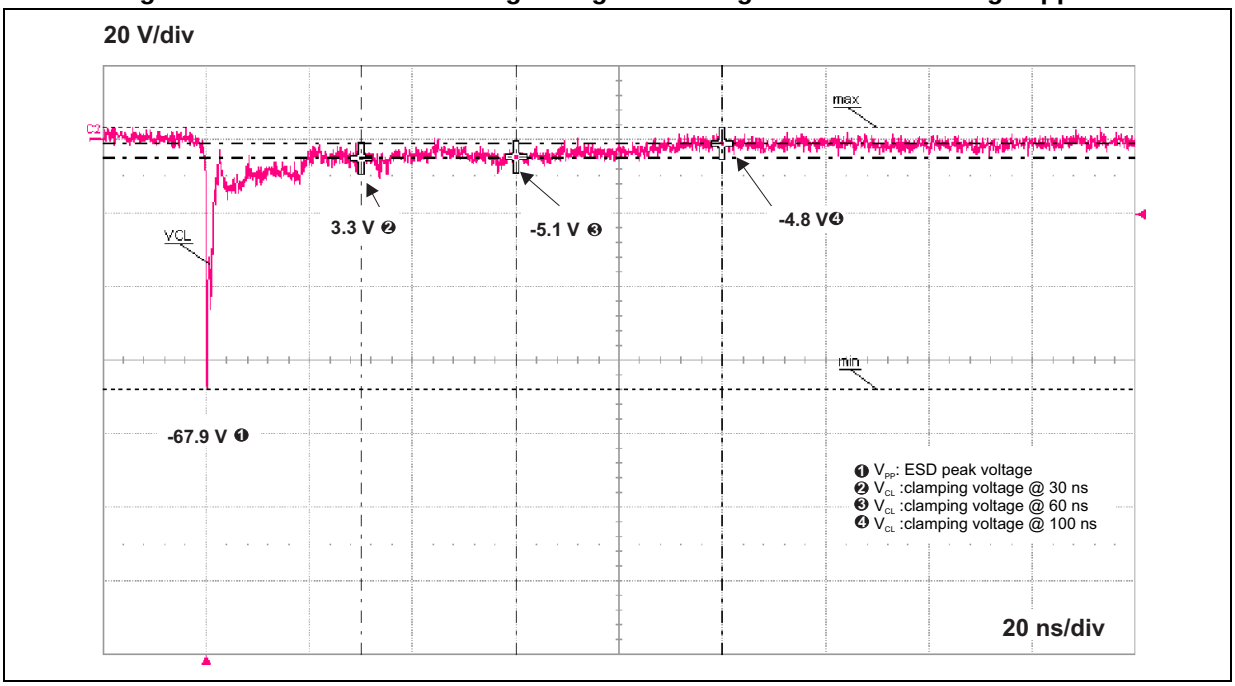


Figure 16. Eye diagram of TMDS line: D0, D1, D2 and CLK lanes (1.485 Gbps)

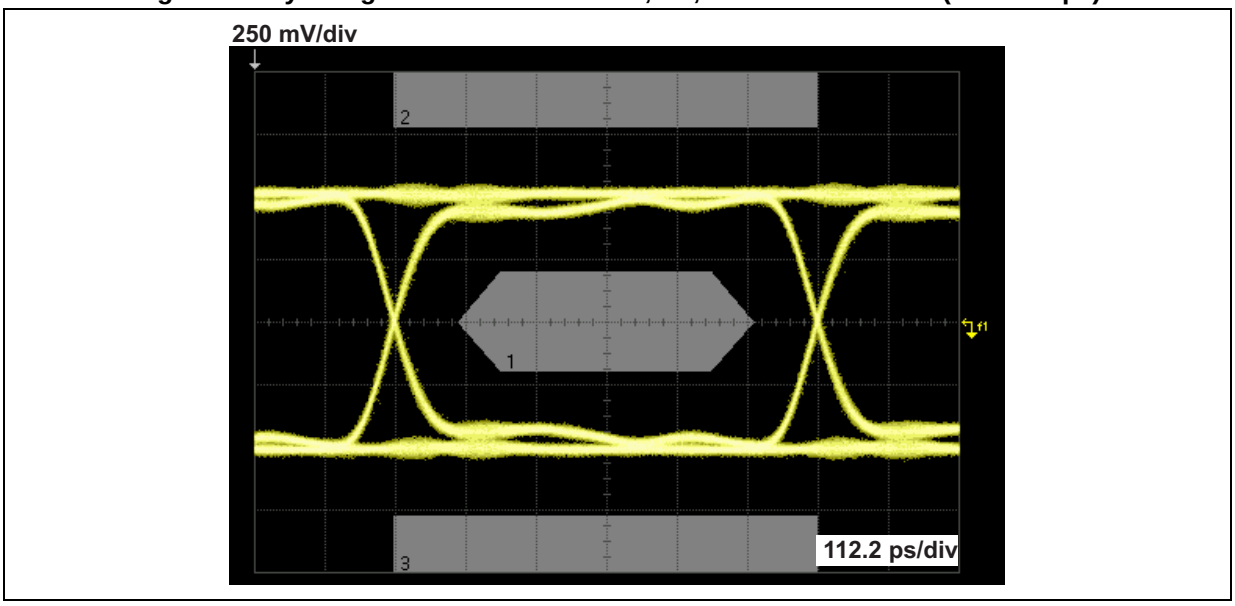


Figure 17. Eye diagram of TMDS line: D0, D1, D2 and CLK lanes (3.350 Gbps)

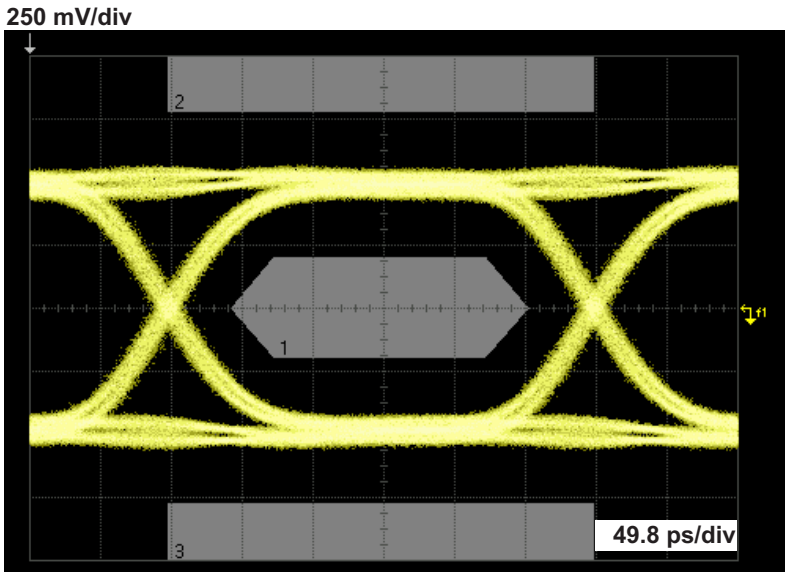


Figure 18. TDR of TMDS lines: D0, D1, D2, CLK lanes

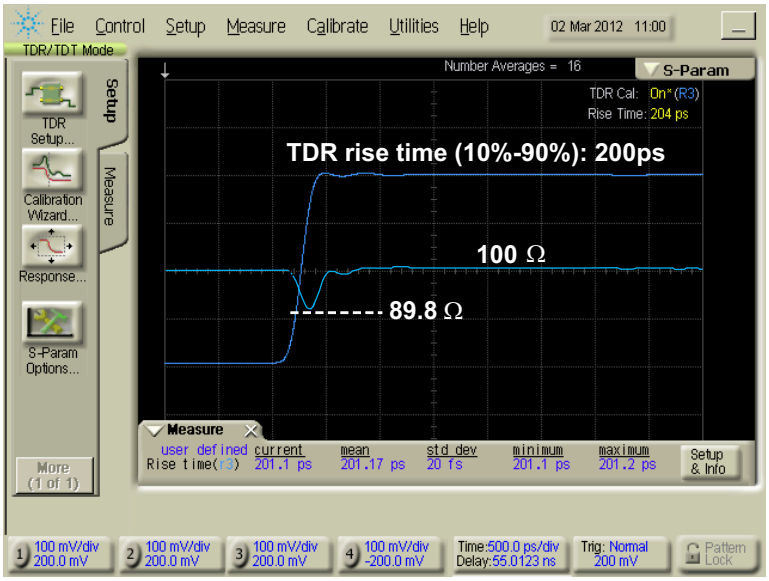


Figure 19. CEC typical waveforms (from source to sink communication)

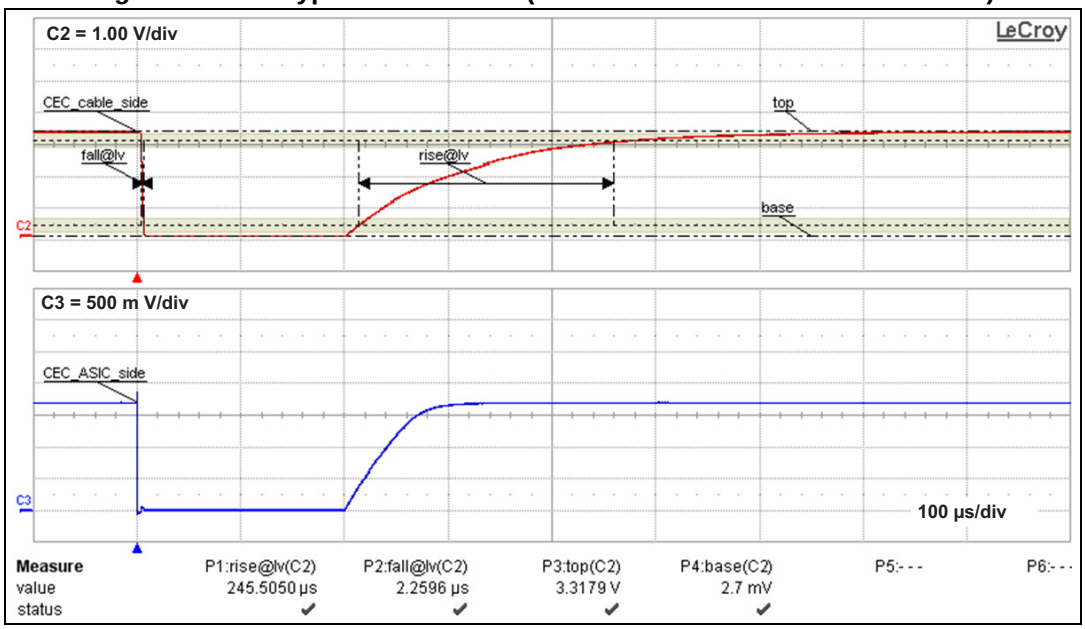


Figure 20. CEC typical waveforms (from sink to source communication)

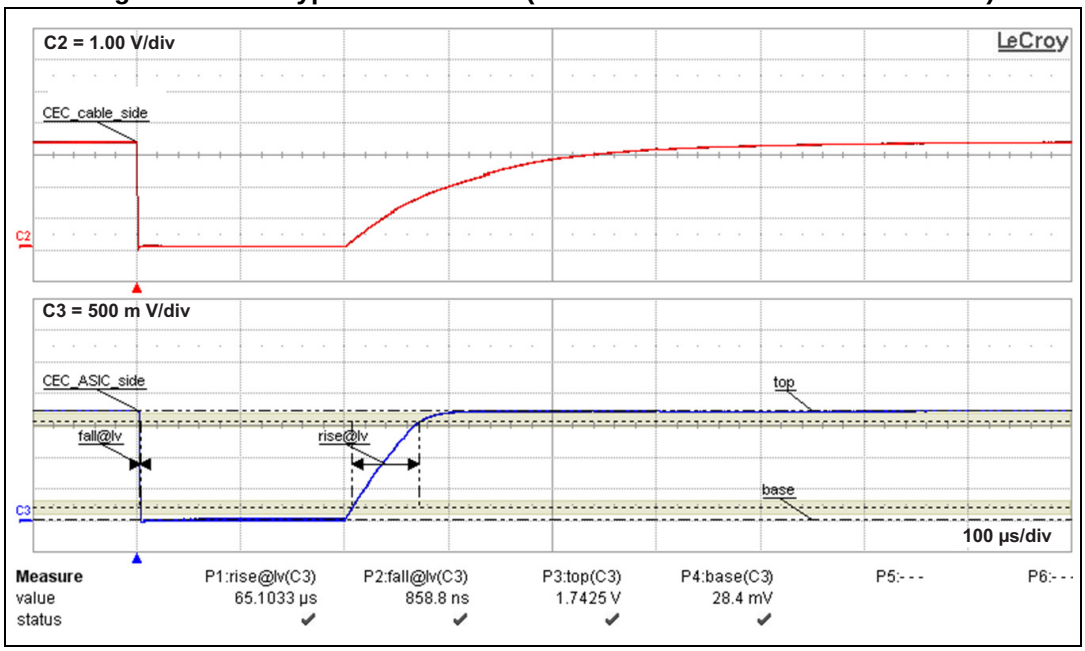


Figure 21. DDC typical waveforms (from sink to source communication)

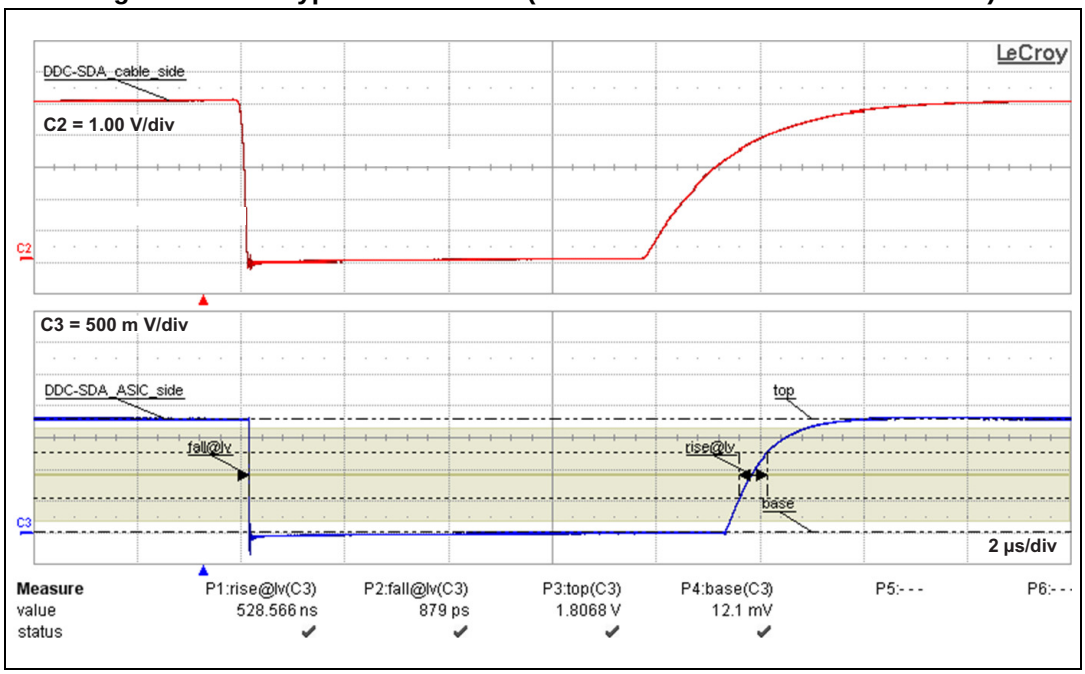
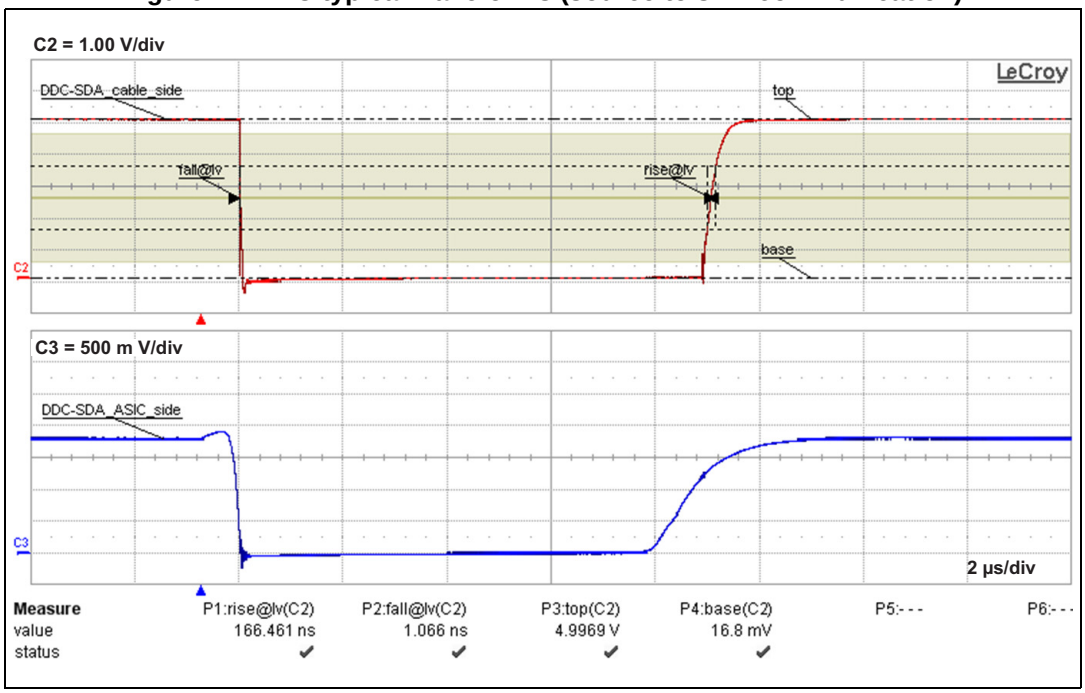


Figure 22. DDC typical waveforms (source to sink communication)



4 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

Figure 23. QFN dimension definitions

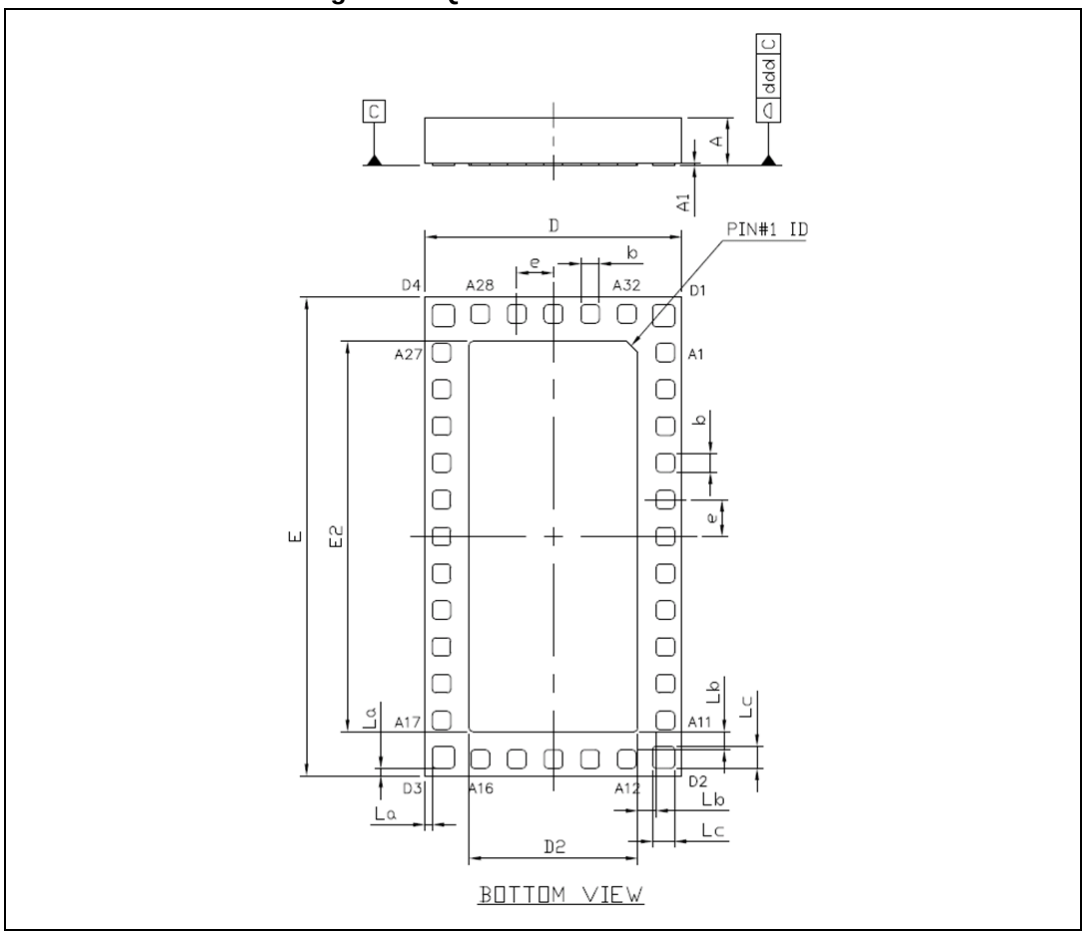


Table 9. QFN dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	0.00		0.05	0.000		0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D	3.40	3.50	3.60	0.134	0.137	0.141
D2	2.25	2.30	2.35	0.088	0.090	0.092
E	6.40	6.50	6.60	0.251	0.255	0.259
E2	5.25	5.30	5.35	0.206	0.208	0.210
e		0.50			0.020	
La	0.00	0.10	0.20	0.00	0.004	0.008
Lb	0.15	0.25	0.30	0.006	0.01	0.012
Lc	0.20	0.30	0.40	0.008	0.012	0.016
ddd		0.09			0.003	

Figure 24. QFN footprint recommendation (dimensions in mm)

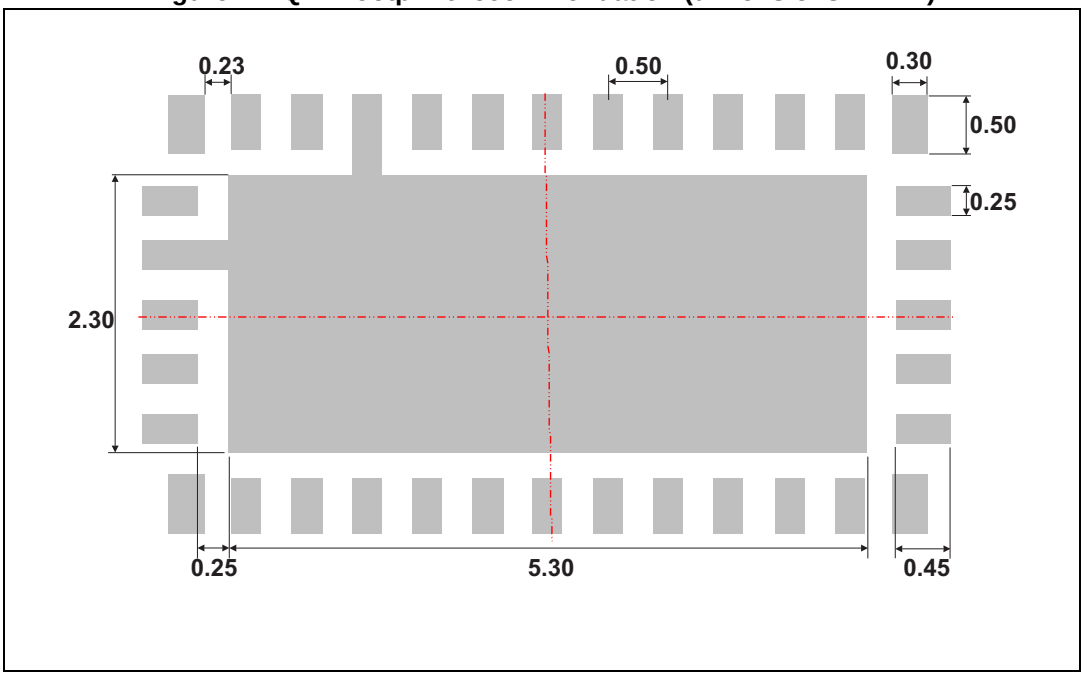
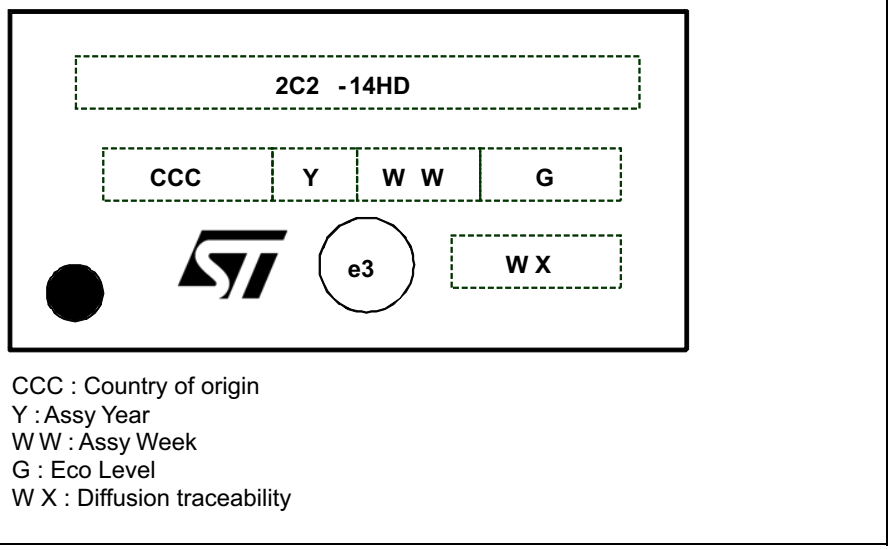
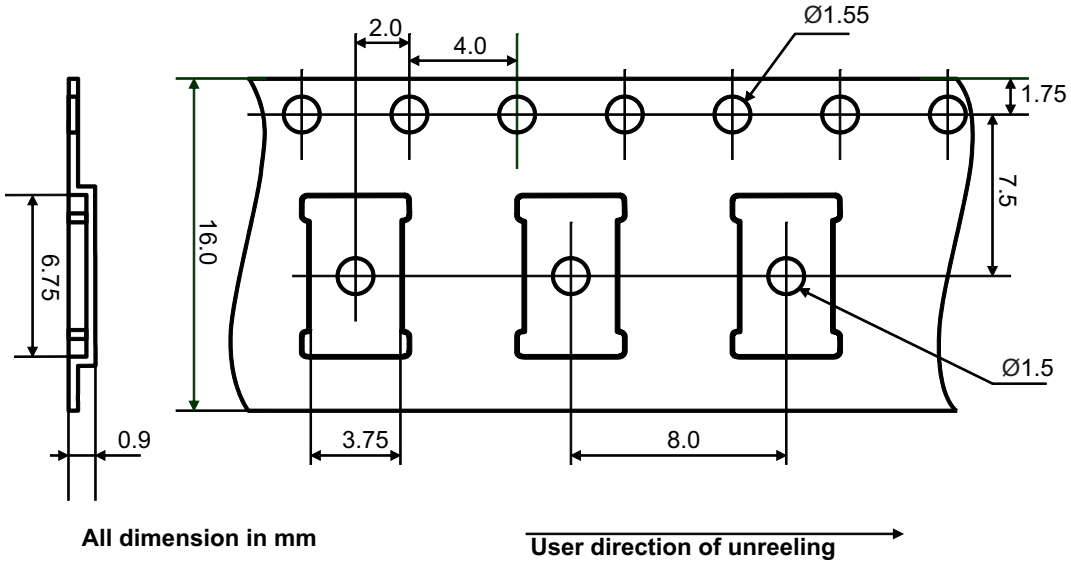


Figure 25. Marking specification



CCC : Country of origin
Y : Assy Year
W W : Assy Week
G : Eco Level
W X : Diffusion traceability

Figure 26. Tape and reel specification

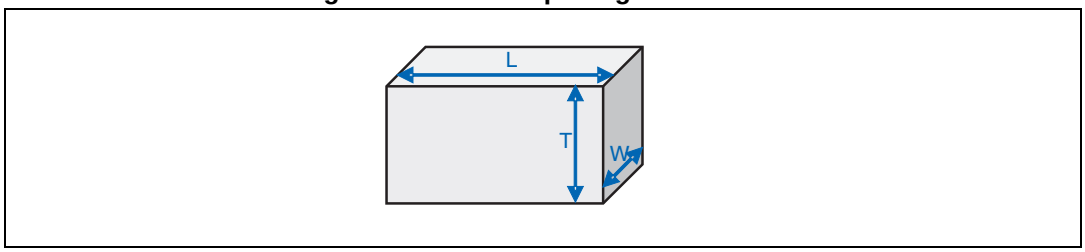


5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 27. Stencil opening dimensions



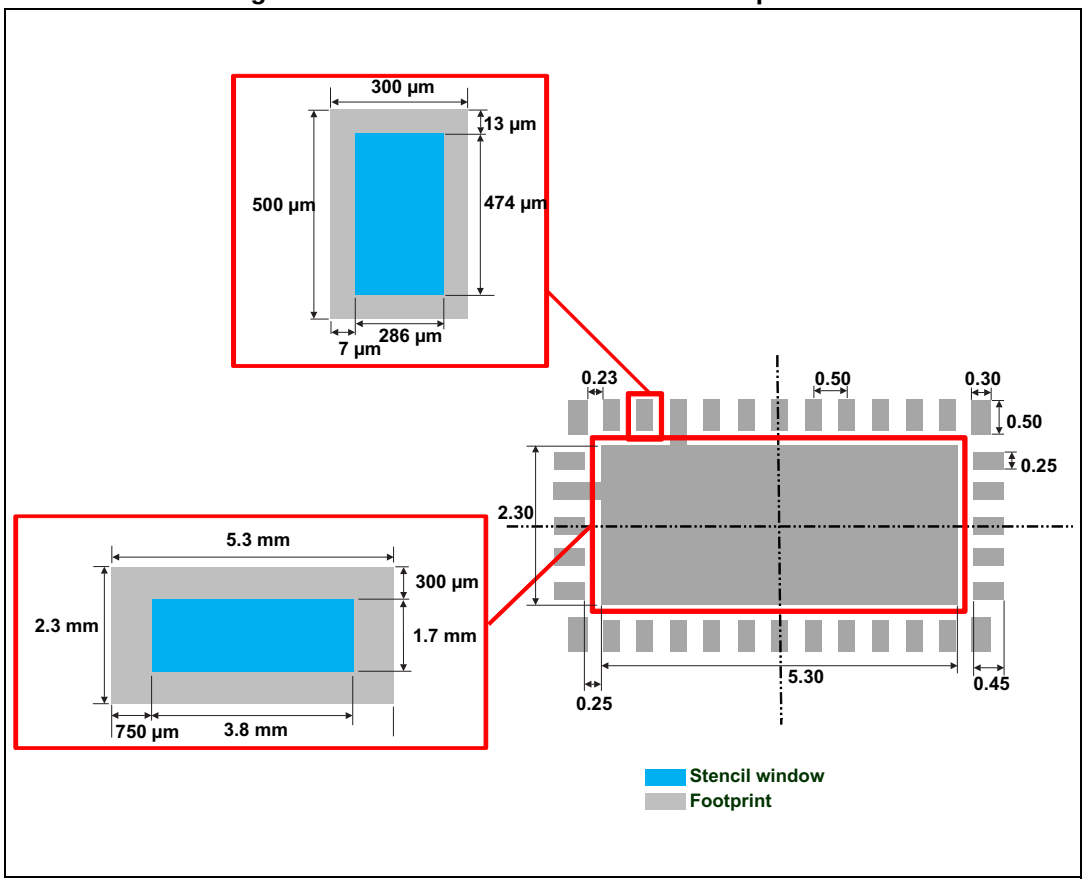
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 28. Recommended stencil window position



5.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

5.3 Placement

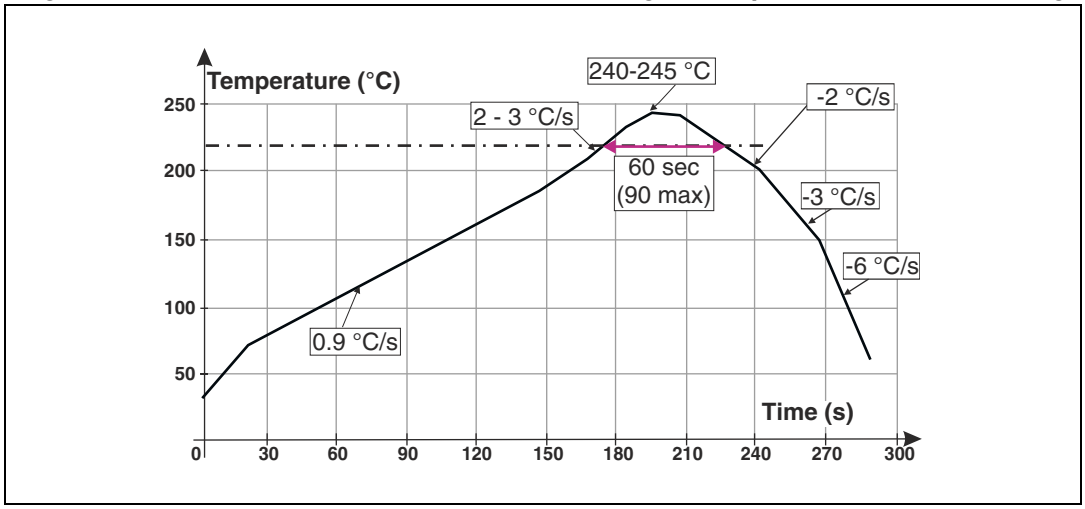
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, closed vias are recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. Symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 29. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Figure 30. Ordering information scheme

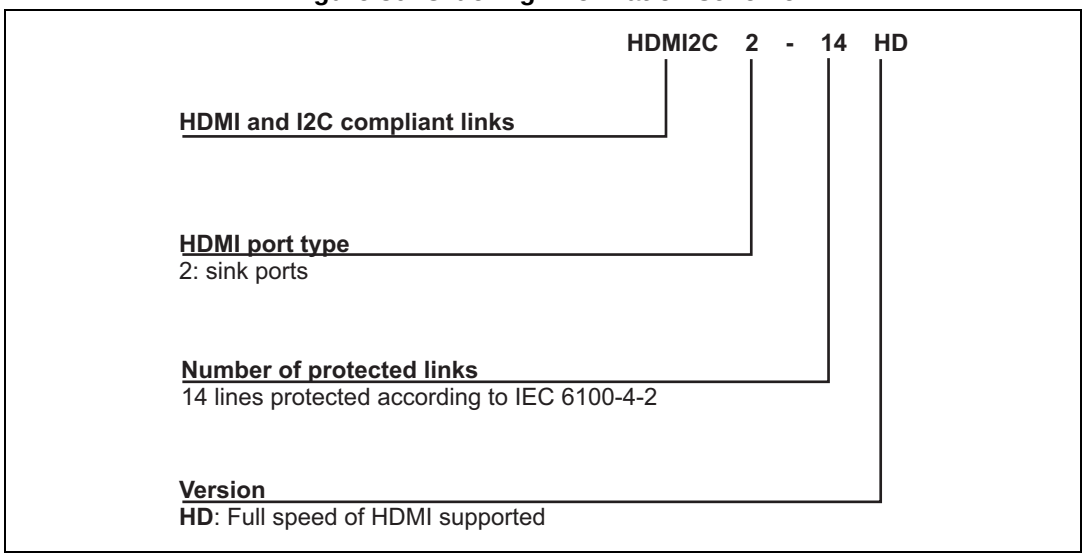


Table 10. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HDMI2C2-14HD	2C2-14HD	QFN	51.6 mg	4.000	Tape and reel

7 Revision history

Table 11. Document revision history

Date	Revision	Changes
04-Aug-2014	1	Initial release