

BUK964R2-60E

N-channel TrenchMOS logic level FET

13 July 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with VGS(th) rating of greater than 0.5V at 175 °C

1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ }^{\circ}\text{C}; T_j \leq 175 \text{ }^{\circ}\text{C}$		-	-	60	V
I_D	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ }^{\circ}\text{C}$; Fig. 1	[1]	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^{\circ}\text{C}$; Fig. 2		-	-	263	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$; Fig. 11		-	3.46	4.2	$\text{m}\Omega$
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 48 \text{ V}$; Fig. 13 ; Fig. 14		-	27	-	nC

[1] Continuous current is limited by package.

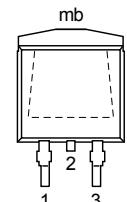
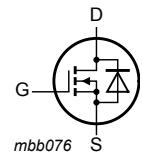


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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain	 D2PAK (SOT404)	

3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description		
BUK964R2-60E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)		SOT404

4. Limiting values

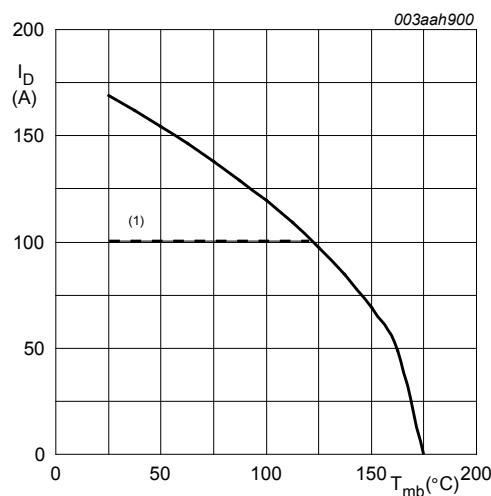
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$		-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage	$T_j = 25^\circ\text{C}$		-10	10	V
		$T_j = 25^\circ\text{C}$; lifetime = 100 hours		-15	15	V
I_D	drain current	$T_{mb} = 25^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[1]	-	100	A
		$T_{mb} = 100^\circ\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 1	[1]	-	100	A
I_{DM}	peak drain current	$T_{mb} = 25^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4		-	675	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; Fig. 2		-	263	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25^\circ\text{C}$	[1]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$		-	675	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100 \text{ A}$; $V_{sup} \leq 60 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 5 \text{ V}$; $T_{j(init)} = 25 \text{ }^\circ\text{C}$; unclamped; Fig. 3	[2][3]	-	372	mJ

[1] Continuous current is limited by package.
 [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
 [3] Refer to application note AN10273 for further information.



(1) Capped at 100A due to package

Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5 \text{ V}$$

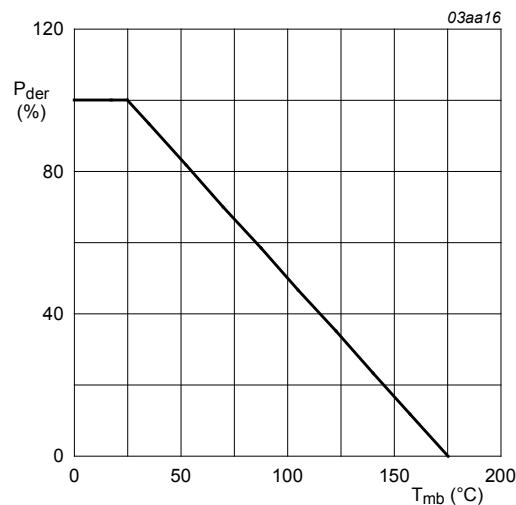


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \text{ \%}$$

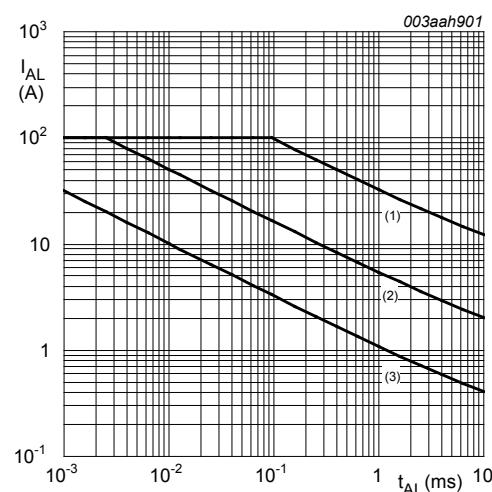


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(init)} = 25 \text{ }^\circ\text{C}$; (2) $T_{j(init)} = 150 \text{ }^\circ\text{C}$; (3) Repetitive Avalanche

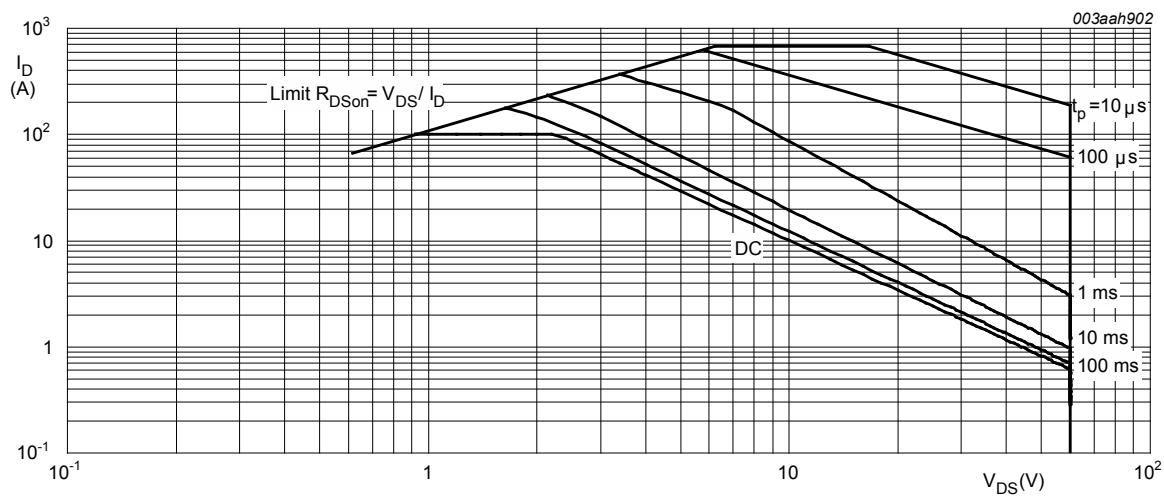


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.57	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

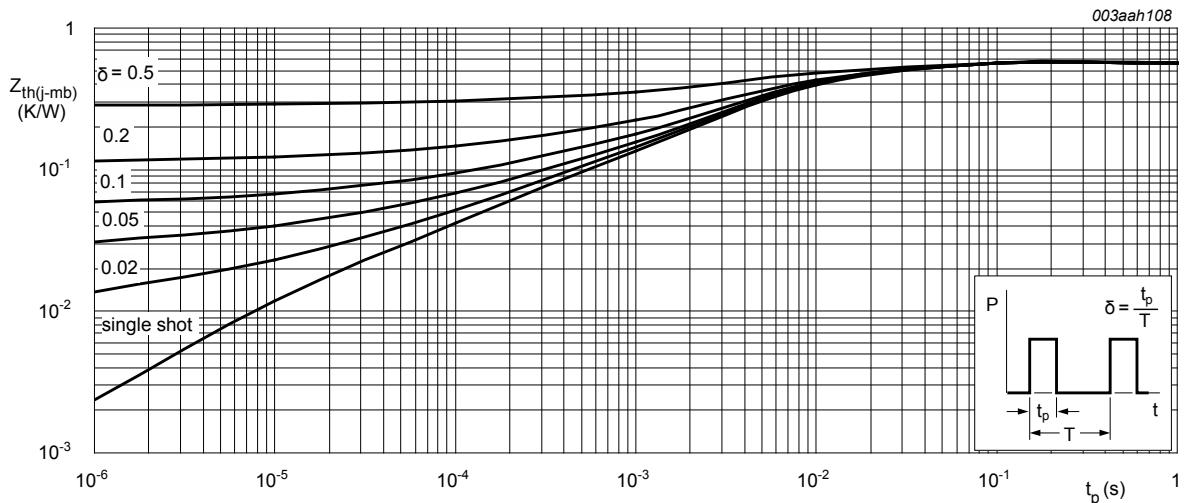


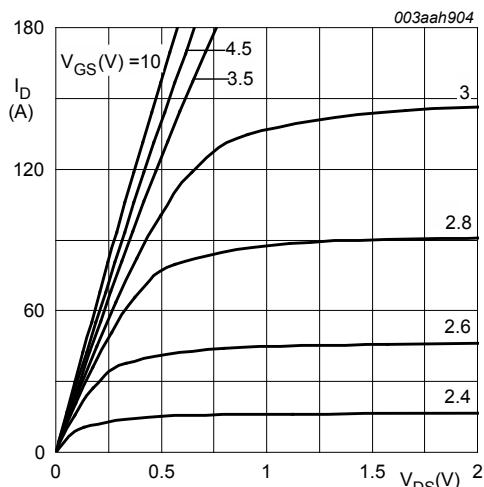
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		60	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$		54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$ Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55^\circ C$ Fig. 9		-	-	2.45	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175^\circ C$ Fig. 9		0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	0.06	1	μA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175^\circ C$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	2	100	nA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 25 A; T_j = 25^\circ C$ Fig. 11		-	3.46	4.2	$m\Omega$
		$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C$ Fig. 11		-	3.17	3.9	$m\Omega$
		$V_{GS} = 5 V; I_D = 25 A; T_j = 175^\circ C$ Fig. 12 ; Fig. 11		-	-	9.2	$m\Omega$
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 48 V; V_{GS} = 5 V$ Fig. 13 ; Fig. 14		-	72	-	nC
Q_{GS}	gate-source charge			-	20	-	nC
Q_{GD}	gate-drain charge			-	27	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz$ $T_j = 25^\circ C$; Fig. 15		-	8533	11380	pF
C_{oss}	output capacitance			-	703	843	pF
C_{rss}	reverse transfer capacitance			-	357	489	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 45 V; R_L = 1.8 \Omega; V_{GS} = 5 V$ $R_{G(ext)} = 5 \Omega$		-	47	-	ns
t_r	rise time			-	97	-	ns
$t_{d(off)}$	turn-off delay time			-	84	-	ns
t_f	fall time			-	73	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 16		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$		-	40	-	ns
Q_r	recovered charge	$V_{DS} = 25 \text{ V}$		-	59	-	nC



$T_j = 25 \text{ }^\circ\text{C}$; $t_p = 300 \mu\text{s}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

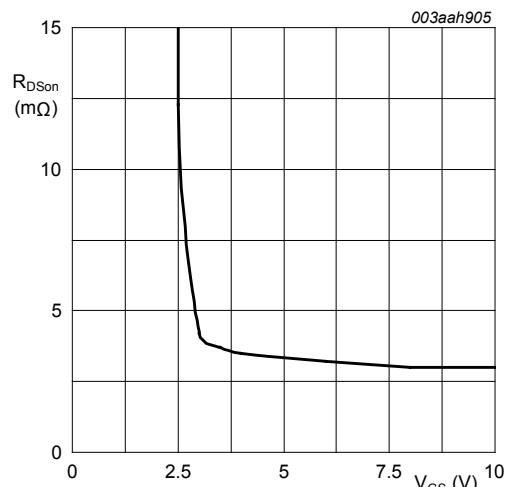


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25 \text{ }^\circ\text{C}$; $I_D = 25 \text{ A}$

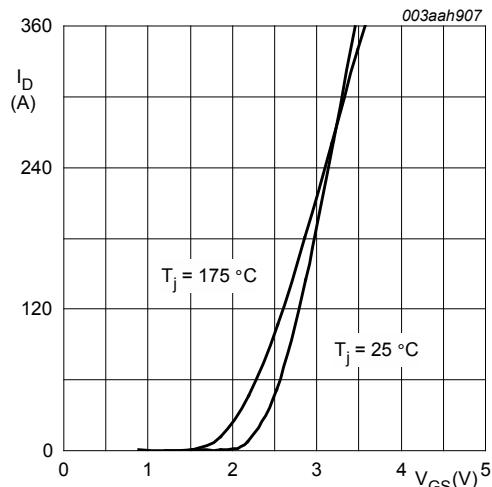


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10 \text{ V}$

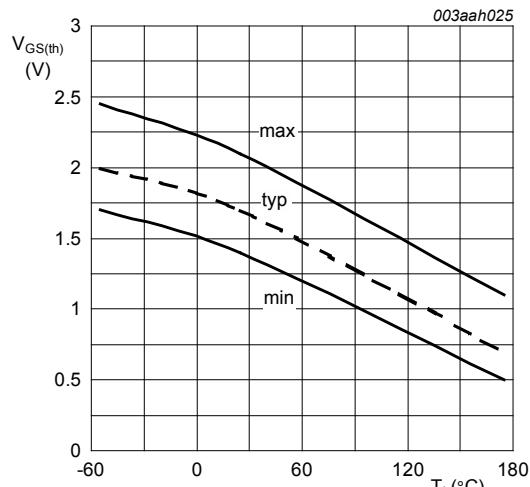


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

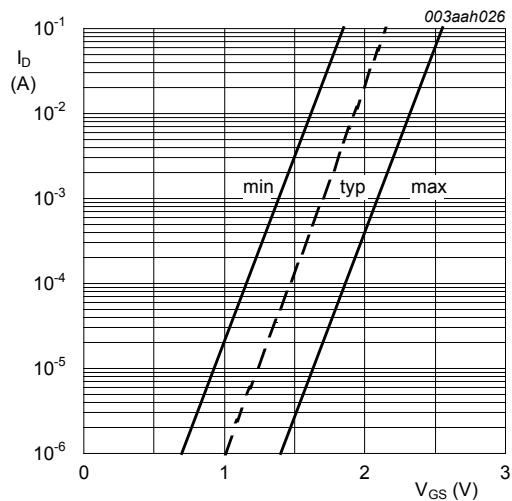
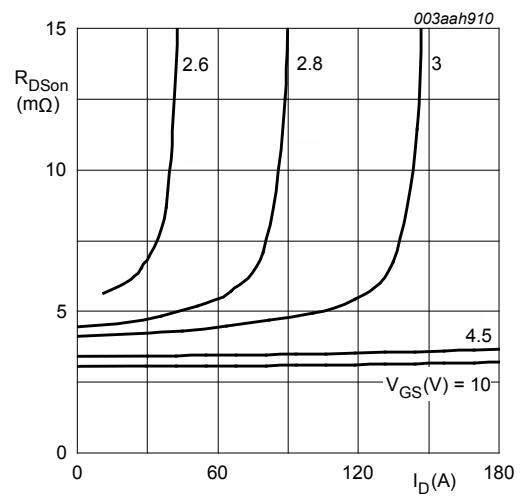


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}$; $V_{DS} = 5\text{V}$



$T_j = 25^\circ\text{C}$; $t_p = 300\ \mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

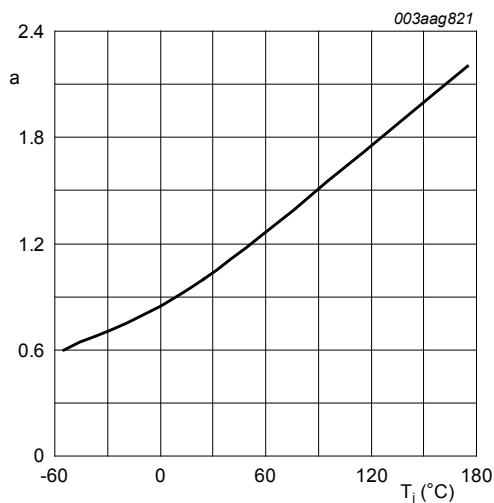


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

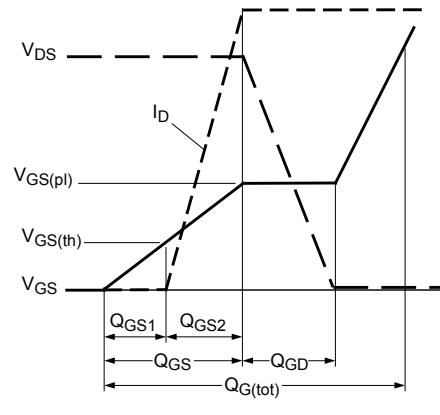


Fig. 13. Gate charge waveform definitions

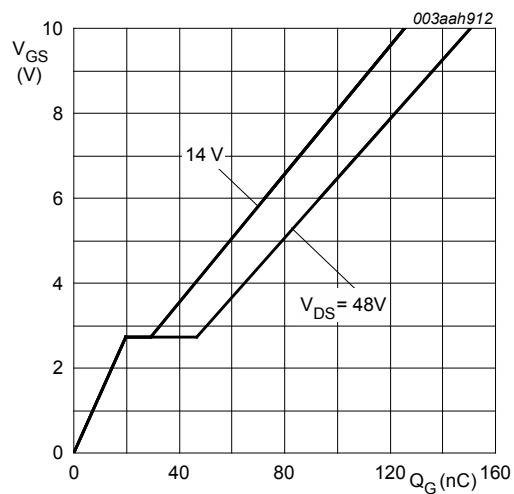


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C$; $I_D = 25A$

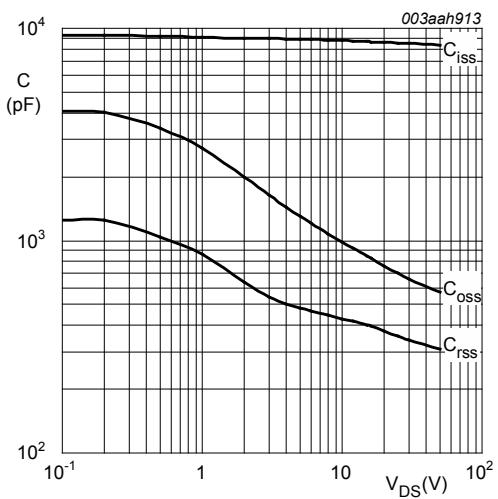


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V$; $f = 1MHz$

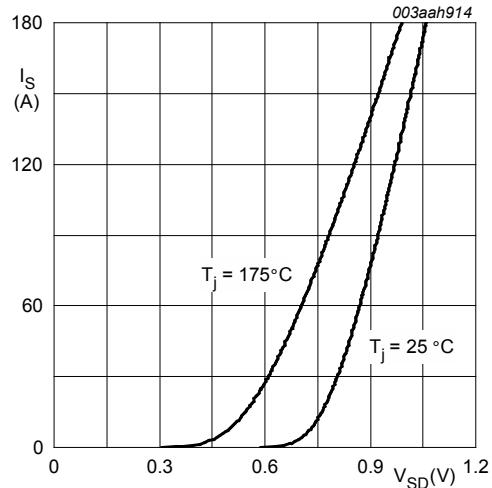


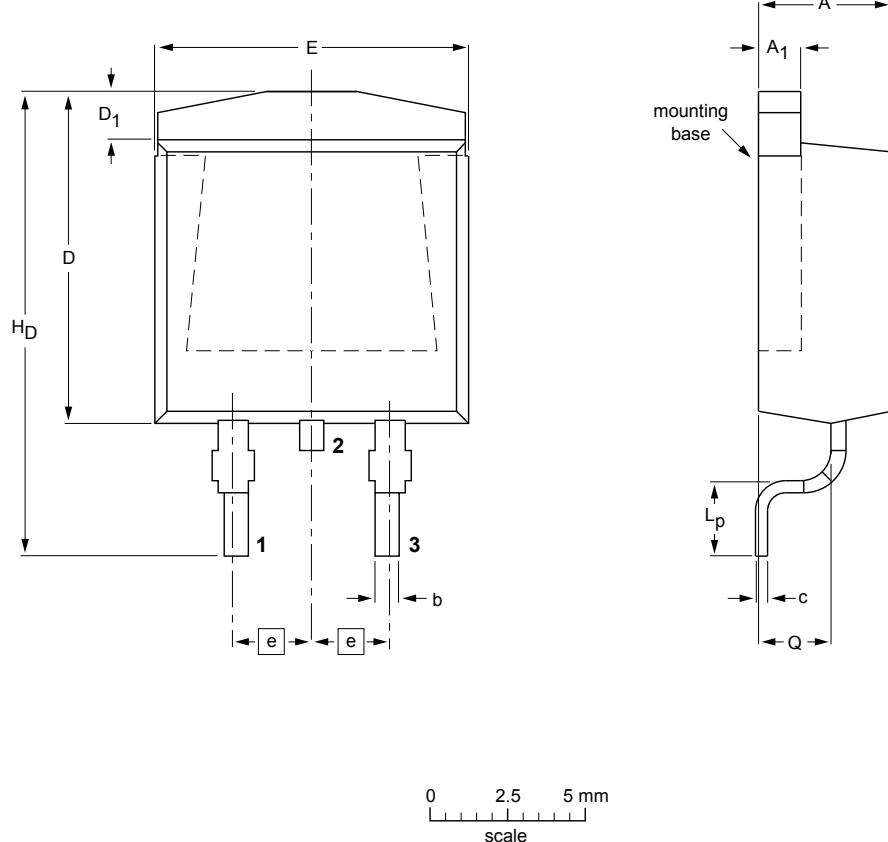
Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig. 17. D2PAK (SOT404)

8. Legal information

8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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