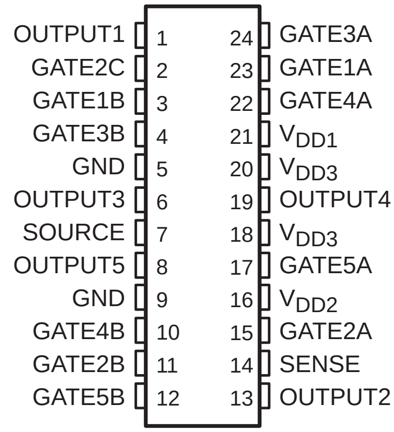
- **Low $r_{DS(on)}$:**
  0.25 Ω Typ (Full H-Bridge)
  0.15 Ω Typ (Triple Half H-Bridge)
- **Pulsed Current:**
  6 A Per Channel (Full H-Bridge)
  8 A Per Channel (Triple Half H-Bridge)
- **Matched Sense Transistor for Class A-B Linear Operation**
- **Fast Commutation Speed**

DW PACKAGE
(TOP VIEW)

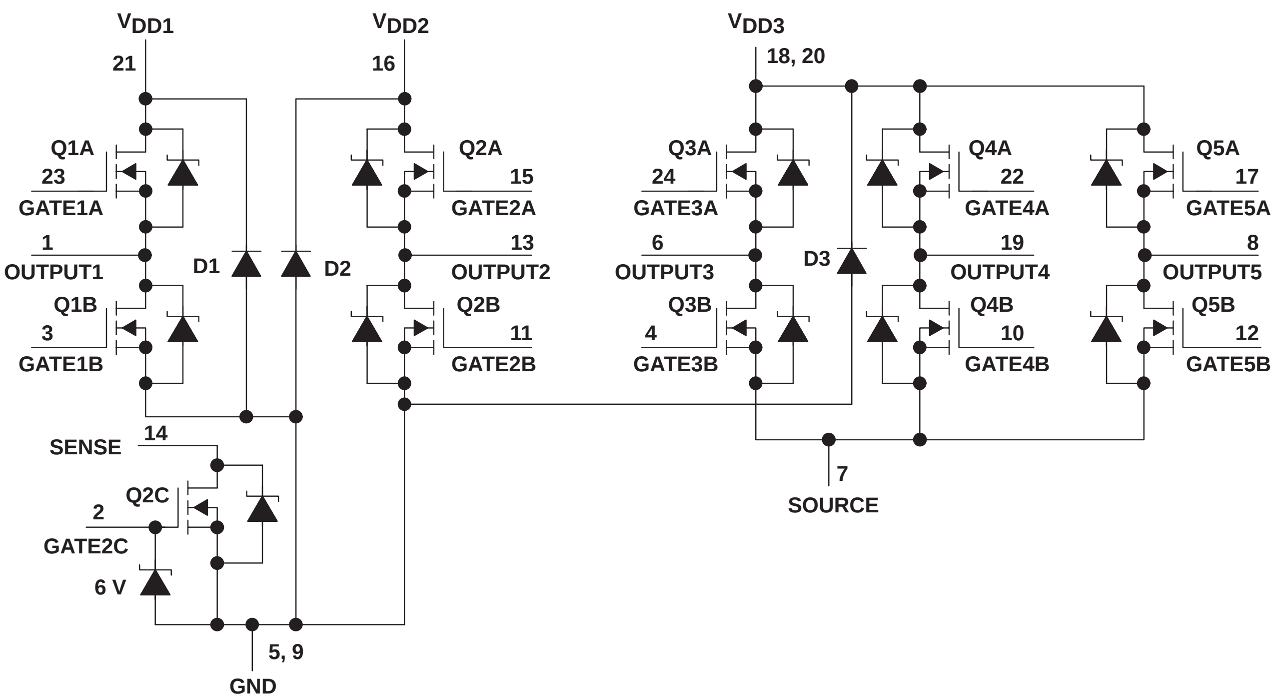


description

The TPIC1504 is a monolithic power DMOS array that consists of ten electrically isolated N-channel enhancement-mode power DMOS transistors, four of which are configured as a full H-bridge and six as a triple half H-bridge. The lower stage of the full H-bridge is provided with an integrated sense-FET to allow biasing of the bridge in class A-B operation.

The TPIC1504 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of –40°C to 125°C.

schematic



NOTES: A. Terminals 5 and 9 must be externally connected.
B. Terminals 18 and 20 must bef externally connected.
C. No output may be taken greater than 0.5 V below GND.

absolute maximum ratings, T_C = 25°C (unless otherwise noted)†

Supply-to-GND voltage	20 V
Source-to-GND voltage (Q3A, Q4A, Q5A)	20 V
Output-to-GND voltage	20 V
Sense-to-GND voltage	20 V
Gate-to-source voltage range, V_{GS} (Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	±20 V
Gate-to-source voltage, V_{GS} (Q2C)	–0.7 V to 6 V
Continuous gate-to-source zener-diode current (Q2C)	±10 mA
Pulsed gate-to-source zener-diode current (Q2C)	±50 mA
Continuous drain current, each output (Q1A, Q1B, Q2A, Q2B)	1.5 A
Continuous drain current, each output (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	2 A
Continuous drain current (Q2C)	5 mA
Continuous source-to-drain diode current (Q1A, Q1B, Q2A, Q2B)	1.5 A
Continuous source-to-drain diode current (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B)	2 A
Continuous source-to-drain diode current (Q2C)	5 mA
Pulsed drain current, each output, I_{max} (Q1A, Q1B, Q2A, Q2B) (see Note 1 and Figure 24)	6 A
Pulsed drain current, each output, I_{max} (Q3A, Q3B, Q4A, Q4B, Q5A, Q5B) (see Note 1 and Figure 25)	8 A
Pulsed drain current, each output, I_{max} (Q2C) (see Note 1)	20 mA
Continuous total power dissipation, T_C = 70°C (see Note 2 and Figures 24 and 25)	2.86 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Pulse duration = 10 ms, duty cycle = 2%
2. Package mounted in intimate contact with infinite heatsink.

electrical characteristics, Q1A, Q1B, Q2A, Q2B, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, $V_{DS} = V_{GS}$, See Figure 5		1.5	1.9	2.2	V
$V_{GS(th)match}$	Gate-to-source threshold voltage matching	I_D = 1 mA, $V_{DS} = V_{GS}$				40	mV
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 µA (D1, D2)		20			V
$V_{(BR)GS}$	Gate-to-source threshold breakdown voltage, Q2C	I_{GS} = 100 µA		6			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage, Q2C	I_{SG} = 100 µA		0.5			V
$V_{(DS)on}$	Drain-to-source on-state voltage	I_D = 1.5 A, V_{GS} = 10 V, See Notes 3 and 4			0.375	0.45	V
V_F	Forward on-state voltage, GND-to-V_{DD1}, GND-to-V_{DD2}	I_D = 1.5 A (D1, D2) See Notes 3 and 4			1.7		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 1.5 A, V_{GS} = 0, See Notes 3 and 4 and Figure 19			0.85	1.2	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 16 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short-circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short-circuited to source	V_{SG} = 0.5 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, V_{DD1}-to-GND, V_{DD2}-to-GND, gate shorted to source	V_{DGND} = 16 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 1.5 A, See Notes 3 and 4 and Figure 9	T_C = 25°C		0.25	0.3	Ω
			T_C = 125°C		0.4	0.475	
g_{fs}	Forward transconductance	V_{DS} = 14 V, I_D = 750 mA, See Notes 3 and 4 and Figure 13		0.8	1.2		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 14 V, V_{GS} = 0, f = 1 MHz, See Figure 17			99		pF
C_{oss}	Short-circuit output capacitance, common source				81		
C_{rss}	Short-circuit reverse transfer capacitance, common source				59		
α_S	Sense-FET drain current ratio	V_{DS} = 6 V, $I_{D(Q2C)}$ = 40 µA		100	150	200	

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, Q1A, Q2A, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 750 mA, V_{GS} = 0, V_{DS} = 14 V, di/dt = 100 A/µs, See Figures 1 and 23		18		ns
Q_{RR}	Total diode charge			13		nC

resistive-load switching characteristics, Q1A, Q1B, Q2A, Q2B, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 14 V, R_L = 18.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 3		11		ns
$t_{d(off)}$	Turn-off delay time			16		
t_r	Rise time			3		
t_f	Fall time			4		
Q_g	Total gate charge	V_{DS} = 14 V, I_D = 750 mA, V_{GS} = 10 V, See Figure 4 and Figure 21		1.8	2.5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.3	0.4	
Q_{gd}	Gate-to-drain charge			0.5	0.6	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		
R_g	Internal gate resistance			10		Ω

electrical characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 250 µA, V_{GS} = 0		20			V
$V_{GS(th)}$	Gate-to-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}, See Figure 6		1.5	1.9	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage	Drain-to-GND current = 250 µA (D3)		20			V
$V_{(DS)on}$	Drain-to-source on-state voltage	I_D = 2 A, V_{GS} = 10 V, See Notes 3 and 4			0.3	0.35	V
V_F	Forward on-state voltage, GND-to-V_{DD3}	I_D = 2 A (D3), See Notes 3 and 4			1.5		V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	I_S = 2 A, V_{GS} = 0 See Notes 3 and 4 and Figure 20			0.85	1.2	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 16 V, V_{GS} = 0	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short-circuited to source	V_{GS} = 16 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short-circuited to source	V_{SG} = 16 V, V_{DS} = 0			10	100	nA
I_{lkg}	Leakage current, V_{DD3}-to-GND, gate shorted to source	V_{DGND} = 16 V	T_C = 25°C		0.05	1	µA
			T_C = 125°C		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	V_{GS} = 10 V, I_D = 2 A, See Notes 3 and 4 and Figure 10	T_C = 25°C		0.15	0.175	Ω
			T_C = 125°C		0.24	0.275	
g_{fs}	Forward transconductance	V_{DS} = 14 V, I_D = 1 A, See Notes 3 and 4 and Figure 14		1	1.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 14 V, V_{GS} = 0, f = 1 MHz, See Figure 18			160		pF
C_{oss}	Short-circuit output capacitance, common source				220		
C_{rss}	Short-circuit reverse transfer capacitance, common source				110		

NOTES: 3: Technique should limit T_J – T_C to 10°C maximum.
4: These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, Q3A, Q4A, Q5A, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse-recovery time	I_S = 1 A, V_{GS} = 0, V_{DS} = 14 V, di/dt = 100 A/µs, See Figures 2 and 23		34		ns
Q_{RR}	Total diode charge			30		nC

resistive-load switching characteristics, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, T_C = 25°C

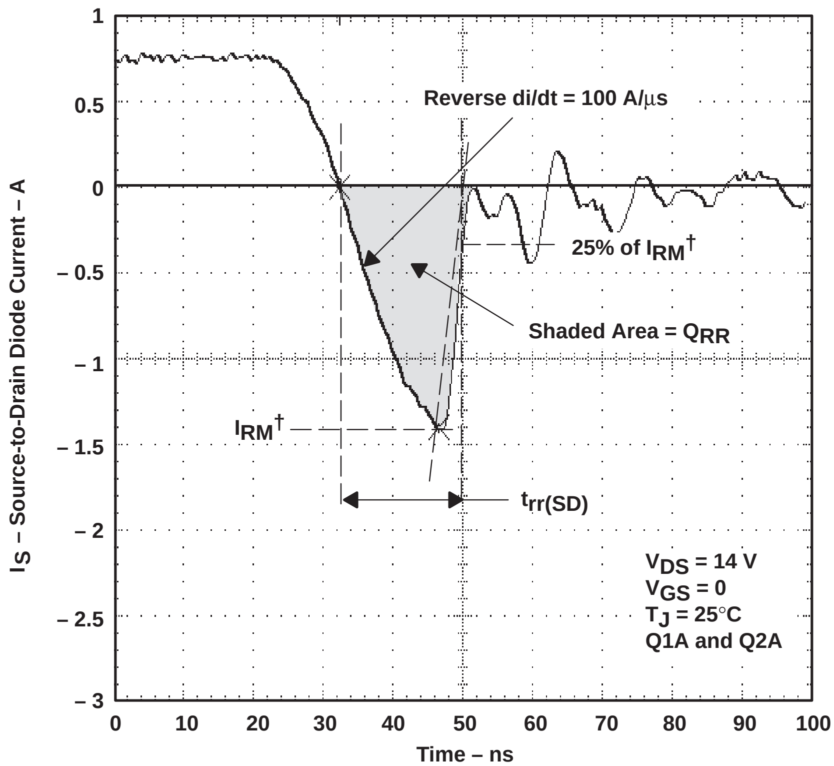
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 14 V, R_L = 14 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 3		30		ns
$t_{d(off)}$	Turn-off delay time			34		
t_r	Rise time			15		
t_f	Fall time			21		
Q_g	Total gate charge	V_{DS} = 14 V, I_D = 1 A, V_{GS} = 10 V, See Figure 4 and Figure 22		3.2	4.5	nC
$Q_{gs(th)}$	Threshold gate-to-source charge			0.5	0.6	
Q_{gd}	Gate-to-drain charge			0.9	1.1	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		
R_g	Internal gate resistance			10		Ω

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 5 and 8		90		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 6 and 8		52		
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 7 and 8		28		

NOTES: 5. Package mounted on a FR4 printed-circuit board with no heatsink.
6. Package mounted on a 24 in^2, 4-layer FR4 printed-circuit board.
7. Package mounted in intimate contact with infinite heatsink.
8. All outputs with equal power

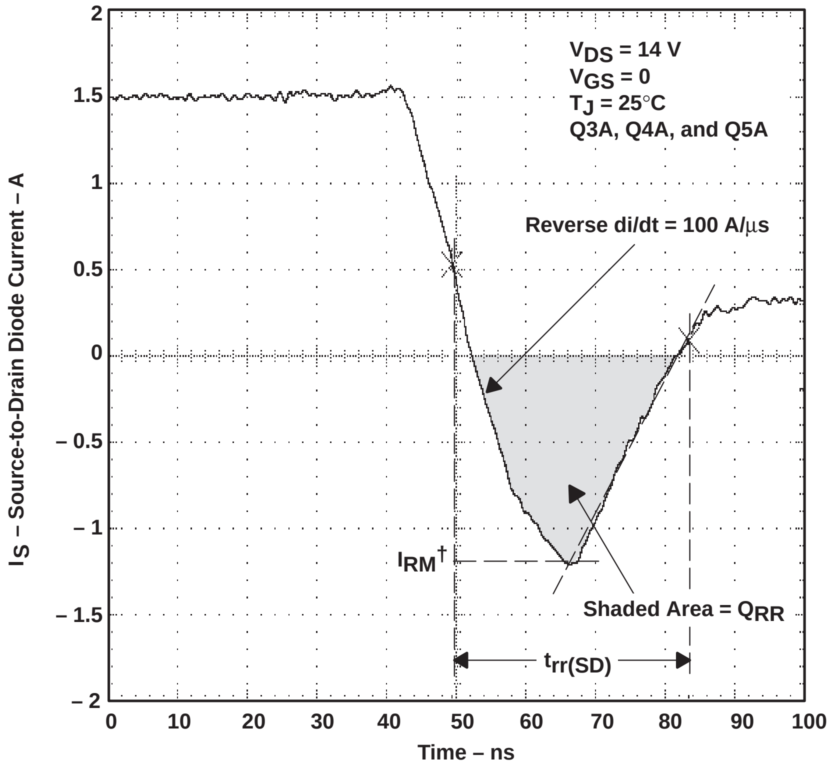
PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

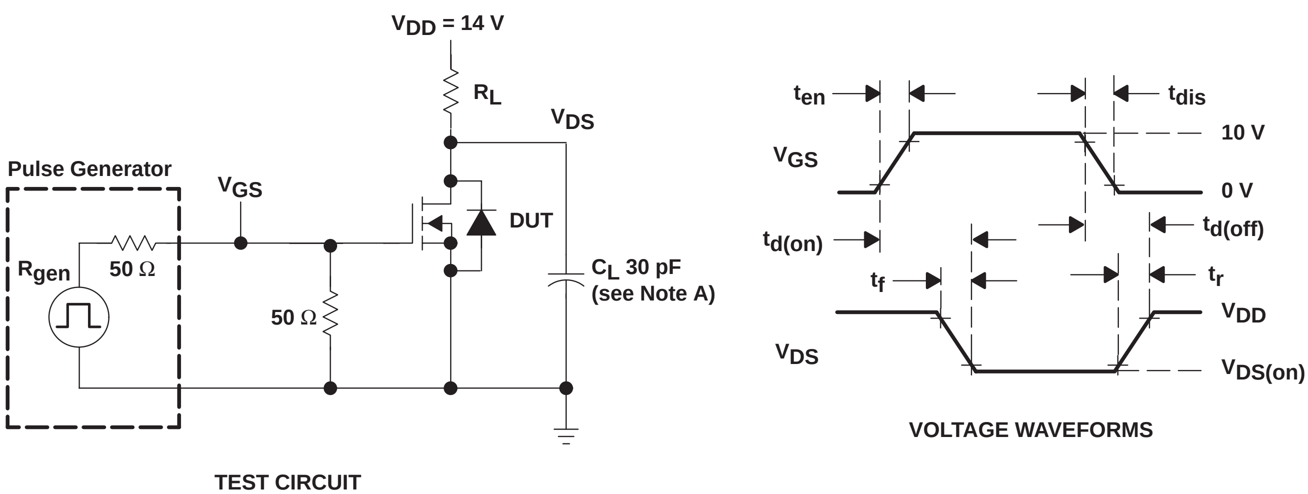
Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes

PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

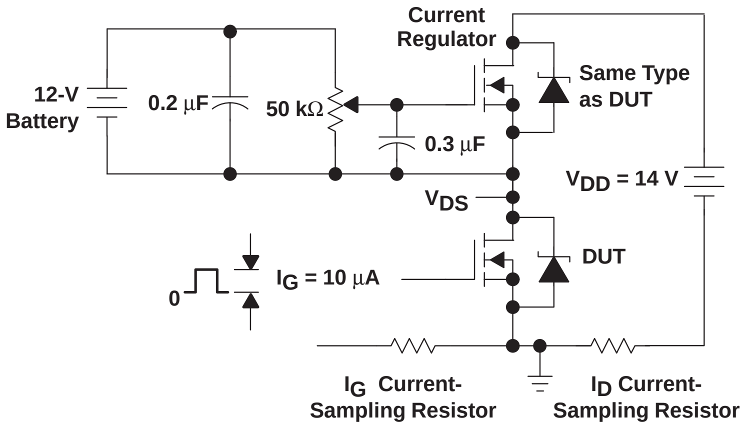
Figure 2. Reverse-Recovery-Current Waveform of Source-to-Drain Diodes



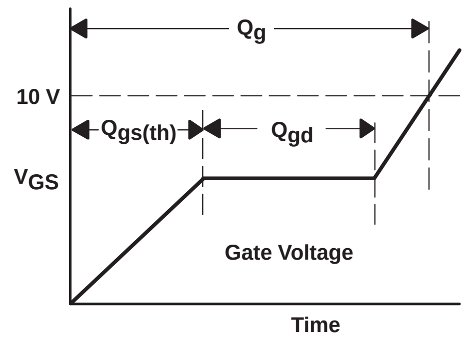
NOTE A: C_L includes probe and jig capacitance.

Figure 3. Resistive-Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

Figure 4. Gate-Charge Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

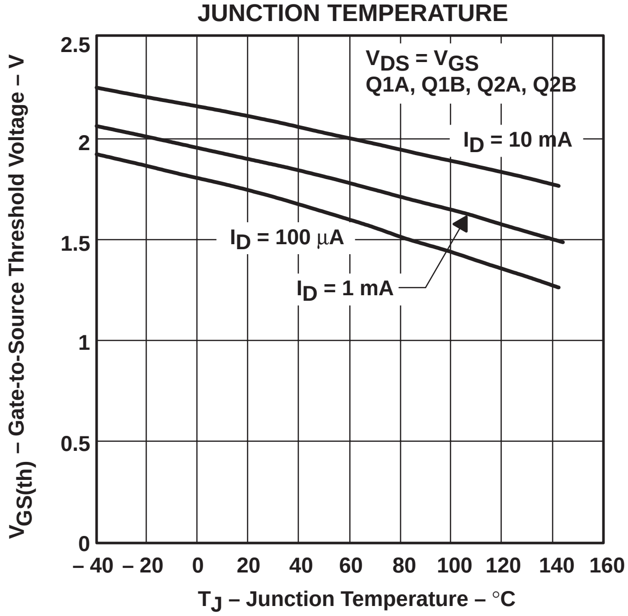


Figure 5

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

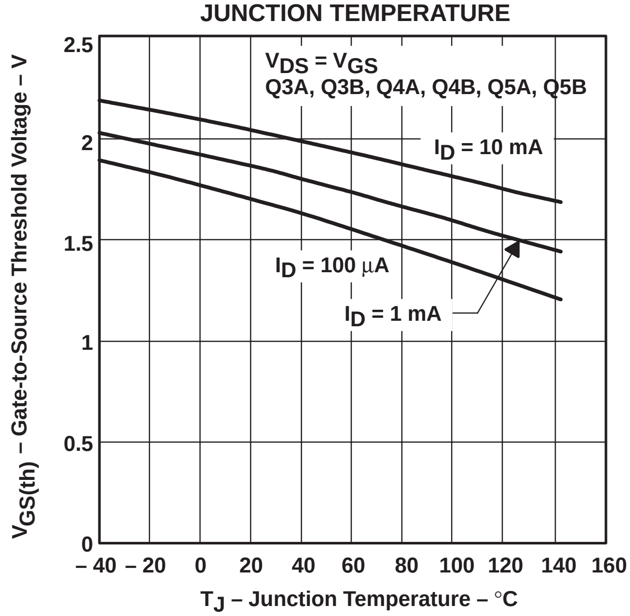


Figure 6

TYPICAL CHARACTERISTICS

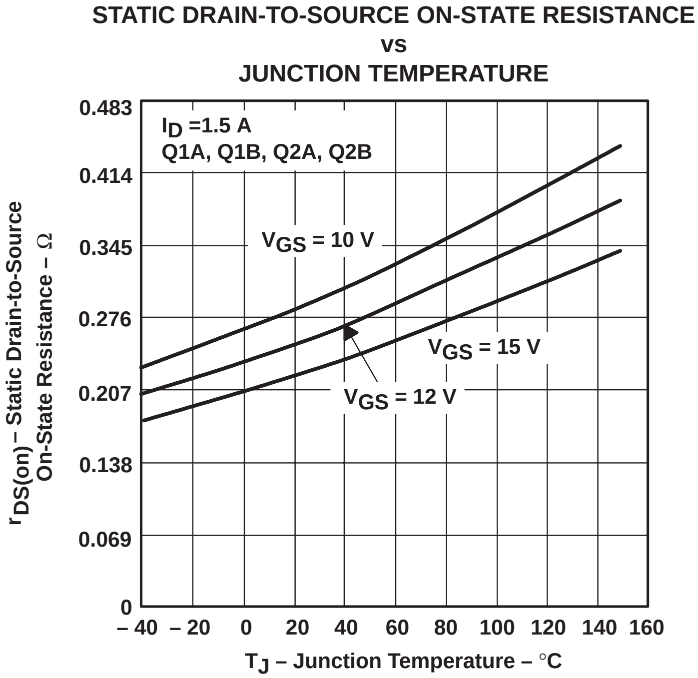


Figure 7

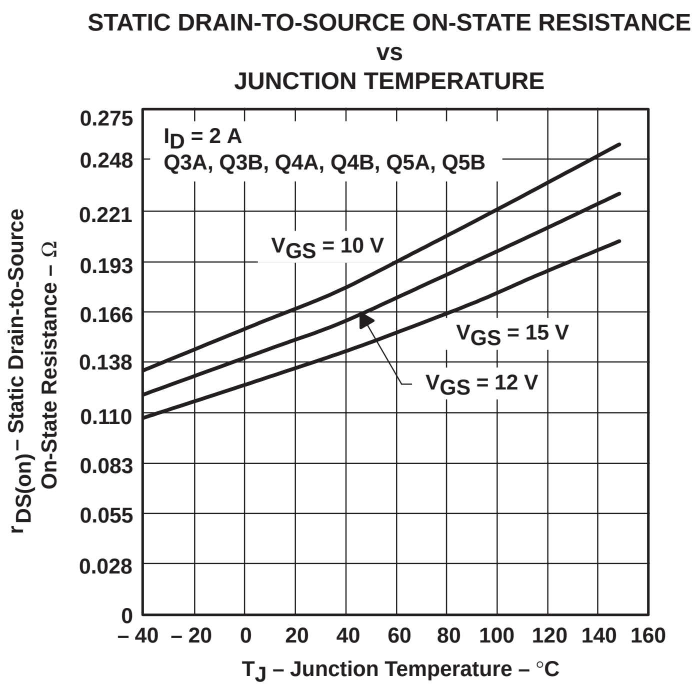


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

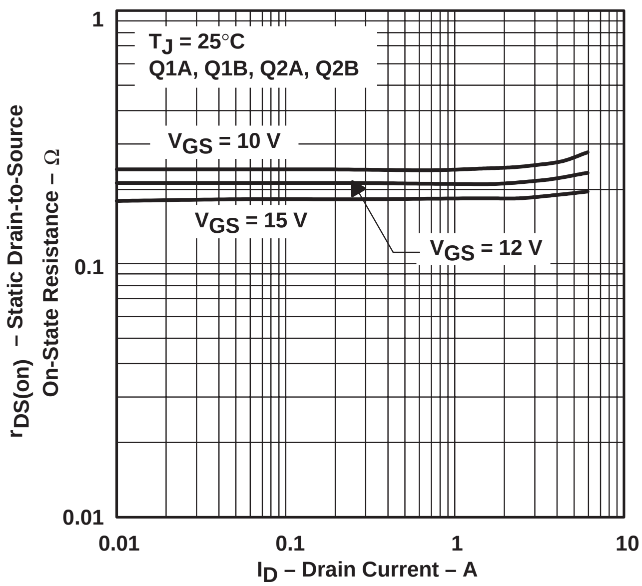


Figure 9

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

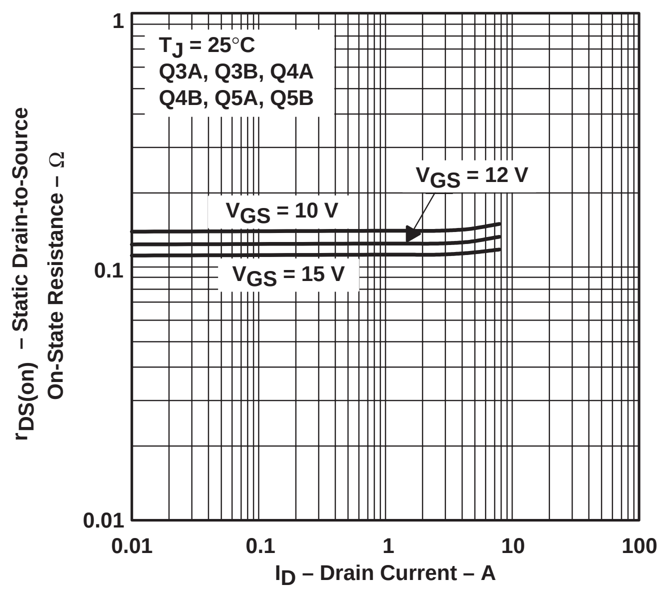


Figure 10

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

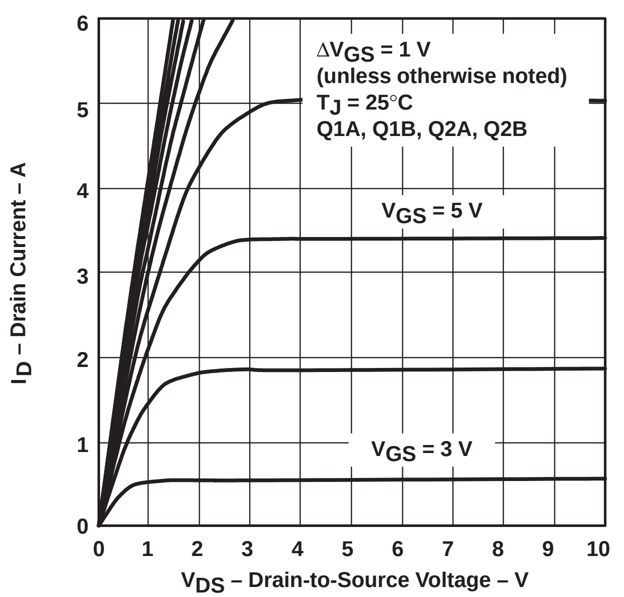


Figure 11

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

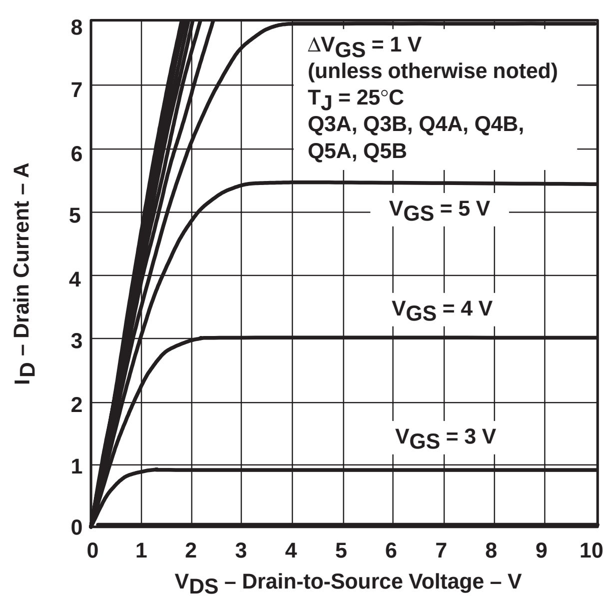


Figure 12

TYPICAL CHARACTERISTICS

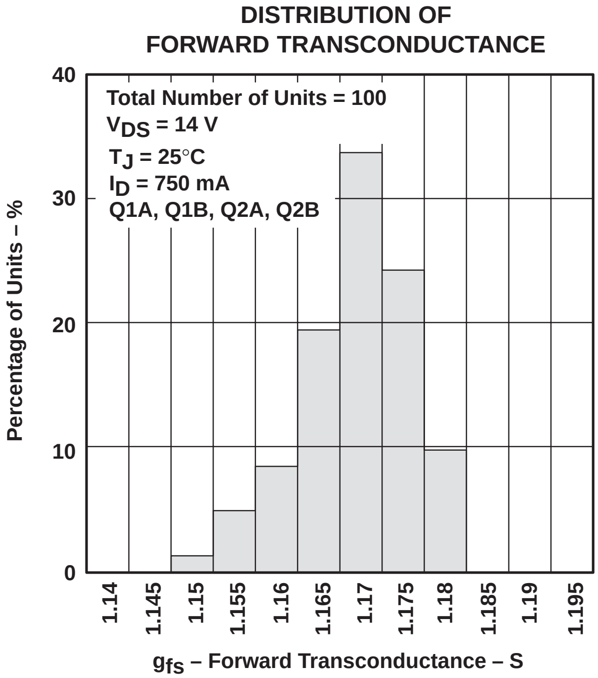


Figure 13

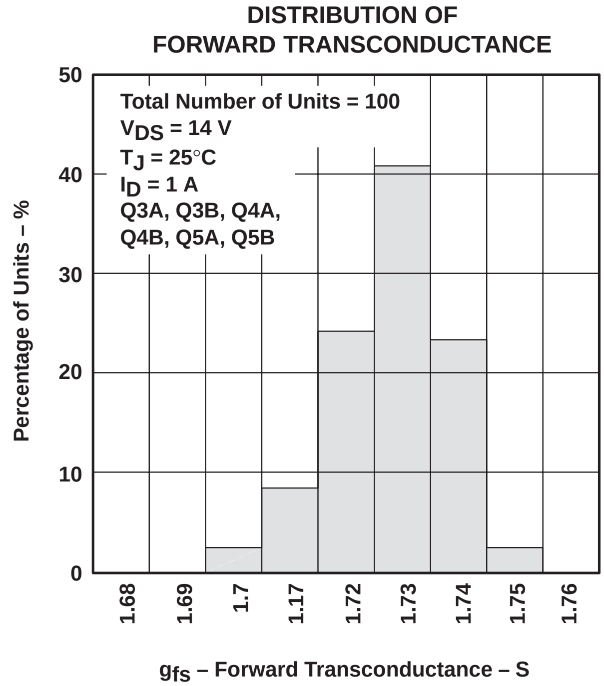


Figure 14

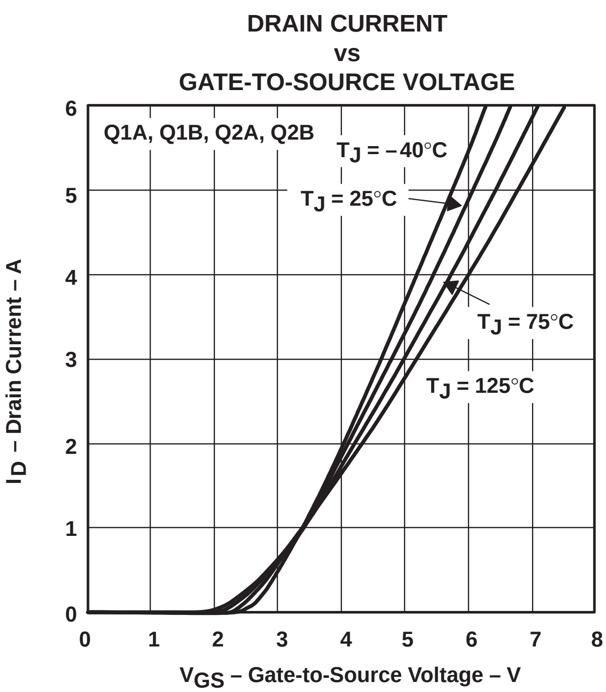


Figure 15

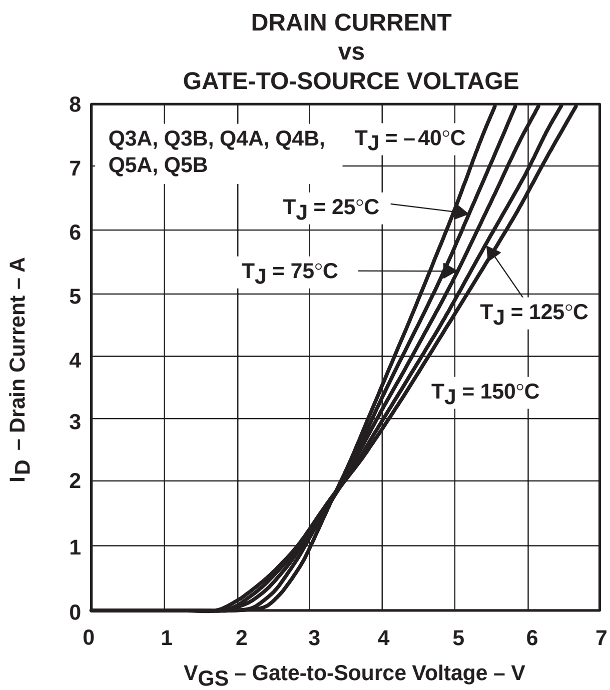


Figure 16

TYPICAL CHARACTERISTICS

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

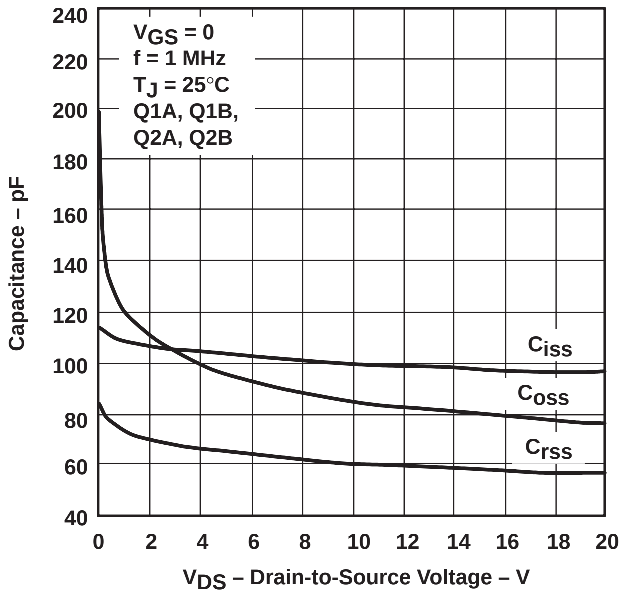


Figure 17

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

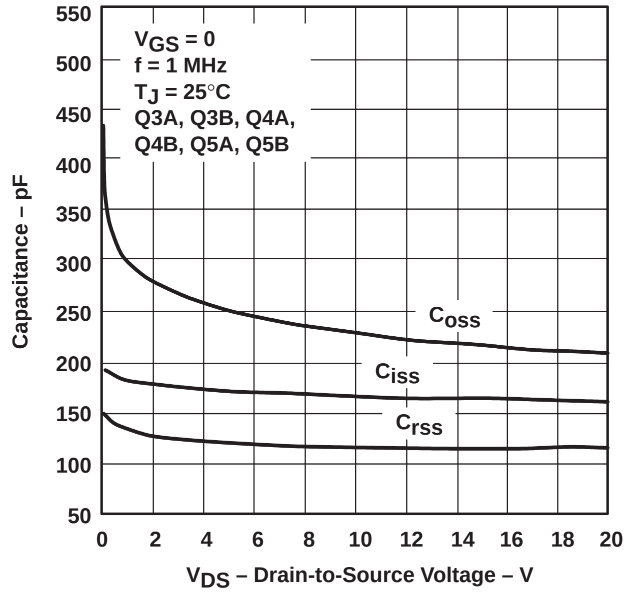


Figure 18

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

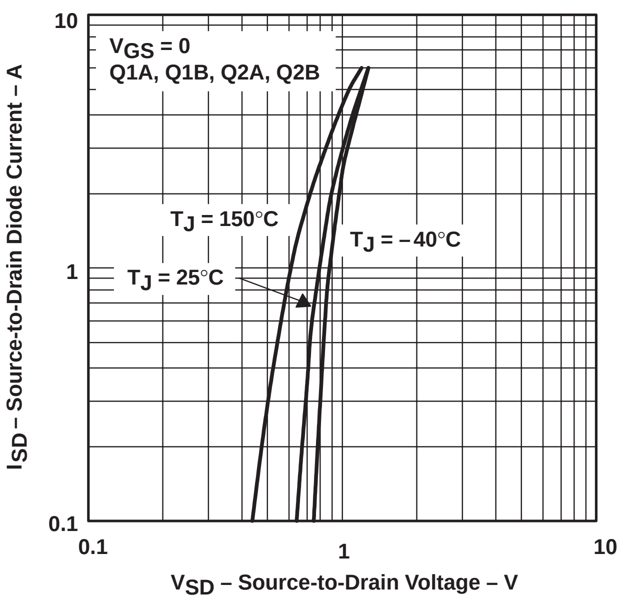


Figure 19

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

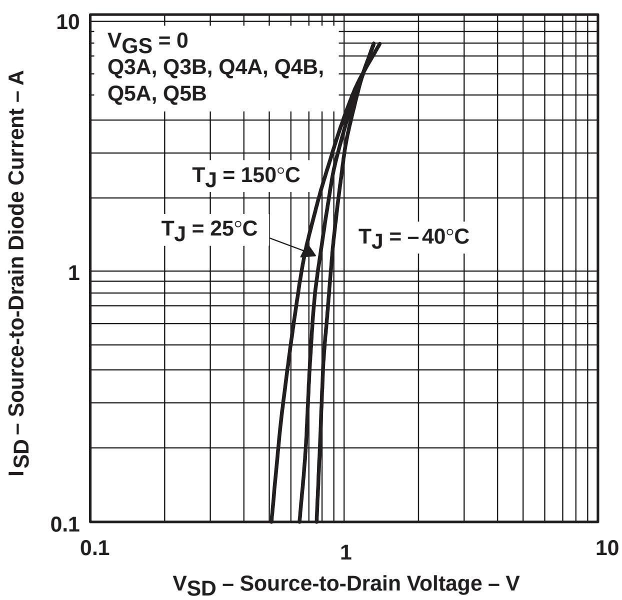


Figure 20

TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

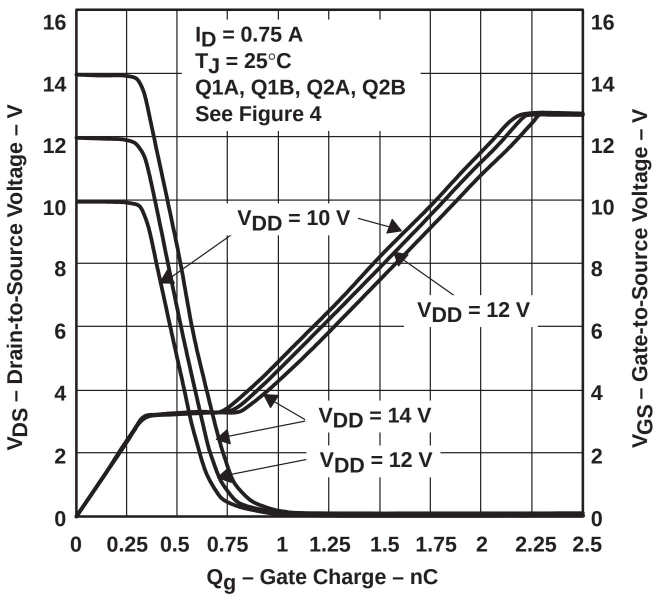


Figure 21

DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

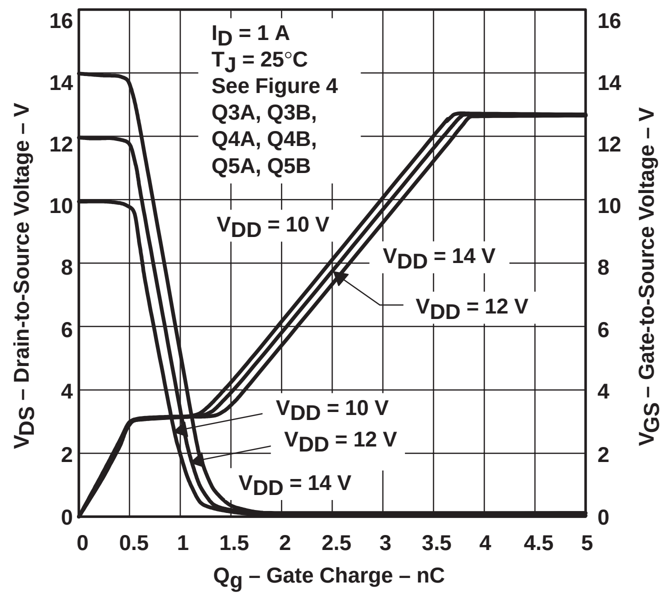


Figure 22

REVERSE RECOVERY TIME vs REVERSE di/dt

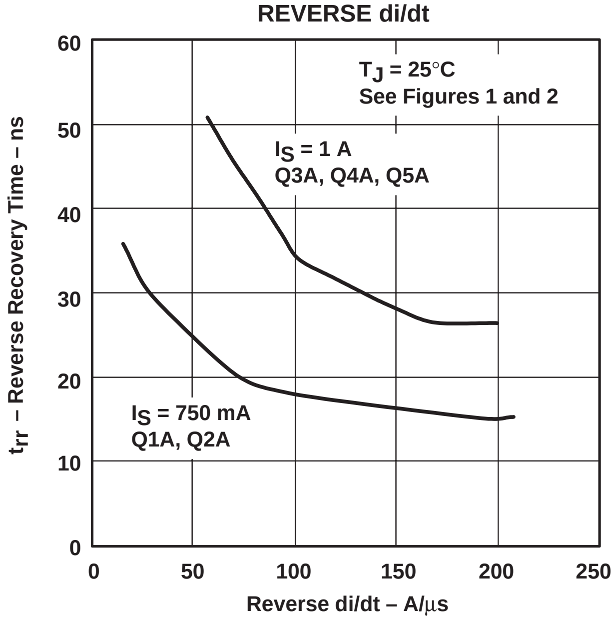


Figure 23

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

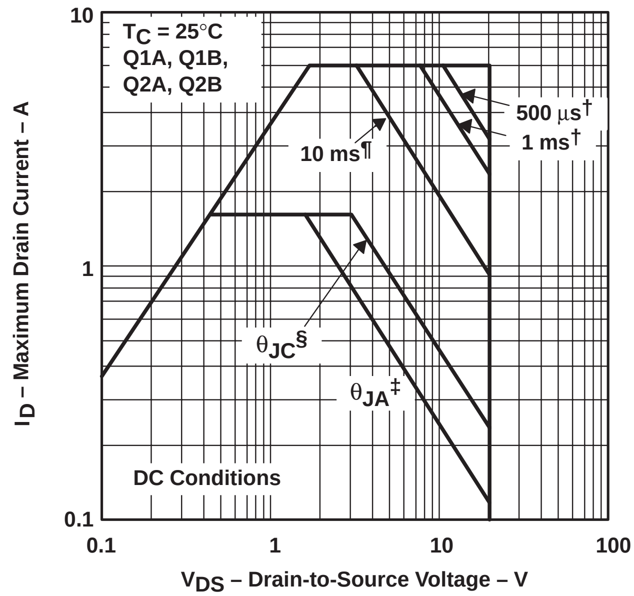


Figure 24

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

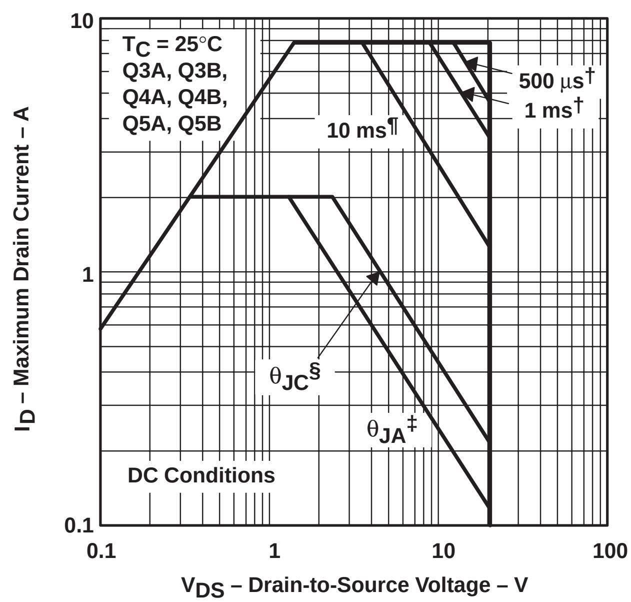
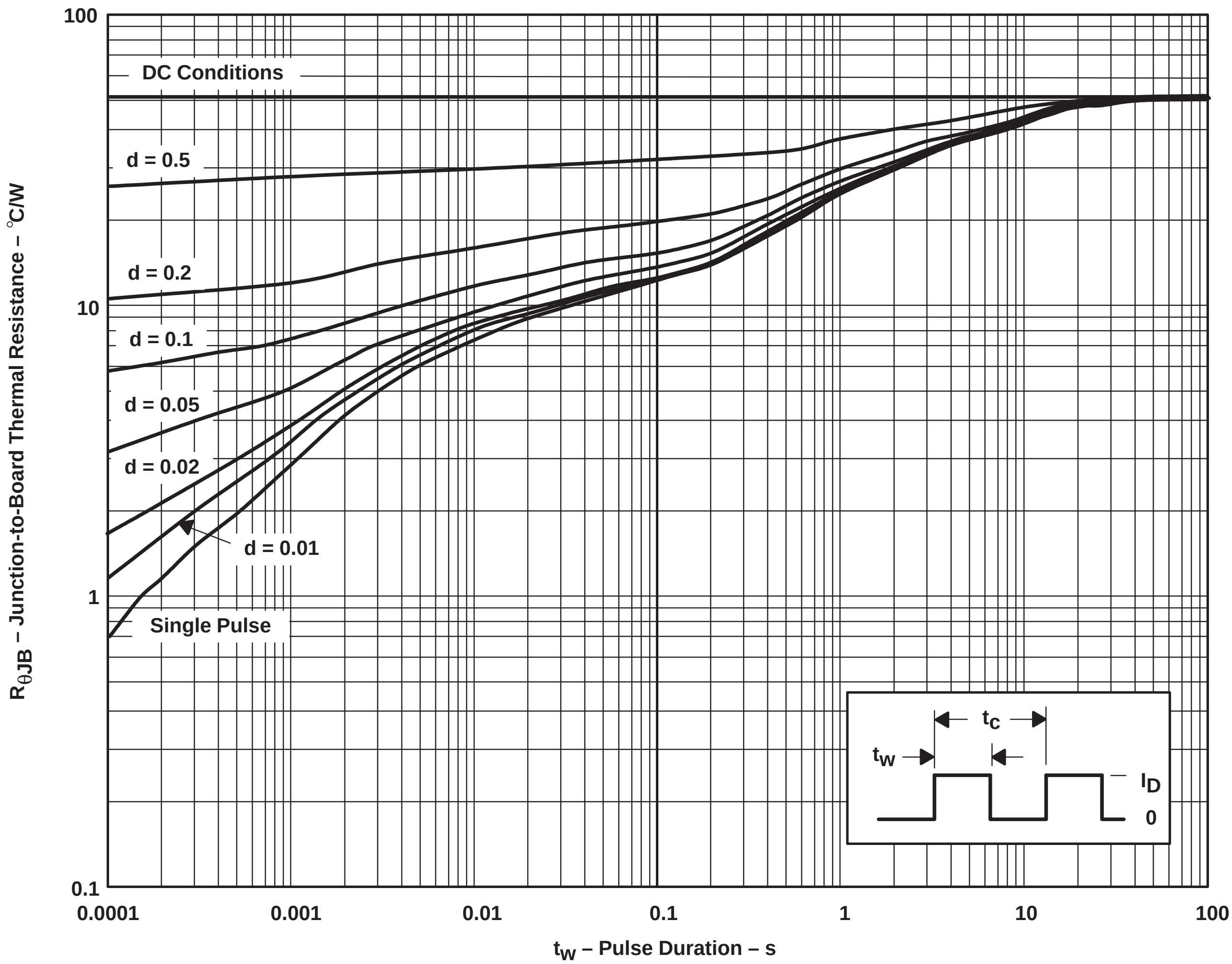


Figure 25

† Less than 10% duty cycle
‡ Device mounted on a 24-in^2, 4-layer FR4 printed-circuit board.
§ Device mounted in intimate contact with infinite heat sink.
¶ Less than 2% duty cycle

THERMAL INFORMATION

DW PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
vs
PULSE DURATION



† Device is mounted on 24-in², 4-layer FR4 printed circuit board with no heat sink.

NOTE A: $Z_{\theta B}(t) = r(t)\ R_{\theta JB}$
t_W = pulse duration
t_c = cycle time
d = duty cycle = t_W/t_c

Figure 26