

Dual Supply Octal Translating Transceiver

with 3-State Outputs

MC74LVX4245

The 74LVX4245 is a 24–pin dual–supply, octal translating transceiver that is designed to interface between a 5.0~V bus and a 3.0~V bus in a mixed 3.0~V / 5.0~V supply environment such as laptop computers using a 3.3~V CPU and 5.0~V LCD display. The A port interfaces with the 5V bus; the B port interfaces with the 3.0~V bus.

The Transmit/Receive (T/\overline{R}) input determines the direction of data flow. Transmit (active–High) enables data from the A port to the B port. Receive (active–Low) enables data from the B port to the A port. The Output Enable (\overline{OE}) input, when High, disables both A and B ports by placing them in 3–State.

Features

- Bi-directional Interface Between 5.0 V and 3.0 V Buses
- Control Inputs Compatible with TTL Level
- 5.0 V Data Flow at A Port and 3.0 V Data Flow at B Port
- Outputs Source/Sink 24 mA at 5.0 V Bus and 12 mA at 3.0 V Bus
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Available in SOIC and TSSOP Packages
- Functionally Compatible with the 74 Series 245
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

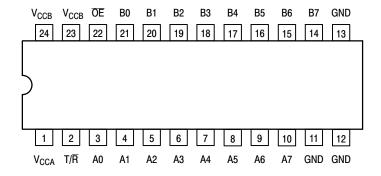
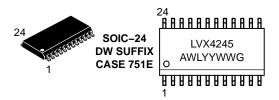


Figure 1. 24-Lead Pinout (Top View)

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MARKING DIAGRAMS







LVX4245 = Specific Device Code A = Assembly Location WL, L = Wafer Lot

Y = Year WW, W = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN NAMES

Pins	Function
ŌE T/R	Output Enable Input Transmit/Receive Input
A0-A7	Side A 3–State Inputs or 3–State Outputs
B0-B7	Side B 3–State Inputs or 3–State Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

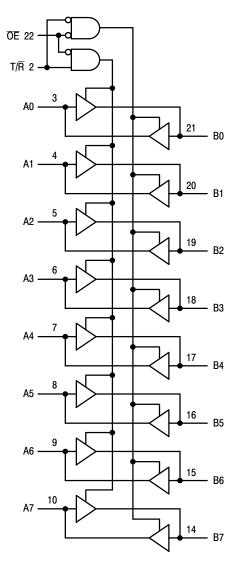


Figure 2. Logic Diagram

INP	UTS	OPERATING MODE
ŌĒ	T/R	OPERATING MODE Non-Inverting
L	L	B Data to A Bus
L	Н	A Data to B Bus
Н	X	Z

 $H = High\ Voltage\ Level;\ L = Low\ Voltage\ Level;\ Z = High\ Impedance\ State;\ X = High\ or\ Low\ Voltage\ Level$ and Transitions are Acceptable; For ICC reasons, Do Not Float Inputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Paramet	er	Value	Condition	Unit
V _{CCA} , V _{CCB}	DC Supply Voltage		-0.5 to +7.0		V
VI	DC Input Voltage	ŌE, T/R	–0.5 to V _{CCA} +0.5		V
V _{I/O}	DC Input/Output Voltage	An	–0.5 to V _{CCA} +0.5		V
		Bn	–0.5 to V _{CCB} +0.5		V
I _{IK}	DC Input Diode Current	ŌĒ, T∕R	±20	V _I < GND	mA
I _{OK}	DC Output Diode Current		±50	$V_O < GND; V_O > V_{CC}$	mA
Io	DC Output Source/Sink Current		±50		mA
I _{CC} , I _{GND}	DC Supply Current	Per Output Pin Maximum Current at I _{CCA} Maximum Current at I _{CCB}	±50 ±200 ±100		mA
T _{STG}	Storage Temperature Range		-65 to +150		°C
Latchup	DC Latchup Source/Sink Current		±300		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Paramete	Parameter		Min	Max	Unit
V _{CCA} , V _{CCB}	Supply Voltage	V _{CCA} V _{CCB}		4.5 2.7	5.5 3.6	V
VI	Input Voltage	ŌĒ, T/R		0	V _{CCA}	V
V _{I/O}	Input/Output Voltage	An Bn		0 0	V _{CCA} V _{CCB}	V
T _A	Operating Free–Air Temperature			-40	+85	°C
Δt/ΔV	Minimum Input Edge Rate V_{IN} from 30% to 70% of V_{CC} ; V_{CC} at 3.0V, 4.5V, 5.5V		0	8	ns/V	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

						T _A =	25°C	T _A = -40 to +85°C	
Symbol	Parameter		Condition	V _{CCA}	V _{CCB}	Тур	Typ Guaranteed Limits		Unit
V _{IHA}	Minimum HIGH Level	An, OE T/R	V _{OUT} ≤ 0.1V	5.5 4.5	3.3 3.3		2.0 2.0	2.0 2.0	V
V _{IHB}	Input Voltage	Bn	or ≥ V _{CC} – 0.1V	5.0 5.0	3.6 2.7		2.0 2.0	2.0 2.0	V
V _{ILA}	Maximum LOW Level	An, OE T/R	V _{OUT} ≤ 0.1V	5.5 4.5	3.3 3.3		0.8 0.8	0.8 0.8	V
V _{ILB}	Input Voltage	Bn	or ≥ V _{CC} – 0.1V	5.0 5.0	2.7 3.6		0.8 0.8	0.8 0.8	V
V _{OHA}	Minimum HIGH Level		I _{OUT} = -100μA I _{OH} = -24mA	4.5 4.5	3.0 3.0	4.50 4.25	4.40 3.86	4.40 3.76	V
V _{OHB}	Output Voltage		$I_{OUT} = -100\mu A$ $I_{OH} = -12mA$ $I_{OH} = -8mA$	4.5 4.5 4.5	3.0 3.0 2.7	2.99 2.80 2.50	2.9 2.4 2.4	2.9 2.4 2.4	V
V _{OLA}	Maximum LOW Level		$I_{OUT} = 100\mu A$ $I_{OL} = 24mA$	4.5 4.5	3.0 3.0	0.002 0.18	0.10 0.36	0.10 0.44	V
V _{OLB}	Output Voltage		$I_{OUT} = 100 \mu A$ $I_{OL} = 12 m A$ $I_{OL} = 8 m A$	4.5 4.5 4.5	3.0 3.0 2.7	0.002 0.1 0.1	0.10 0.31 0.31	0.10 0.40 0.40	V

DC ELECTRICAL CHARACTERISTICS

						T _A =	25°C	T _A = -40 to +85°C		
Symbol	ol Parameter		Condition	V _{CCA}	V _{CCB}	Тур	G	uaranteed Limits	Unit	
I _{IN}	Max Input Leak- age Current	ŌĒ, T∕R	V _I = V _{CCA} , GND	5.5	3.6		±0.1	±1.0	μΑ	
I _{OZA}	Max 3–State Out- put Leakage	An	$V_{I} = V_{IH}, V_{IL}$ $\overline{OE} = V_{CCA}$ $V_{O} = V_{CCA}, GND$	5.5	3.6		±0.5	±5.0	μΑ	
I _{OZB}	Max 3–State Out- put Leakage	Bn	$\begin{aligned} & V_{I} = V_{IH}, \ V_{IL} \\ & \overline{OE} = V_{CCA} \\ & V_{O} = V_{CCB}, \ GND \end{aligned}$	5.5	3.6		±0.5	±5.0	μΑ	
ΔI_{CC}	Maximum I _{CCT} per Input	An, OE T/R	V _I =V _{CCA} -2.1V	5.5	3.6	1.0	1.35	1.5	mA	
		Bn	V _I =V _{CCB} -0.6V	5.5	3.6		0.35	0.5	mA	
I _{CCA}	Quiescent V _{CCA} Supply Current		An=V _{CCA} or GND Bn=V _{CCB} or GND OE=GND T/R=GND	5.5	3.6		8	80	μΑ	
I _{CCB}	Quiescent V _{CCB} Supply Current		$\begin{array}{c} \text{An=V}_{\text{CCA}} \text{ or GND} \\ \text{Bn=V}_{\text{CCB}} \text{ or GND} \\ \hline \text{OE=GND} \\ \text{T/\overline{R}=$V}_{\text{CCA}} \end{array}$	5.5	3.6		5	50	μΑ	
V _{OLPA} V _{OLPB}	Quiet Output Max Dynamic V _{OL}		Notes 1, 2	5.0 5.0	3.3 3.3		1.5 1.2		V	
V _{OLVA} V _{OLVB}	Quiet Output Min Dynamic V _{OL}		Notes 1, 2	5.0 5.0	3.3 3.3		-1.2 -0.8		V	
V _{IHDA} V _{IHDB}	Min HIGH Level Dynamic Input Voltage		Notes 1, 3	5.0 5.0	3.3 3.3		2.0 2.0		V	
V _{ILDA} V _{ILDB}	Max LOW Level Dynamic Input Voltage		Notes 1, 3	5.0 5.0	3.3 3.3		0.8 0.8		V	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Worst case package.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	input Capacitance $V_{CCA} = 5.0V; V_{CCB} = 3.3V$		4.5	pF
C _{I/O}	Input/Output Capacitance	$V_{CCA} = 5.0V; V_{CCB} = 3.3V$	15	pF
C _{PD}	Power Dissipation Capacitance $B \rightarrow A$ (Measured at 10MHz) $A \rightarrow E$	COA	55 40	pF

Worst case package.
 Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.
 Max number of data inputs (n) switching. (n-1) inputs switching 0V to V_{CC} level. Input under test switching: V_{CC} level to threshold (V_{ILD}), 0V to threshold (V_{ILD}), f = 1MHz.

AC ELECTRICAL CHARACTERISTICS

		TA	= -40 to +85 C _L = 50pF	5°C	T _A = -40 C _L =		
		۷ ₀	$_{CA}$ = 5V ±0. $_{CB}$ = 3.3V ±0	5V .3V	$V_{CCA} = 5V \pm 0.5V$ $V_{CCB} = 2.7V$		
Symbol	Parameter	Min	Typ (Note 4)	Max	Min	Max	Unit
t _{PHL} t _{PLH}	Propagation Delay A to B	1.0 1.0	5.1 5.3	9.0 9.0	1.0 1.0	10.0 10.0	ns
t _{PHL}	Propagation Delay B to A	1.0 1.0	5.4 5.5	9.0 9.0	1.0 1.0	10.0 10.0	ns
t _{PZL} t _{PZH}	Output Enable Time OE to B	1.0 1.0	6.5 6.7	10.5 10.5	1.0 1.0	11.5 11.5	ns
t _{PZL} t _{PZH}	Output Enable Time OE to A	1.0 1.0	5.2 5.8	9.5 9.5	1.0 1.0	10.0 10.0	ns
t _{PHZ}	Output Disable Time OE to B	1.0 1.0	6.0 3.3	10.0 7.0	1.0 1.0	10.0 7.5	ns
t _{PHZ}	Output Disable Time OE to A	1.0 1.0	3.9 2.9	7.5 7.0	1.0 1.0	7.5 7.5	ns
toshl toslh	Output to Output Skew, Data to Output (Note 5)		1.0	1.5		1.5	ns

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX4245DWR2G	SOIC-24 (Pb-Free)	1000 / Tape & Reel
MC74LVX4245DTR2G	TSSOP-24 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 6)

MC74LVX4245DWG	SOIC-24 (Pb-Free)	30 Units / Rail
MC74LVX4245DTG	TSSOP-24	62 Units / Rail
NLVLVX4245DTR2G*	(Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Typical values at V_{CCA} = 5.0V; V_{CCB} = 3.3V at 25°C.
 Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter
 guaranteed by design.

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

^{6.} DISCONTINUED: These devices are not recommended for new design. Please contact your onsemi representative for information. The most current information on these devices may be available on www.onsemi.com.

Dual Supply Octal Translating Transceiver

The 74LVX4245 is a is a dual—supply device well capable of bidirectional signal voltage translation. This level shifting ability provides an excellent interface between low voltage CPU local bus and a standard 5.0 V I/O bus. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5.0 V I/O levels.

The LVX4245 is ideal for mixed voltage applications such as notebook computers using a 3.3 V CPU and 5.0 V peripheral devices.

Applications:

Mixed Mode Dual Supply Interface Solutions

The LVX4245 is designed to solve 3.0~V/5.0~V interfaces when CMOS devices cannot tolerate I/O levels above their applied $V_{\rm CC}$. If an I/O pin of a 3.0~V device is driven by a 5.0~V device, the P–Channel transistor in the 3.0~V device will conduct – causing current flow from the I/O bus to the 3.0~V power supply. The result may be destruction of the 3.0~V device through latchup effects. A current limiting resistor may be used to prevent destruction, but it causes speed degradation and needless power dissipation.

A better solution is provided in the LVX4245. It provides two different output levels that easily handle the dual voltage interface. The A port is a dedicated 5.0 V port; the B port is a dedicated 3.0 V port.

Since the LVX4245 is a '245 transceiver, the user may either use it for bidirectional or unidirectional applications. The center 20 pins are configured to match a '245 pinout. This enables the user to easily replace this level shifter with a 3.0 V '245 device without additional layout work or remanufacture of the circuit board (when both buses are 3.0 V).

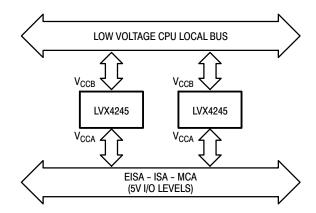


Figure 3. 3.3V/5V Interface Block Diagram

Powering Up the LVX4245

When powering up the LVX4245, please note that if the V_{CCB} pin is powered—up well in advance of the V_{CCA} pin, several milliamps of either I_{CCA} or I_{CCB} current will result. If the V_{CCA} pin is powered—up in advance of the V_{CCB} pin then only nanoamps of Icc current will result. In actuality the V_{CCB} can be powered "slightly" before the V_{CCA} without the current penalty, but this "setup time" is dependent on the power—up ramp rate of the V_{CC} pins. With a ramp rate of approximately 50 mV/ns (50V/ μ s) a 25 ns setup time was observed (V_{CCB} before V_{CCA}). With a 7.0 V/ μ s rate, the setup time was about 140ns. When all is said and done, the safest powerup strategy is to simply power V_{CCA} before V_{CCB} . One more note: if the V_{CCB} ramp rate is faster than the V_{CCA} ramp rate then power problems might still occur, even if the V_{CCA} powerup began prior to the V_{CCB} powerup.

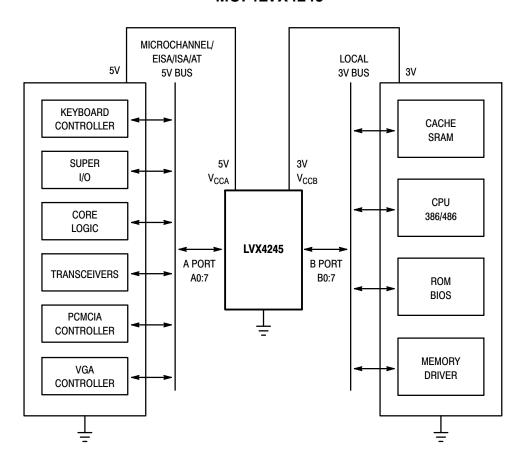


Figure 4. MC74LVX4245 Fits Into a System with 3V Subsystem and 5V Subsystem

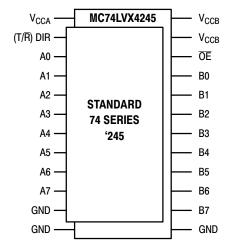
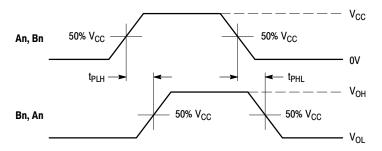
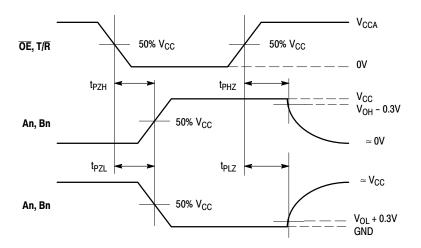


Figure 5. MC74LVX4245 Pin Arrangement Is Compatible to 20-Pin 74 Series '245s



WAVEFORM 1 - PROPAGATION DELAYS

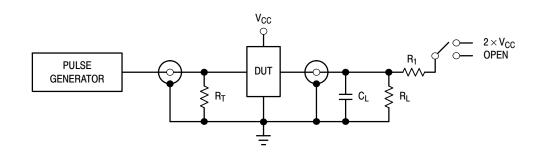
 t_R = t_F = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES

 t_R = t_F = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 6. AC Waveforms



TEST	SWITCH
t _{PLH} , t _{PHL} , t _{PZH} , t _{PHZ}	Open
t _{PZL} , t _{PLZ}	$2 \times V_{CC}$

C_L = 50pF or equivalent (Includes jig and probe capacitance)

 $R_L = R_1 = 500\Omega$ or equivalent

 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

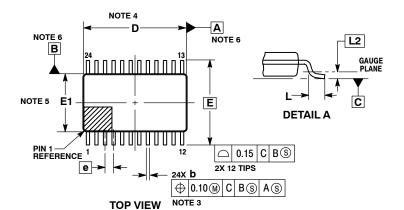
Figure 7. Test Circuit

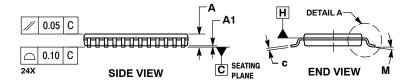




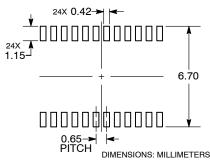
TSSOP24 7.8x4.4, 0.65P CASE 948H **ISSUE B**

DATE 21 JUN 2012





RECOMMENDED SOLDERING FOOTPRINT*



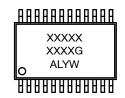
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
 A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEAT-
- ING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIN	IETERS		
DIM	MIN	MAX		
Α		1.20		
A1	0.05	0.15		
b	0.19	0.30		
C	0.09	0.20		
D	7.70	7.90		
Е	6.40	BSC		
E1	4.30	4.50		
е	0.65	BSC		
L	0.50	0.75		
L2	0.25	0.25 BSC		
M	0°	8°		

GENERIC MARKING DIAGRAM*



= Specific Device Code = Assembly Location

= Wafer Lot L Υ = Year W = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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