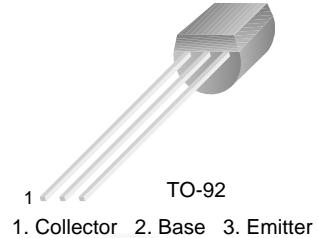


BC556/557/558/559/560

PNP Epitaxial Silicon Transistor

Features

- Switching and Amplifier
- High Voltage: BC556, $V_{CEO} = -65V$
- Low Noise: BC559, BC560
- Complement to BC546 ... BC 550



Absolute Maximum Ratings $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage : BC556 : BC557/560 : BC558/559	-80 -50 -30	V
V_{CEO}	Collector-Emitter Voltage : BC556 : BC557/560 : BC558/559	-65 -45 -30	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current (DC)	-100	mA
P_C	Collector Power Dissipation	500	mW
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-65 ~ 150	$^\circ\text{C}$

Electrical Characteristics $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{CBO}	Collector Cut-off Current	$V_{CB} = -30V, I_E = 0$			-15	nA
h_{FE}	DC Current Gain	$V_{CE} = -5V, I_C = 2\text{mA}$	110		800	
$V_{CE(\text{sat})}$	Collector-Emitter Saturation Voltage	$I_C = -10\text{mA}, I_B = -0.5\text{mA}$ $I_C = -100\text{mA}, I_B = -5\text{mA}$		-90 -250	-300 -650	mV mV
$V_{BE(\text{sat})}$	Collector-Base Saturation Voltage	$I_C = -10\text{mA}, I_B = -0.5\text{mA}$ $I_C = -100\text{mA}, I_B = -5\text{mA}$		-700 -900		mV mV
$V_{BE(\text{on})}$	Base-Emitter On Voltage	$V_{CE} = -5V, I_C = -2\text{mA}$ $V_{CE} = -5V, I_C = -10\text{mA}$	-600	-660	-750 -800	mV mV
f_T	Current Gain Bandwidth Product	$V_{CE} = -5V, I_C = -10\text{mA}, f = 10\text{MHz}$		150		MHz
C_{ob}	Output Capacitance	$V_{CB} = -10V, I_E = 0, f = 1\text{MHz}$			6	pF
NF	Noise Figure : BC556/557/558 : BC559/560 : BC559 : BC560	$V_{CE} = -5V, I_C = -200\mu\text{A}$ $f = 1\text{kHz}, R_G = 2\text{K}\Omega$ $V_{CE} = -5V, I_C = -200\mu\text{A}$ $R_G = 2\text{K}\Omega, f = 30\text{~}15000\text{MHz}$		2 1 1.2 1.2	10 4 4 2	dB dB dB dB

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

Typical Performance Characteristics

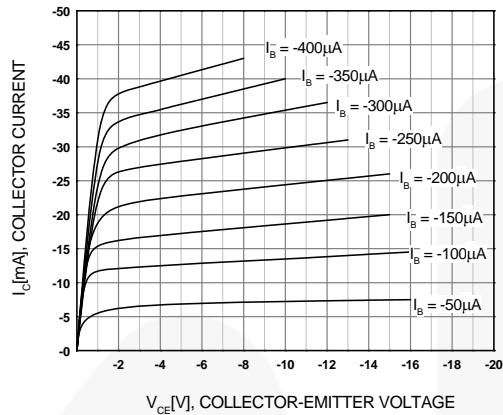


Figure 1. Static Characteristic

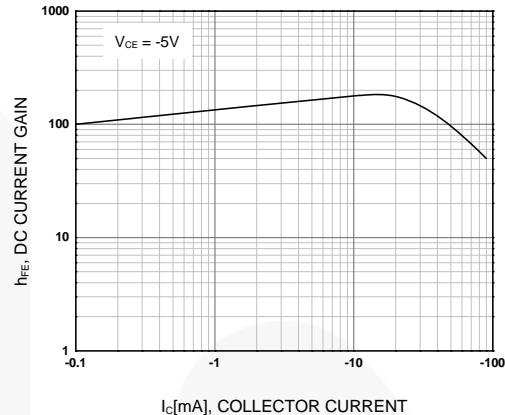


Figure 2. DC current Gain

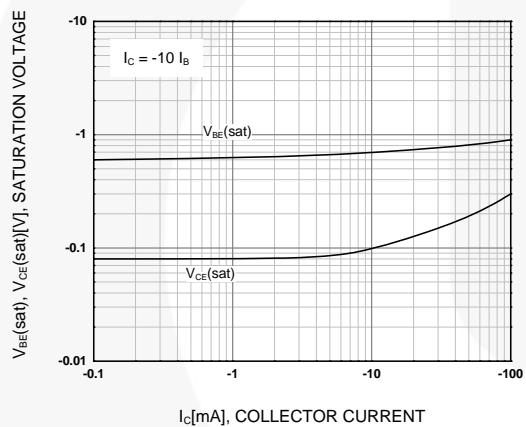


Figure 3. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

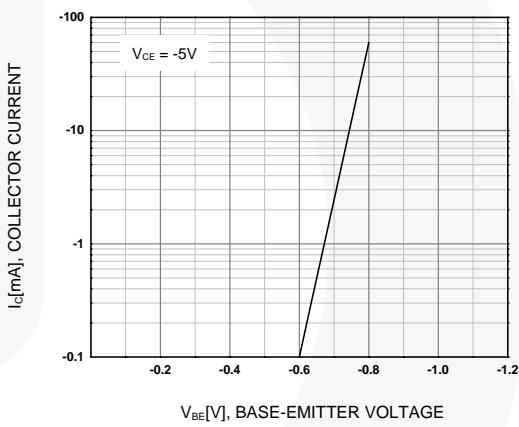


Figure 4. Base-Emitter On Voltage

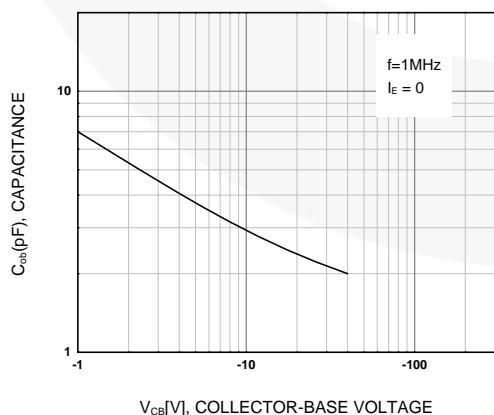


Figure 5. Collector Output Capacitance

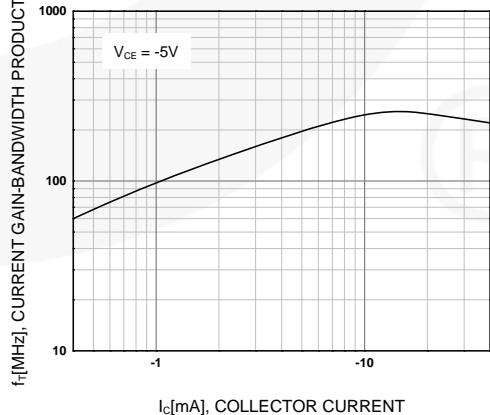
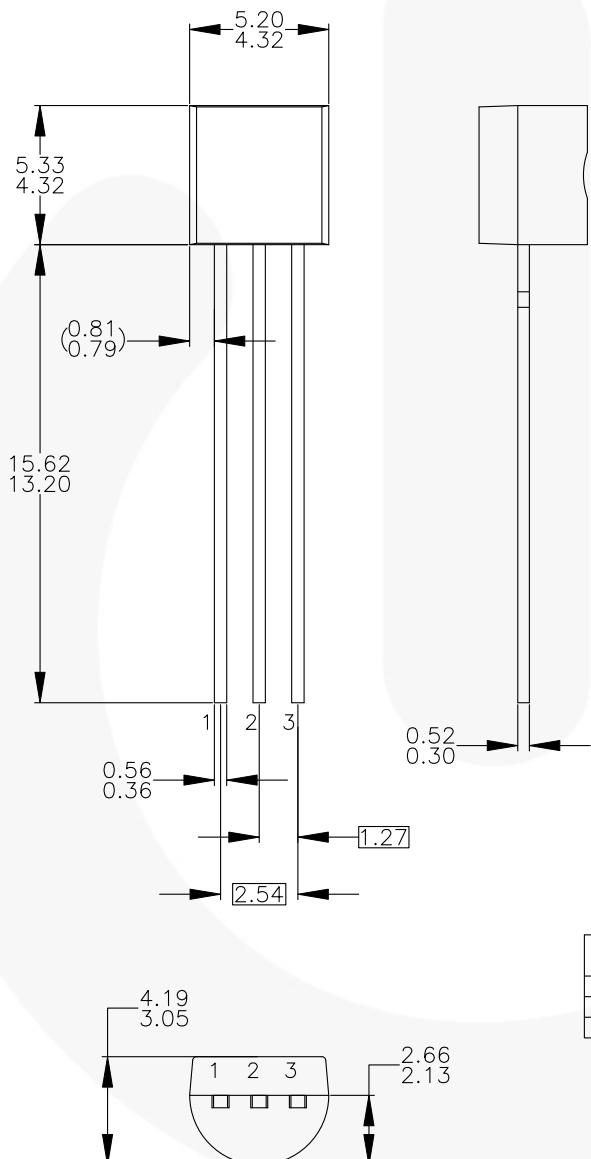


Figure 6. Current Gain Bandwidth Product

Physical Dimensions

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

Pin	92				94				96				97				98			
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M	P	F	M		
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D					
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S					
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G					

LEGEND:

P — BIPOLAR E — Emitter D — Drain
 F — JFET B — Base S — Source
 M — DMOS C — Collector G — Gate

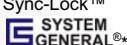
- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Dimensions in Millimeters



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FETBench™			
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