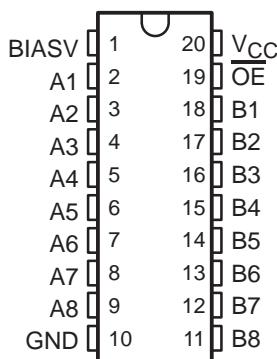
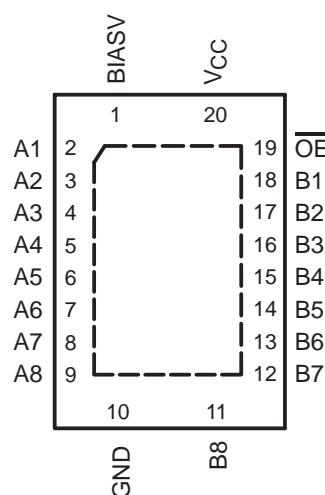


- Undershoot Protection for Off-Isolation on A and B Ports Up To -2 V
- B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging
- Supports PCI Hot Plug
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 3 \Omega$ Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 5.5 \text{ pF}$ Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 3 \mu\text{A}$ Max)
- V_{CC} Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CBT6845C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT6845C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description/ordering information (continued)

The SN74CBT6845C is an 8-bit bus switch with a single output-enable (\overline{OE}) input. When \overline{OE} is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-k Ω resistor when \overline{OE} is high, or if the device is powered down ($V_{CC} = 0$ V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

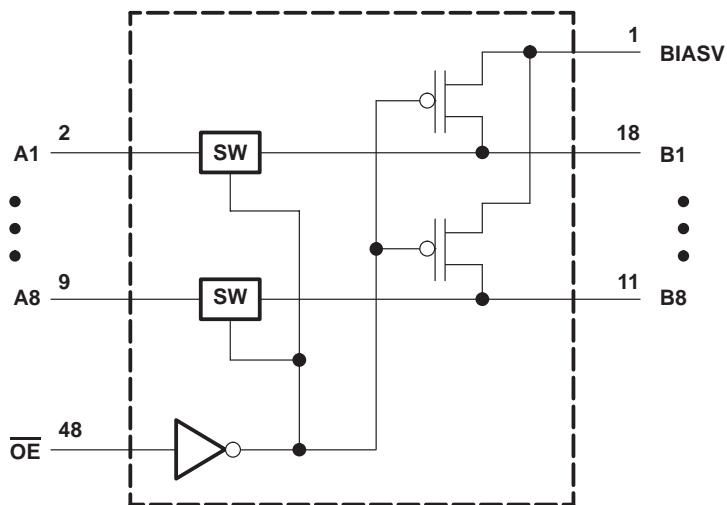
T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT6845CRGYR	CT6845C
	SOIC – DW	Tube	SN74CBT6845CDW	CBT6845C
		Tape and reel	SN74CBT6845CDWR	
	SSOP – DB	Tube	SN74CBT6845CDB	CT6845C
		Tape and reel	SN74CBT6845CDBR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT6845CDBQR	CBT6845C
	TSSOP – PW	Tube	SN74CBT6845CPW	CT6845C
		Tape and reel	SN74CBT6845CPWR	
	TVSOP – DGV	Tape and reel	SN74CBT6845CDGVR	CT6845C

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

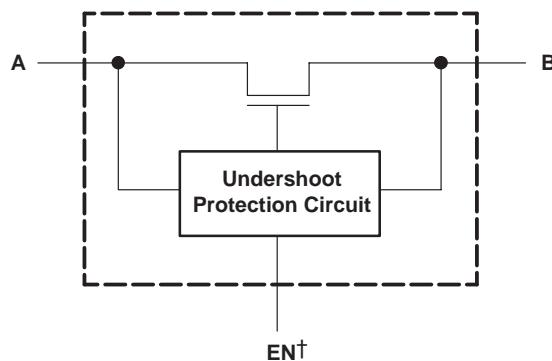
FUNCTION TABLE

INPUT \overline{OE}	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

SN74CBT6845C

8-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS140 – OCTOBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.

1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
BIASV	Bias supply voltage	0	V _{CC}	V
V _{IH}	High-level control input voltage	2	5.5	V
V _{IL}	Low-level control input voltage	0	0.8	V
V _{I/O}	Data input/output voltage	0	5.5	V
T _A	Operating free-air temperature	-40	85	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

SN74CBT6845C
8-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION
SCDS140 – OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$					-1.8	V
V_{IKU}	Data inputs	$V_{CC} = 5 \text{ V}$, $0 \text{ mA} > I_I \geq -50 \text{ mA}$, $V_{IN} = V_{CC}$ or GND, Switch OFF					-2	V
$V_{O(USP)}^{\ddagger}$		$V_{CC} = \text{BIASV} = 5 \text{ V}$, $I_I = -10 \text{ mA}$, $V_{IN} = V_{CC}$ or GND, Switch OFF			3			V
V_O	B port	$V_{CC} = 0 \text{ V}$, $\text{BIASV} = V_x$, $I_O = 0$			V_x	-0.1	V_x	V
I_{IN}	Control inputs	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = V_{CC}$ or GND					± 1	μA
I_O	B port	$V_{CC} = 4.5 \text{ V}$, $\text{BIASV} = 2.4 \text{ V}$, $V_O = 0$, $V_{IN} = V_{CC}$ or GND			0.25			mA
$I_{OZ}^{\$}$		$V_{CC} = 5.5 \text{ V}$, $V_O = 0$ to 5.5 V , $V_I = 0$, $V_{IN} = V_{CC}$ or GND					± 10	μA
I_{off}		$V_{CC} = 0$, $V_O = 0$ to 5.5 V , $V_I = 0$			10			μA
I_{CC}		$V_{CC} = 5.5 \text{ V}$, $I_{I/O} = 0$, $V_{IN} = V_{CC}$ or GND, Switch ON or OFF			3			μA
$\Delta I_{CC}^{\parallel}$	Control inputs	$V_{CC} = 5.5 \text{ V}$, One input at 3.4 V , Other inputs at V_{CC} or GND			2.5			mA
C_{in}	Control inputs	$V_{IN} = 3 \text{ V}$ or 0			4			pF
$C_{io(OFF)}$	A port	$V_{I/O} = 3 \text{ V}$ or 0, Switch OFF, $V_{IN} = V_{CC}$ or GND			5.5			pF
$C_{io(ON)}$		$V_{I/O} = 3 \text{ V}$ or 0, Switch ON, $V_{IN} = V_{CC}$ or GND			13.5			pF
$r_{on}^{\#}$	$V_{CC} = 4 \text{ V}$, TYP at $V_{CC} = 4 \text{ V}$		$V_I = 2.4 \text{ V}$, $I_O = -15 \text{ mA}$		8	12		Ω
	$V_{CC} = 4.5 \text{ V}$		$V_I = 0$	$I_O = 64 \text{ mA}$	3	6		
				$I_O = 30 \text{ mA}$	3	6		
			$V_I = 2.4 \text{ V}$	$I_O = -15 \text{ mA}$	5	10		

V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

† All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ $V_{O(USP)}$ = A-port undershoot static protection.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

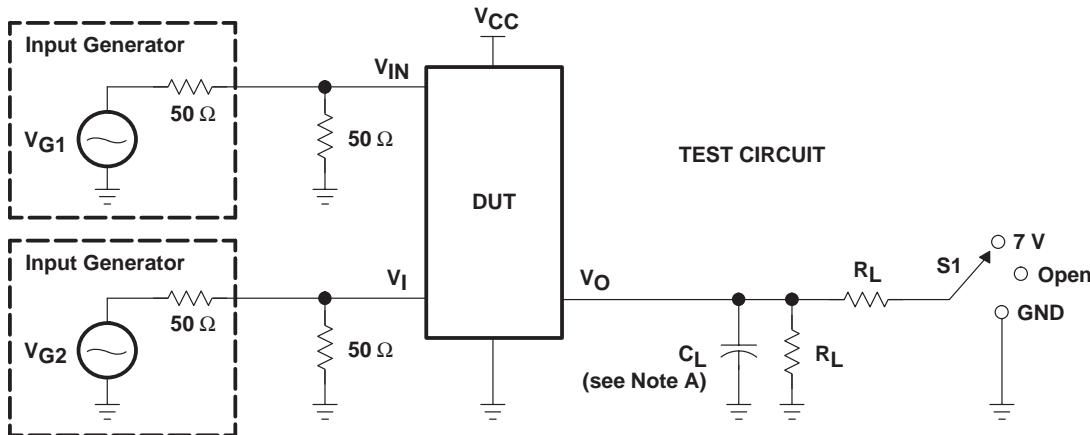
Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

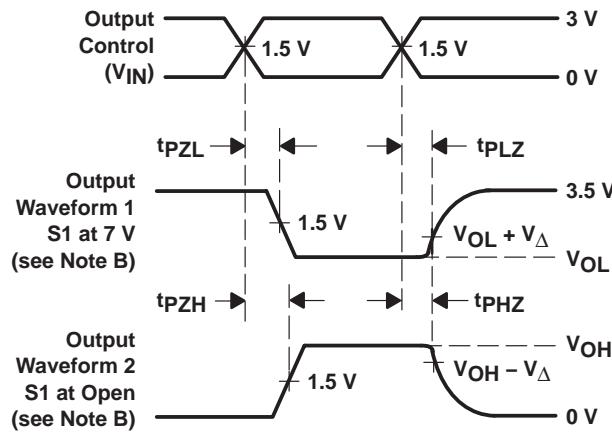
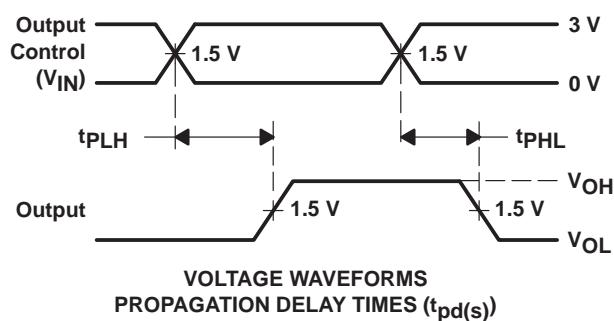
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}^{\parallel}		A or B	B or A	0.24		0.15		ns
t_{PZH}	BIASV = GND	\overline{OE}	A or B	5.2	1.5	4.8		ns
t_{PZL}	BIASV = 3 V			5.2	1.5	4.8		
t_{PHZ}	BIASV = GND	\overline{OE}	A or B	4.9	1.5	5.3		ns
t_{PLZ}	BIASV = 3 V			4.9	1.5	5.3		

|| The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	$S1$	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	$5 \text{ V} \pm 0.5 \text{ V}$ 4 V	Open Open	500Ω 500Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	$5 \text{ V} \pm 0.5 \text{ V}$ 4 V	7 V 7 V	500Ω 500Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	$5 \text{ V} \pm 0.5 \text{ V}$ 4 V	Open Open	500Ω 500Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- All parameters and waveforms are not applicable to all devices.

Figure 1. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT6845CDBQRE4	ACTIVE	SSOP	DBQ	20		TBD	Call TI	Call TI	-40 to 85	CBT6845C	Samples
SN74CBT6845CDBQRG4	ACTIVE	SSOP	DBQ	20		TBD	Call TI	Call TI	-40 to 85	CBT6845C	Samples
SN74CBT6845CDBRE4	ACTIVE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85	CT6845C	Samples
SN74CBT6845CDBRG4	ACTIVE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85	CT6845C	Samples
SN74CBT6845CDGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CDGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CDGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT6845C	Samples
SN74CBT6845CDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT6845C	Samples
SN74CBT6845CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT6845C	Samples
SN74CBT6845CDWRE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	CBT6845C	Samples
SN74CBT6845CDWRG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	CBT6845C	Samples
SN74CBT6845CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CPWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples
SN74CBT6845CPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6845C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT6845CRGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CT6845C	Samples
SN74CBT6845CRGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CT6845C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

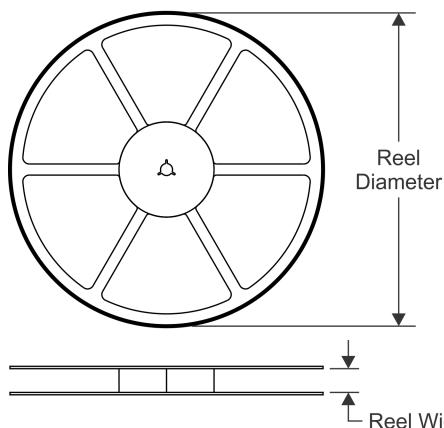
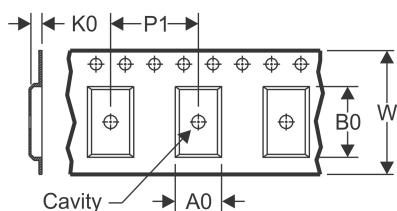
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

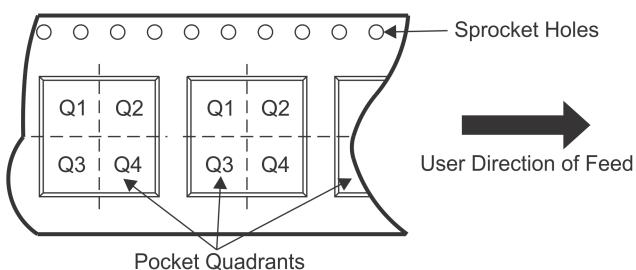
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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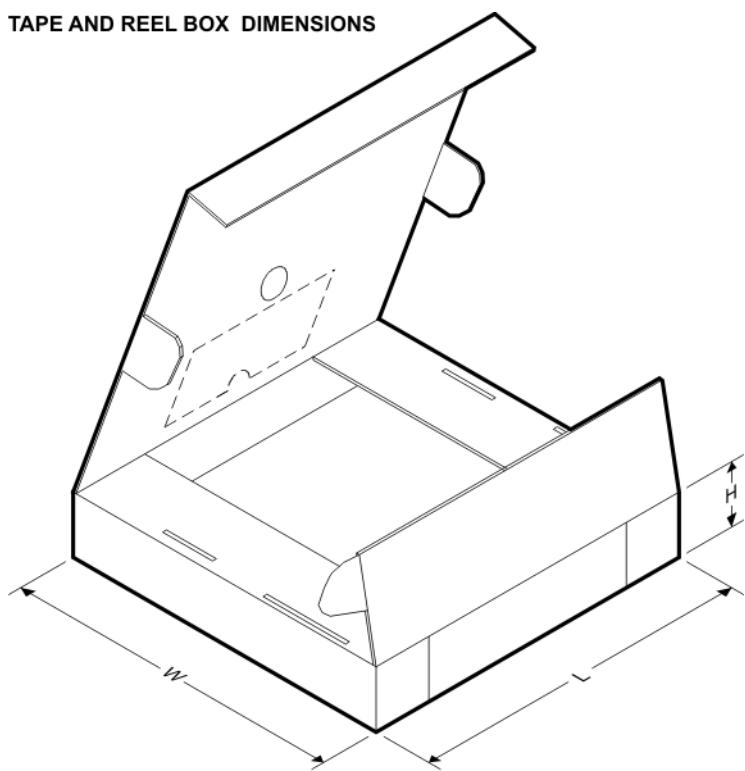
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT6845CDGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT6845CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74CBT6845CRGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


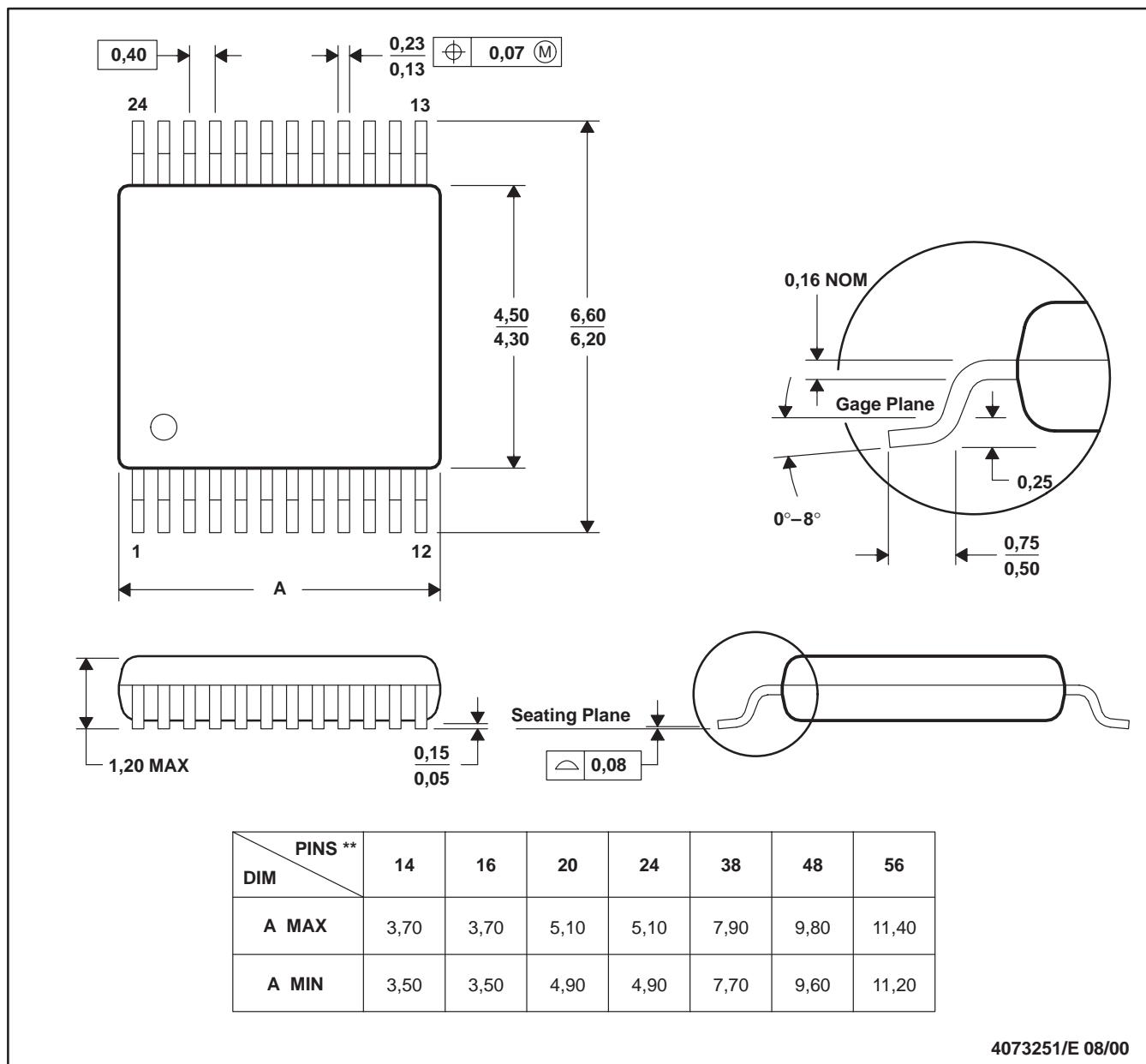
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT6845CDGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CBT6845CPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74CBT6845CRGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

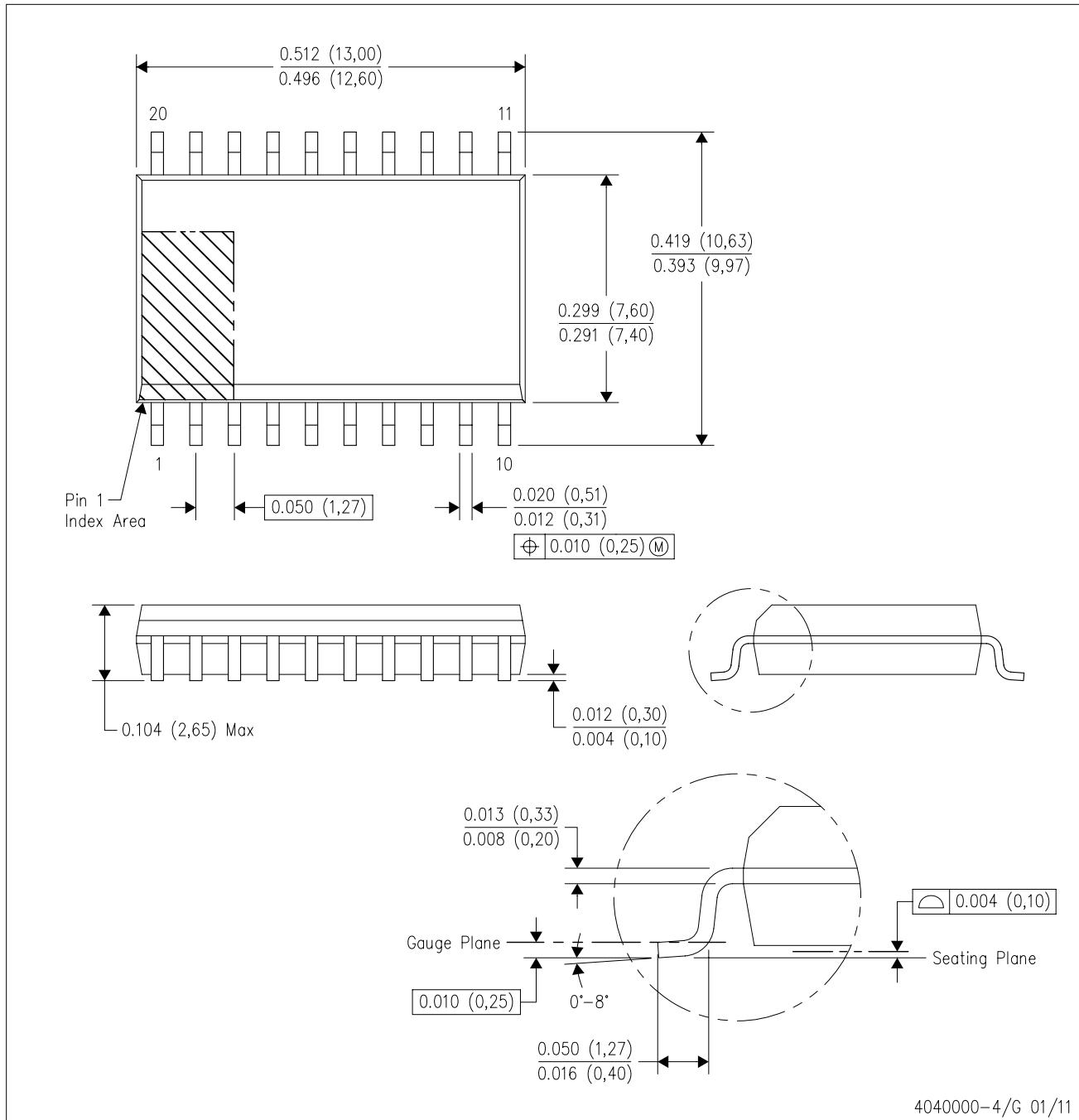
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

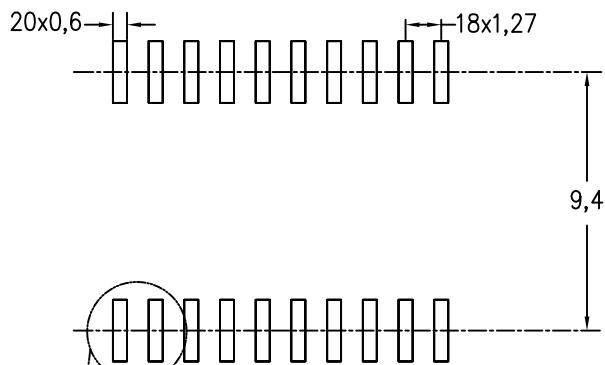
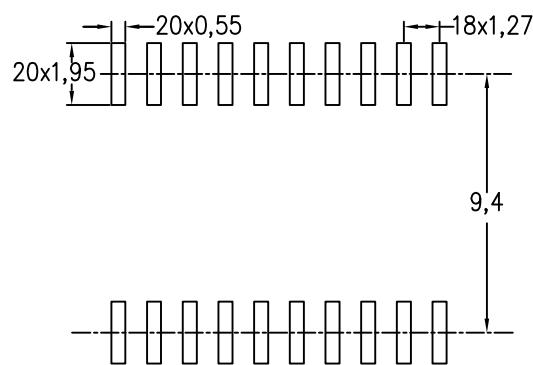


NOTES:

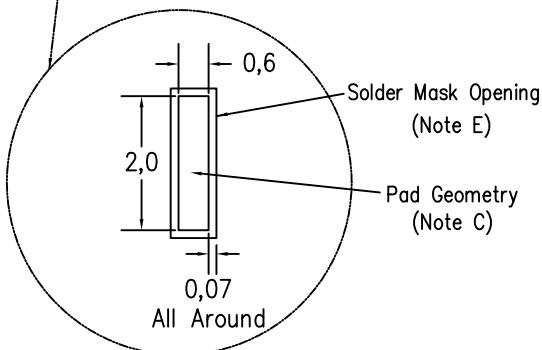
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)

Non Solder Mask Define Pad



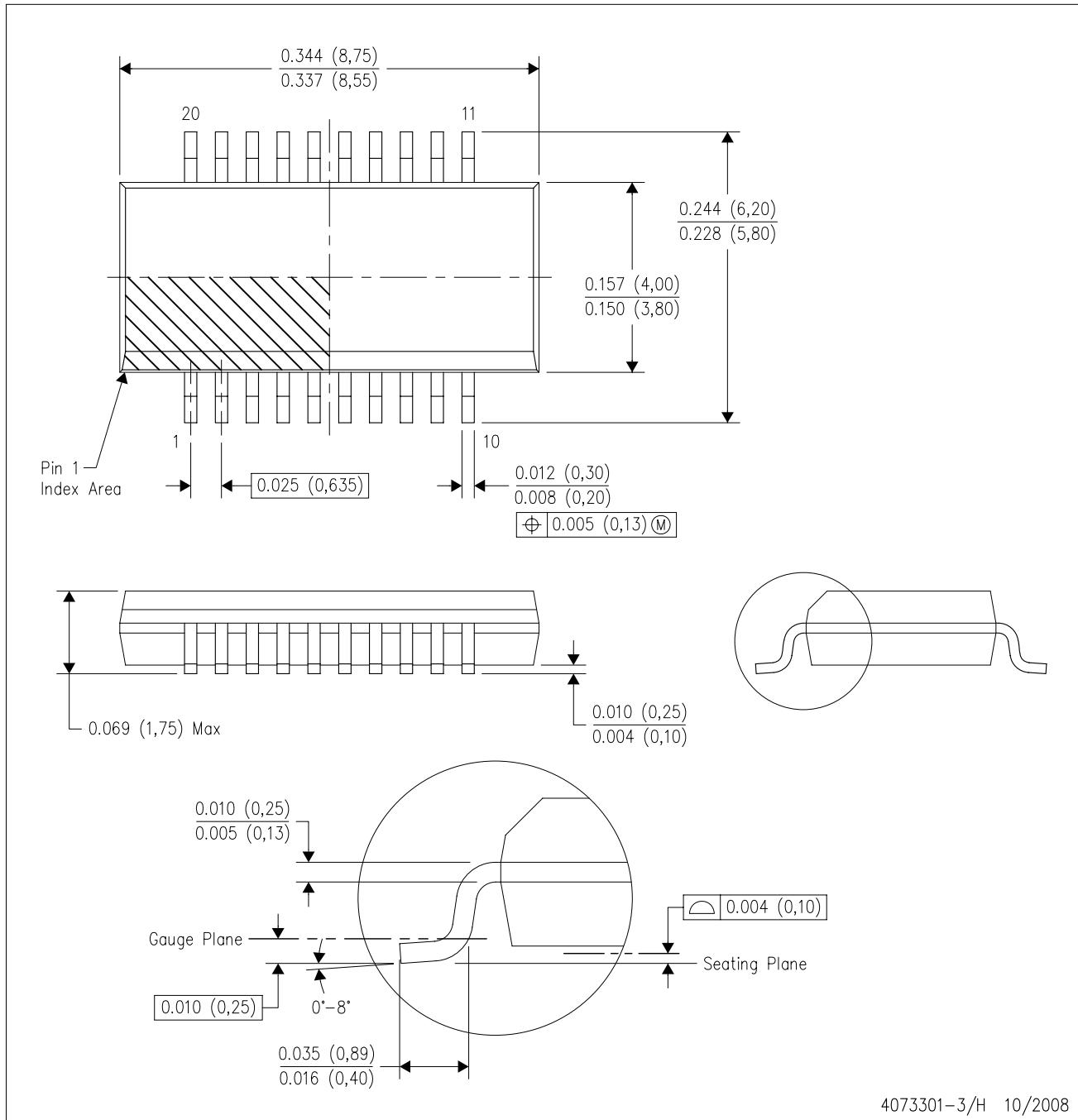
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NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

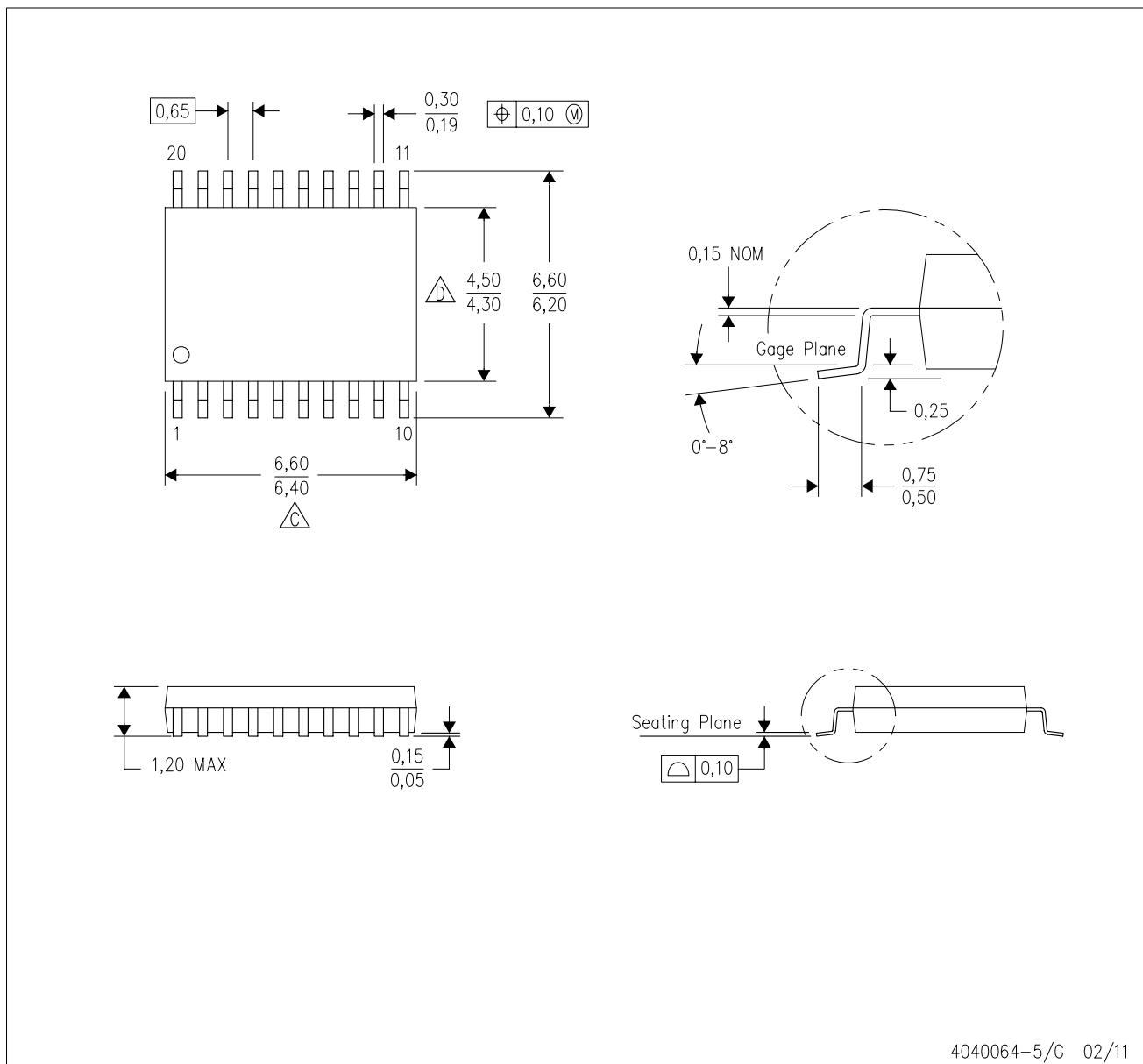


NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- Falls within JEDEC MO-137 variation AD.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

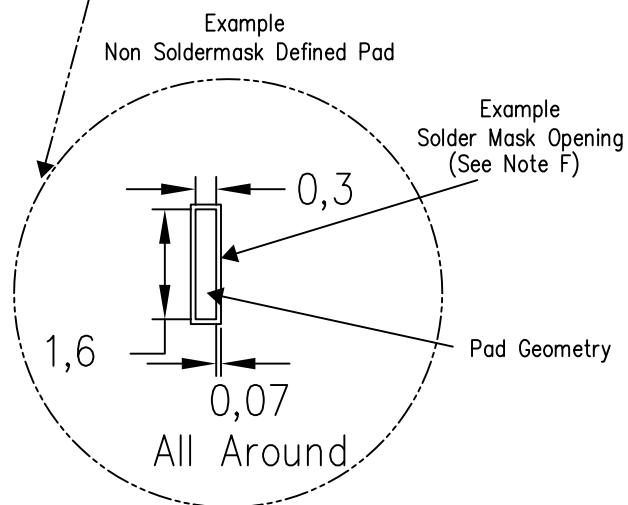
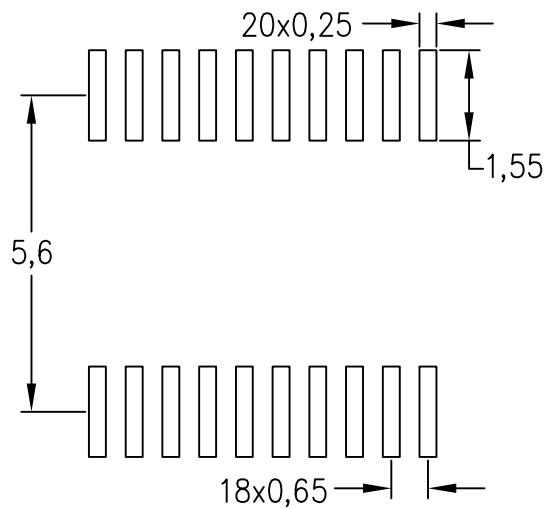
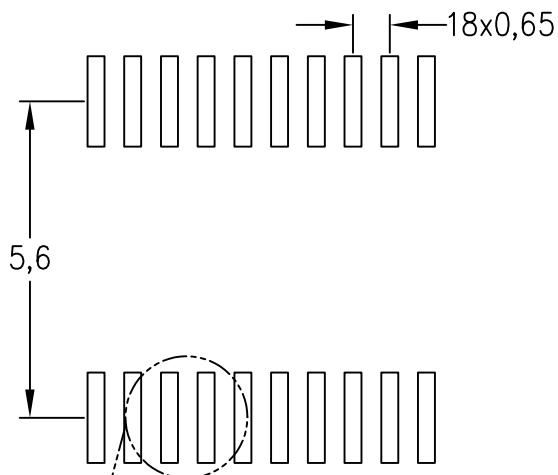
4040064-5/G 02/11

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).



4211284-5/F 12/12

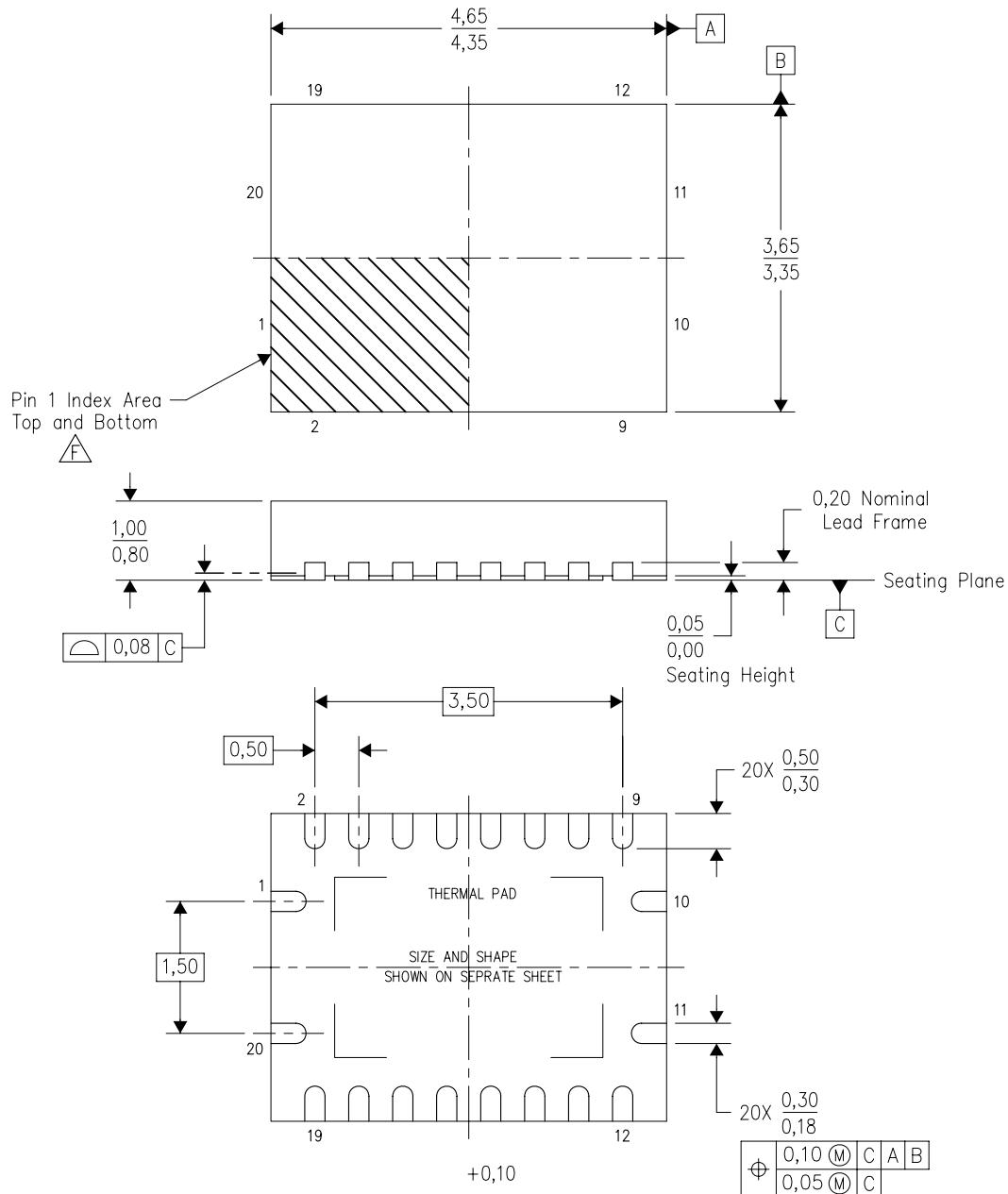
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-4/l 06/2011

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC M0-241 variation BA.

THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N20)

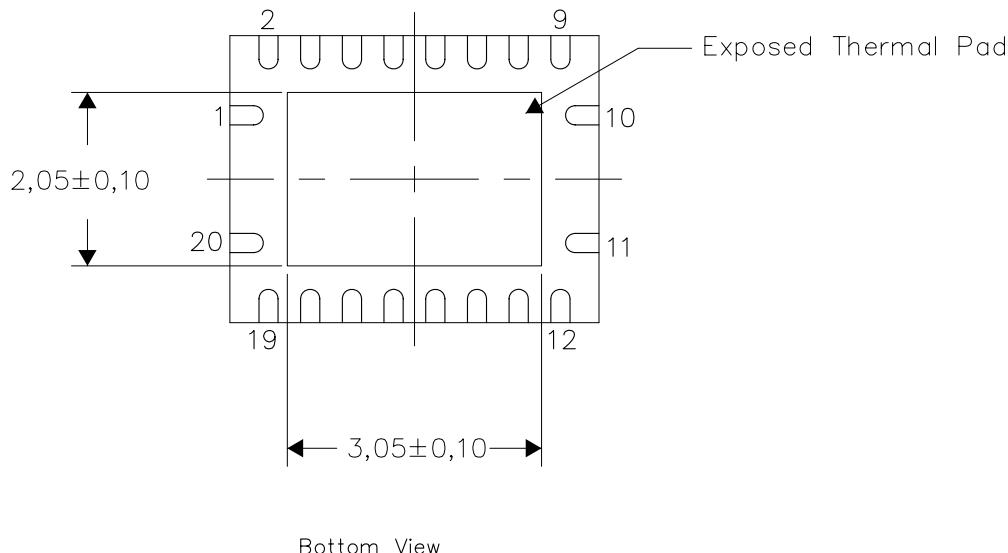
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



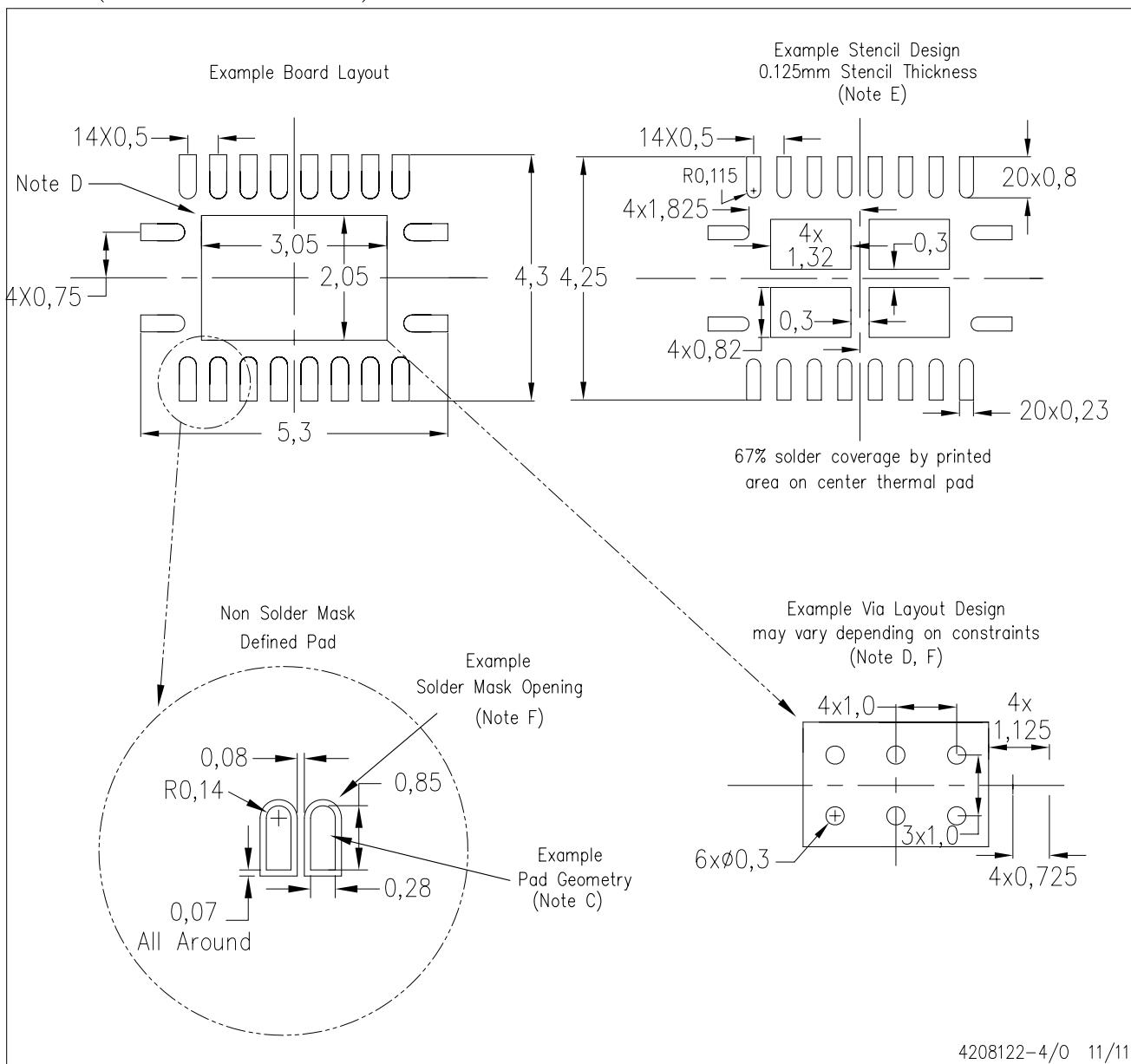
Exposed Thermal Pad Dimensions

4206353-4/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



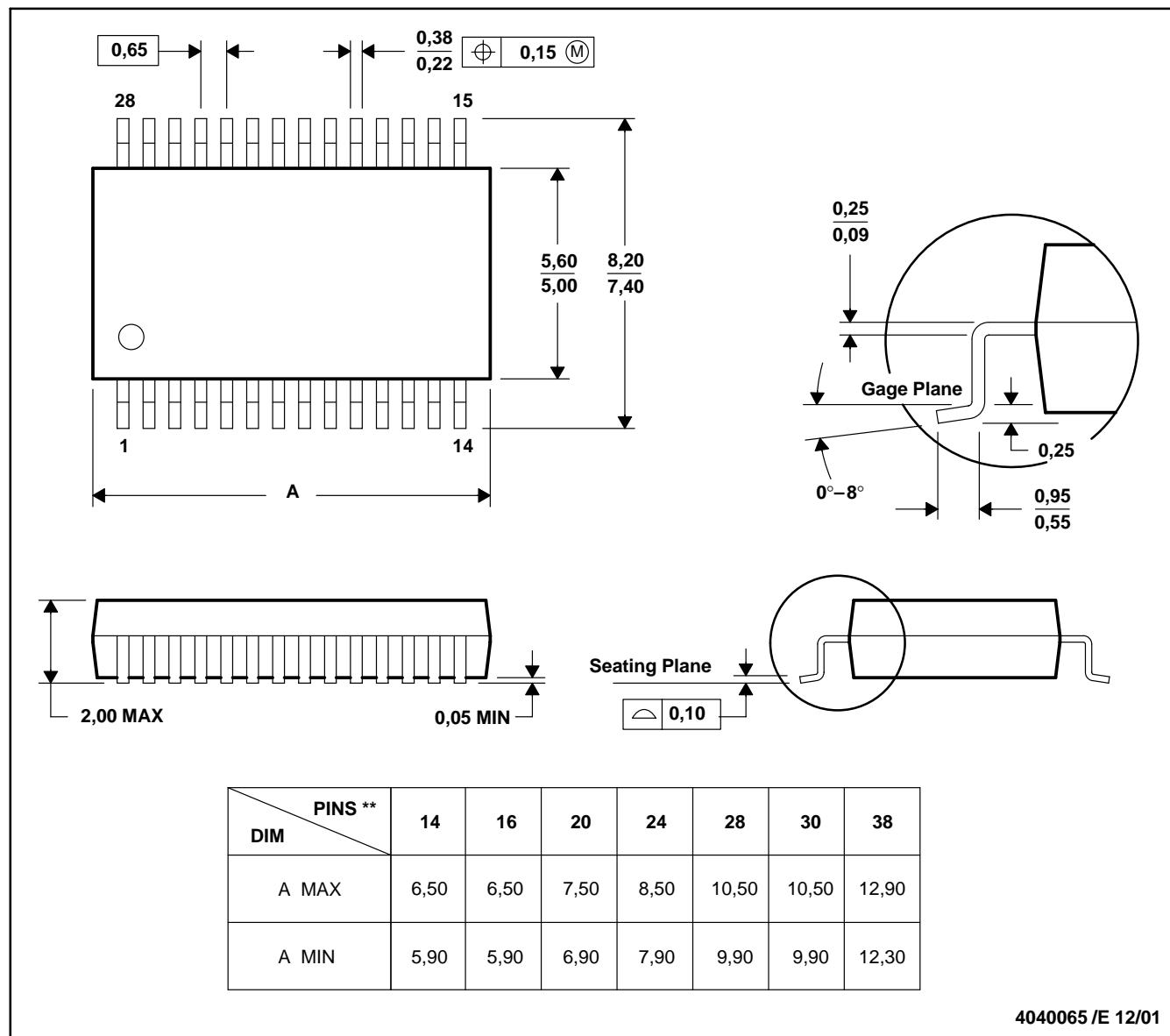
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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