BT169D-L

SCR

20 March 2014 Product data sheet

1. General description

Planar passivated very sensitive gate Silicon Controlled Rectifier in a SOT54 (TO-92) plastic package.

2. Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Very sensitive gate

3. Applications

- Ignition circuits
- Low power latching circuits
- Protection / shut-down circuits: lighting ballasts
- Protection / shut-down circuits: Switched Mode Power Supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	400	V
V_{RRM}	repetitive peak reverse voltage			-	-	400	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	8	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq$ 83 °C; Fig. 2; Fig. 3		-	-	0.8	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 7		-	-	50	µA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	0.4	1	mA
I_L	latching current	V_D = 12 V; I_G = 0.5 mA; T_j = 25 °C; Fig. 8		-	2	4	mA

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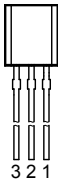
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 TO-92 (SOT54)	
2	G	gate		
3	K	cathode		

6. Ordering information

Table 3. Ordering information

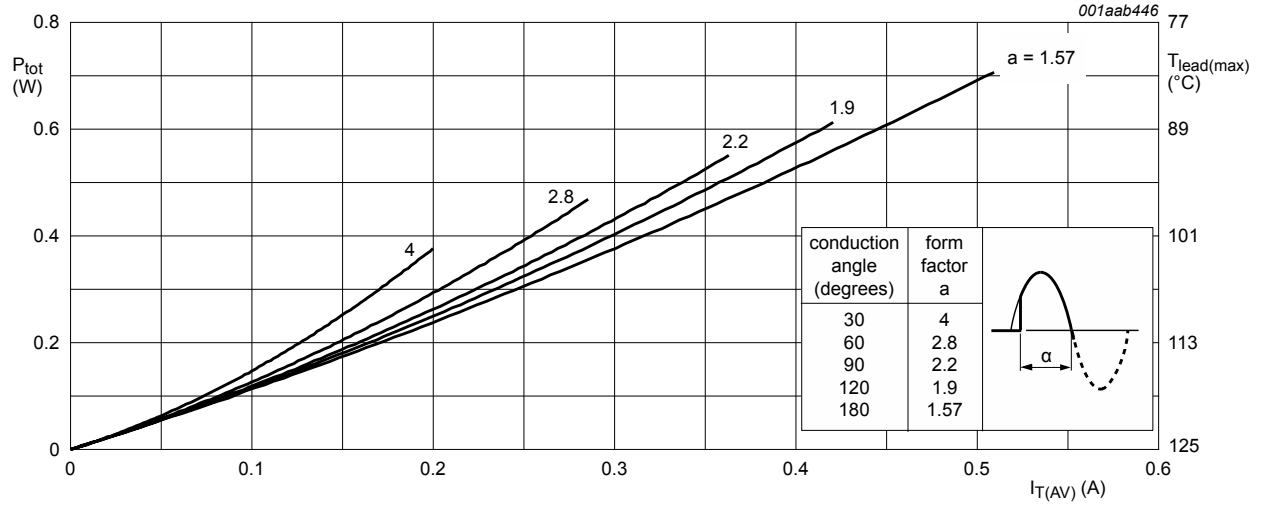
Type number	Package		
	Name	Description	Version
BT169D-L	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

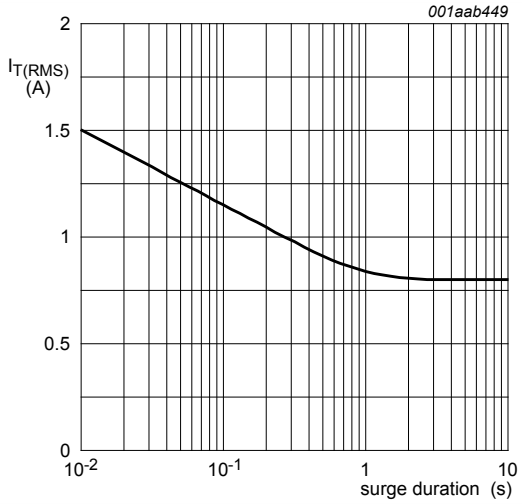
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	400	V
V_{RRM}	repetitive peak reverse voltage			-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83$ °C; Fig. 1		-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83$ °C; Fig. 2; Fig. 3		-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	9	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	8	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	0.32	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 2$ A; $I_G = 10$ mA; $dI_G/dt = 100$ mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C



α = conduction angle

a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz; T_{lead} = 83 °C

Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

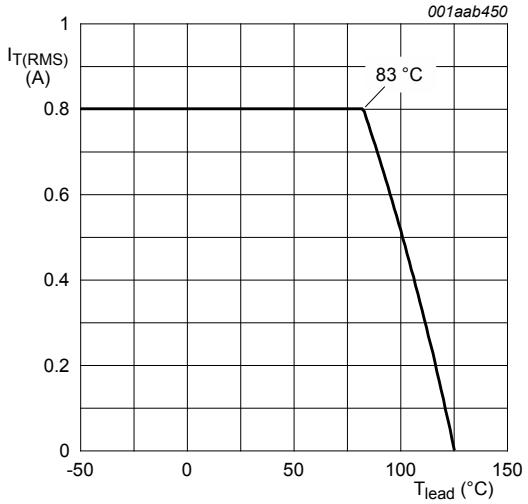
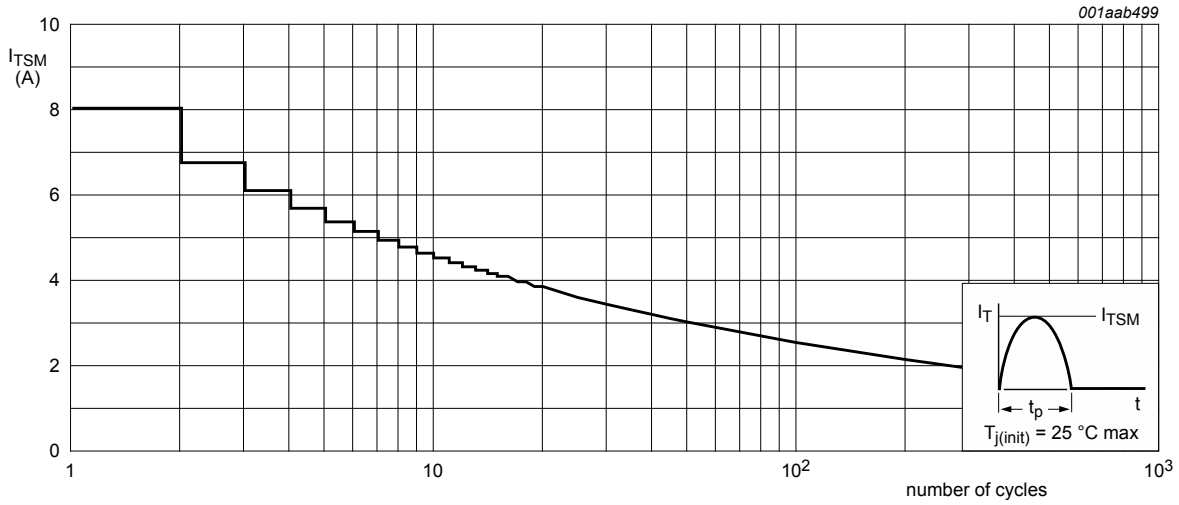


Fig. 3. RMS on-state current as a function of lead temperature; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

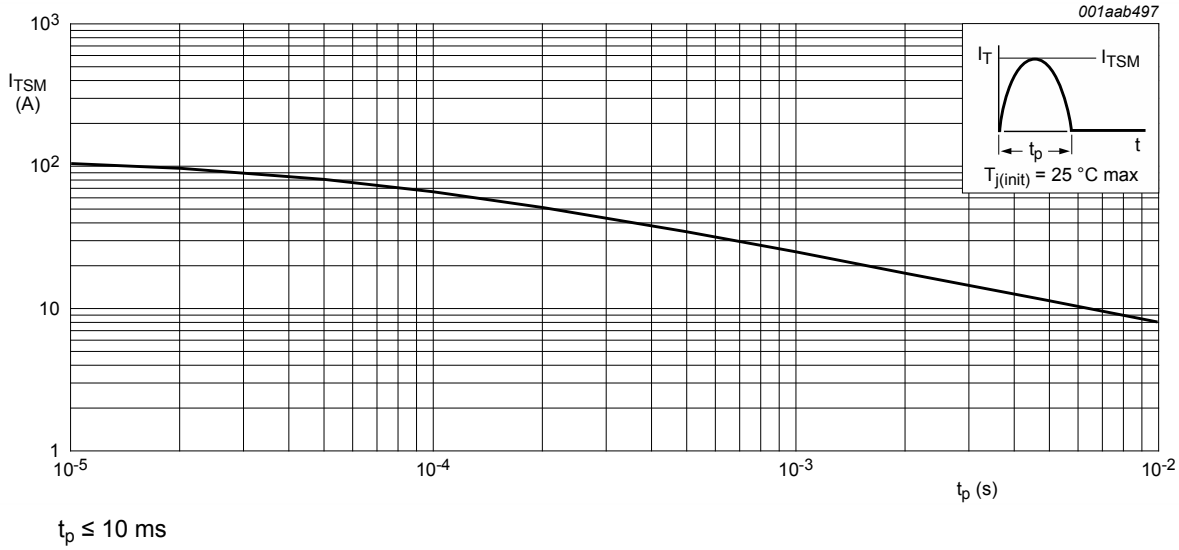


Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	Fig. 6		-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm		-	150	-	K/W

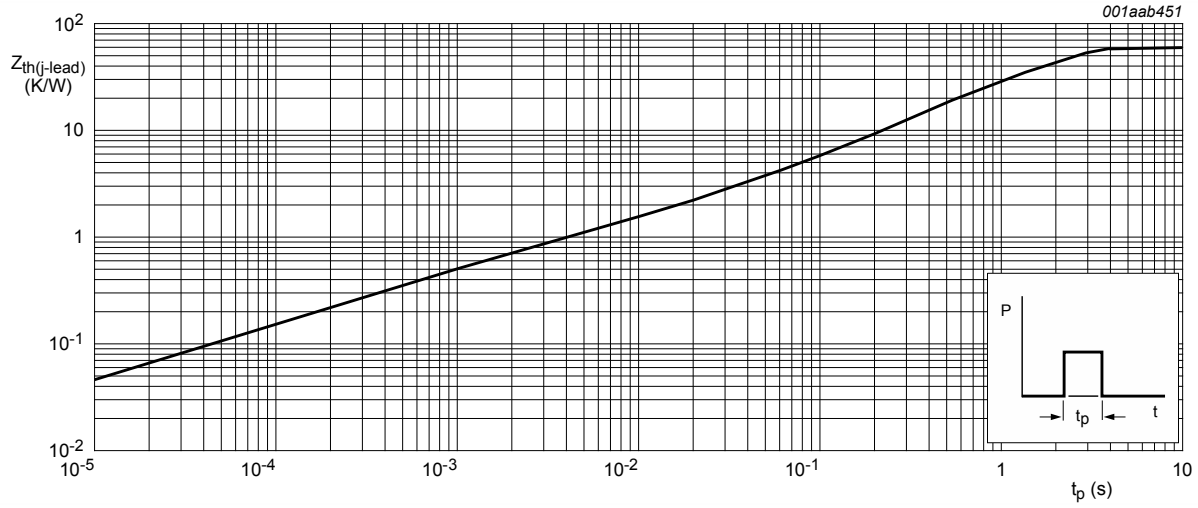


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 7		-	-	50	µA
I_L	latching current	V_D = 12 V; I_G = 0.5 mA; T_j = 25 °C; Fig. 8		-	2	4	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	0.4	1	mA
V_T	on-state voltage	I_T = 1.2 A; T_j = 25 °C; Fig. 10		-	1.25	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 11		-	0.5	0.8	V
		V_D = 12 V; I_T = 10 mA; T_j = 125 °C; Fig. 11		0.2	0.3	-	V
I_D	off-state current	V_D = 400 V; T_j = 25 °C; R_{GK} = 1 kΩ		-	-	2	µA
		V_D = 400 V; T_j = 125 °C; R_{GK} = 1 kΩ		-	0.05	0.1	mA
I_R	reverse current	V_R = 400 V; T_j = 25 °C; R_{GK} = 1 kΩ		-	0.05	2	µA
		V_R = 400 V; T_j = 125 °C; R_{GK} = 1 kΩ		-	0.05	0.1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 268 V; T_j = 125 °C; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		500	800	-	V/µs
		V_{DM} = 268 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	25	-	V/µs

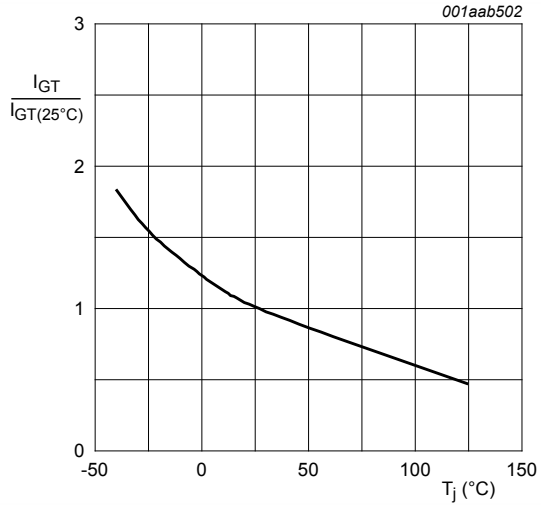


Fig. 7. Normalized gate trigger current as a function of junction temperature

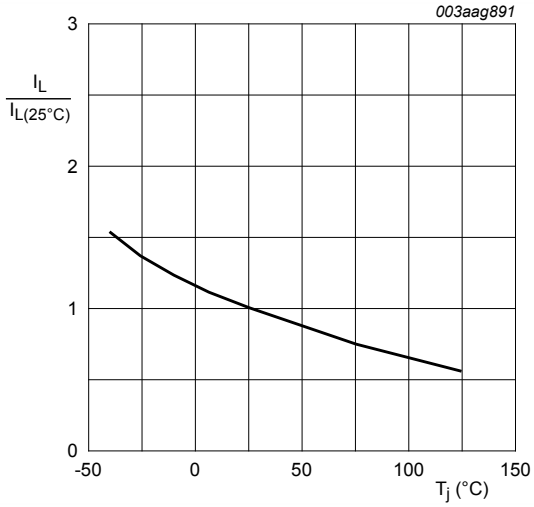


Fig. 8. Normalized latching current as a function of junction temperature

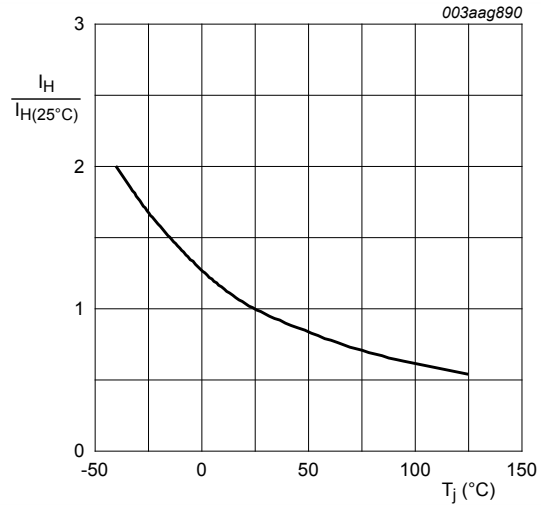
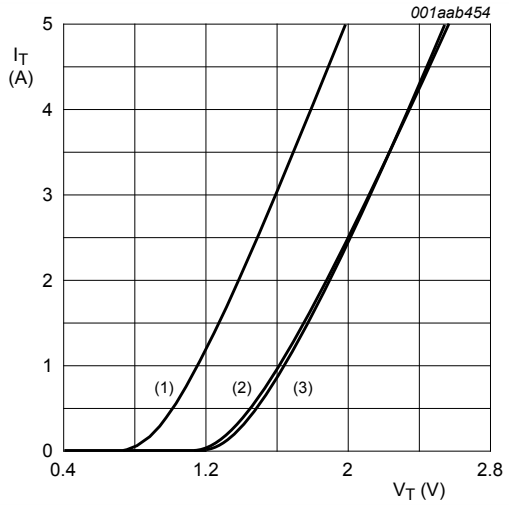


Fig. 9. Normalized holding current as a function of junction temperature



Vo = 1.067 V; Rs = 0.187 Ω
(1) Tj = 125 °C; typical values
(2) Tj = 125 °C; maximum values
(3) Tj = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

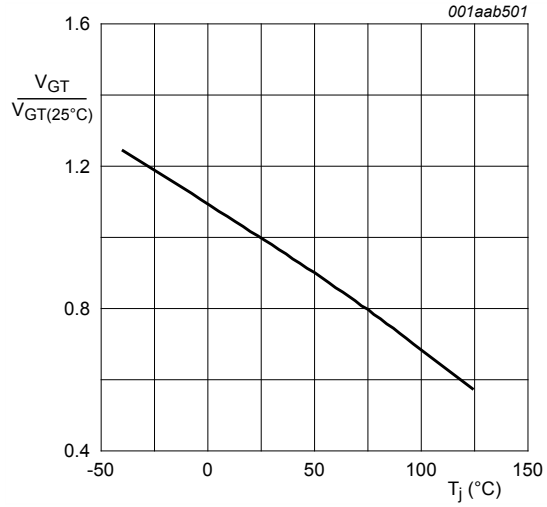
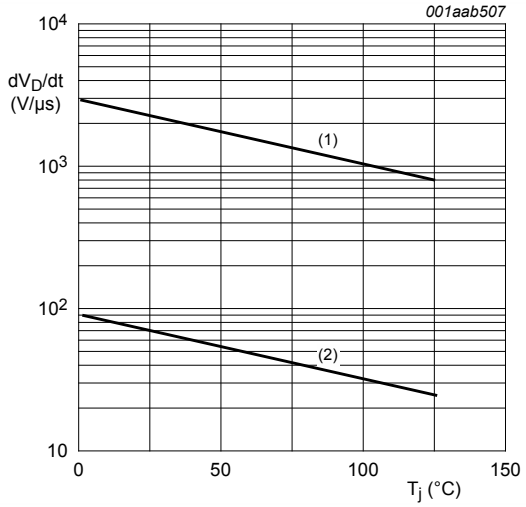


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



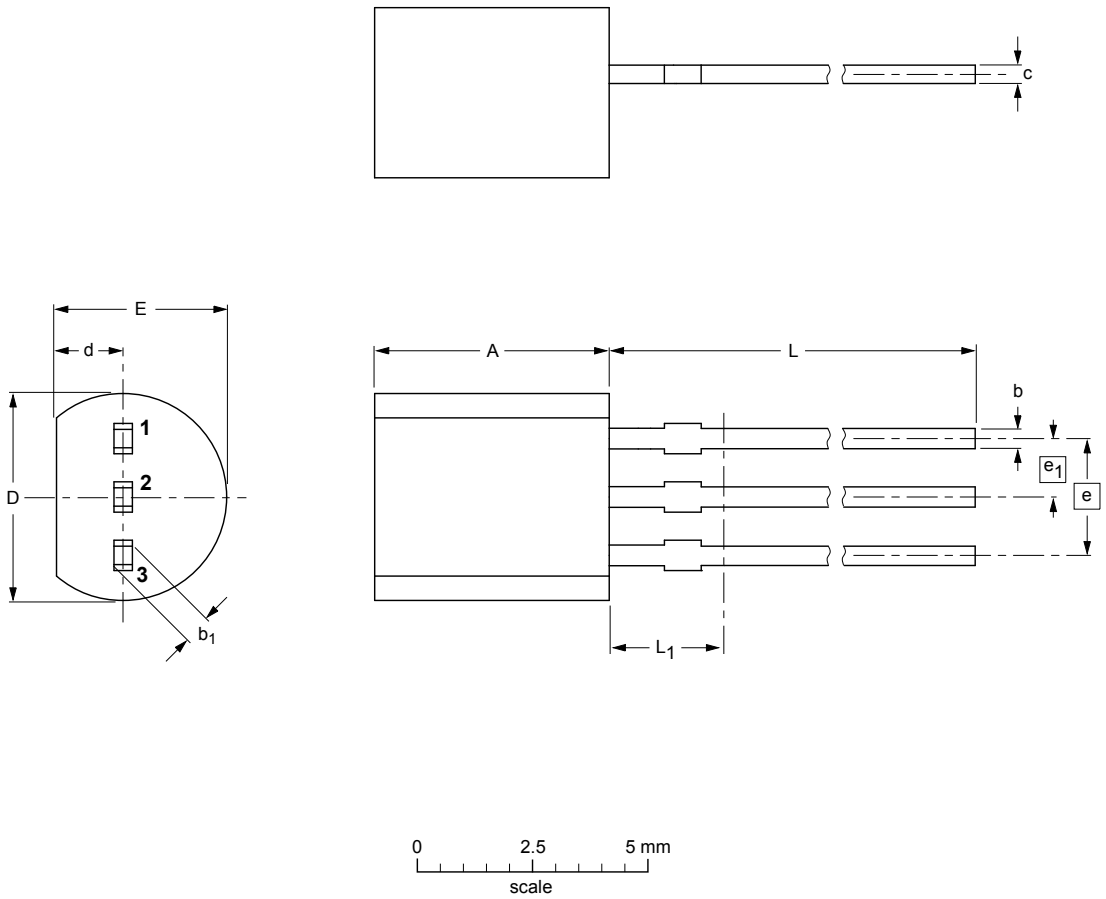
(1) R_{GK} = 1 kΩ

(2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig. 13. Package outline TO-92 (SOT54)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 20 March 2014