# TEXAS INSTRUMENTS

**CY74FCT2827T**

## 10-Bit Buffer

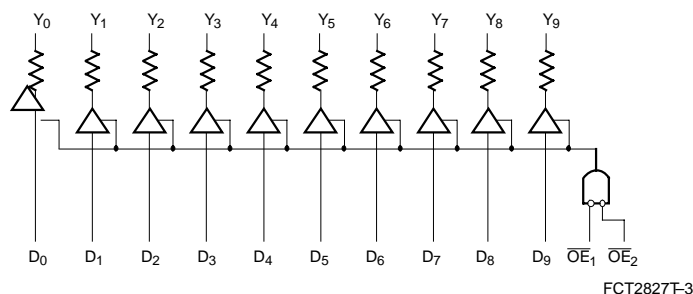SCCS045 - May 1994 - Revised March 2000

## Features

- **Function and pinout compatible with FCT, F, and AM29827 logic**
- **FCT-C speed at 5.0 ns max. (Com'l), FCT-A speed at 8.0 ns max. (Com'l)**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced $V_{OH}$ (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Extended commercial temp. range of –40˚C to +85˚C**
- **Sink current        12 mA**
  **Source current      15 mA**
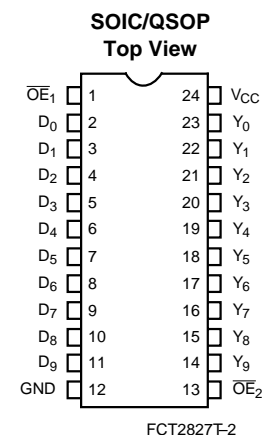
## Functional Description

The FCT2827T 10-bit bus driver provides high-performance bus interface buffering for wide data/address paths or buses carrying parity. This 10-bit buffer has NAND-ed output enables for maximum control flexibility. The FCT2827T is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The FCT2827T can be used to replace the FCT827T to reduce noise in an existing design.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

## Logic Block Diagram



FCT2827T–3

## Pin Configurations

**SOIC/QSOP**
**Top View**

| | | | |
|---|---|---|---|
| $\overline{OE}_1$ | 1 | 24 | $V_{CC}$ |
| $D_0$ | 2 | 23 | $Y_0$ |
| $D_1$ | 3 | 22 | $Y_1$ |
| $D_2$ | 4 | 21 | $Y_2$ |
| $D_3$ | 5 | 20 | $Y_3$ |
| $D_4$ | 6 | 19 | $Y_4$ |
| $D_5$ | 7 | 18 | $Y_5$ |
| $D_6$ | 8 | 17 | $Y_6$ |
| $D_7$ | 9 | 16 | $Y_7$ |
| $D_8$ | 10 | 15 | $Y_8$ |
| $D_9$ | 11 | 14 | $Y_9$ |
| GND | 12 | 13 | $\overline{OE}_2$ |

FCT2827T–2

## Function Table[1]

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | D | Y | Function |
| L | L | L | L | Transparent |
| L | L | H | H | |
| H | X | X | Z | Three-State |
| X | H | X | Z | |

**Note:**
1.   H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.

**TEXAS INSTRUMENTS**

## Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ...................................−65°C to +150°C

Ambient Temperature with
Power Applied..............................................−65°C to +135°C

Supply Voltage to Ground Potential ...............−0.5V to +7.0V

DC Input Voltage...........................................−0.5V to +7.0V

DC Output Voltage ........................................−0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ......120 mA

Power Dissipation ............................................................0.5W

Static Discharge Voltage............................................>2001V
(per MIL-STD-883, Method 3015)

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | −40°C to +85°C | 5V ± 5% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −15 mA | 2.4 | 3.3 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 12 mA | | 0.3 | 0.55 | V |
| $R_{OUT}$ | Output Resistance | $V_{CC}$ = Min., $I_{OL}$ = 12 mA | 20 | 25 | 40 | Ω |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $V_H$ | Hysteresis[5] | All inputs | | 0.2 | | V |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = −18 mA | | −0.7 | −1.2 | V |
| $I_I$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ | | | 5 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7V | | | ±1 | μA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.5V | | | ±1 | μA |
| $I_{OZH}$ | Off State HIGH-Level Output Current | $V_{CC}$ = Max., $V_{OUT}$ = 2.7V | | | 10 | μA |
| $I_{OZL}$ | Off State LOW-Level Output Current | $V_{CC}$ = Max., $V_{OUT}$ = 0.5V | | | −10 | μA |
| $I_{OS}$ | Output Short Circuit Current[6] | $V_{CC}$ = Max., $V_{OUT}$ = 0.0V | −60 | −120 | −225 | mA |
| $I_{OFF}$ | Power-Off Disable | $V_{CC}$ = 0V, $V_{OUT}$ = 4.5V | | | ±1 | μA |

## Capacitance[5]

| Parameter | Description | Typ.[4] | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | 9 | 12 | pF |

**Notes:**
2.  Unless otherwise noted, these limits are over the operating free-air temperature range.
3.  Unused inputs must always be connected to an appropriate logic voltage level, preferably either $V_{CC}$ or ground.
4.  Typical values are at $V_{CC}$=5.0V, $T_A$=+25˚C ambient.
5.  This parameter is specified but not tested.
6.  Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

## Power Supply Characteristics

| Parameter | Description | Test Conditions | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$=Max., $V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}$-0.2V | 0.1 | 0.2 | mA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current (TTL inputs HIGH) | $V_{CC}$=Max., $V_{IN}$=3.4V,[7] $f_1$=0, Outputs Open | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[8] | $V_{CC}$=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}$-0.2V | 0.06 | 0.12 | mA/ MHz |
| $I_C$ | Total Power Supply Current[9] | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}$-0.2V | 0.7 | 1.4 | mA |
| | | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1$=10 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN}$=3.4V or $V_{IN}$=GND | 1.0 | 2.4 | mA |
| | | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at $f_1$=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}$-0.2V | 1.6 | 3.2[10] | mA |
| | | $V_{CC}$=Max., 50% Duty Cycle, Outputs Open, Ten Bits Toggling at $f_1$=2.5 MHz, $\overline{OE}_1$ or $\overline{OE}_2$=GND, $V_{IN}$=3.4V or $V_{IN}$=GND | 4.1 | 13.2[10] | mA |

**Notes:**
7. Per TTL driven input ($V_{IN}$=3.4V); all other inputs at $V_{CC}$ or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. $I_C$ = $I_{QUIESCENT}$ + $I_{INPUTS}$ + $I_{DYNAMIC}$
   $I_C$ = $I_{CC}$+$\Delta I_{CC}D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
   $I_{CC}$ = Quiescent Current with CMOS input levels
   $\Delta I_{CC}$ = Power Supply Current for a TTL HIGH input
      ($V_{IN}$=3.4V)
   $D_H$ = Duty Cycle for TTL inputs HIGH
   $N_T$ = Number of TTL inputs at $D_H$
   $I_{CCD}$ = Dynamic Current caused by an input transition pair
      (HLH or LHL)
   $f_0$ = Clock frequency for registered devices, otherwise zero
   $f_1$ = Input signal frequency
   $N_1$ = Number of inputs changing at $f_1$
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the $I_{CC}$ formula. These limits are specified but not tested.

## Switching Characteristics Over the Operating Range[11]

| Param. | Description | Test Load | CY74FCT2827AT | | CY74FCT2827CT | | Unit | Fig. No.[12] |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay D to Y | $C_L$=50 pF $R_L$=500Ω | 1.5 | 8.0 | 1.5 | 4.4 | ns | 1, 3 |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay D to Y[5] | $C_L$=300 pF $R_L$=500Ω | 1.5 | 15.0 | 1.5 | 10.0 | ns | 1, 3 |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time $\overline{OE}$ to Y | $C_L$=50 pF $R_L$=500Ω | 1.5 | 12.0 | 1.5 | 7.0 | ns | 1, 7, 8 |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time $\overline{OE}$ to Y[5] | $C_L$=300 pF $R_L$=500Ω | 1.5 | 23.0 | 1.5 | 14.0 | ns | 1, 7, 8 |
| $t_{PHZ}$ $t_{PHL}$ | Output Disable Time $\overline{OE}$ to Y[5] | $C_L$=5 pF $R_L$=500Ω | 1.5 | 9.0 | 1.5 | 5.7 | ns | 1, 7, 8 |
| $t_{PHZ}$ $t_{PHL}$ | Output Disable Time $\overline{OE}$ to Y | $C_L$=50 pF $R_L$=500Ω | 1.5 | 9.0 | 1.5 | 6.0 | ns | 1, 7, 8 |

## Ordering Information

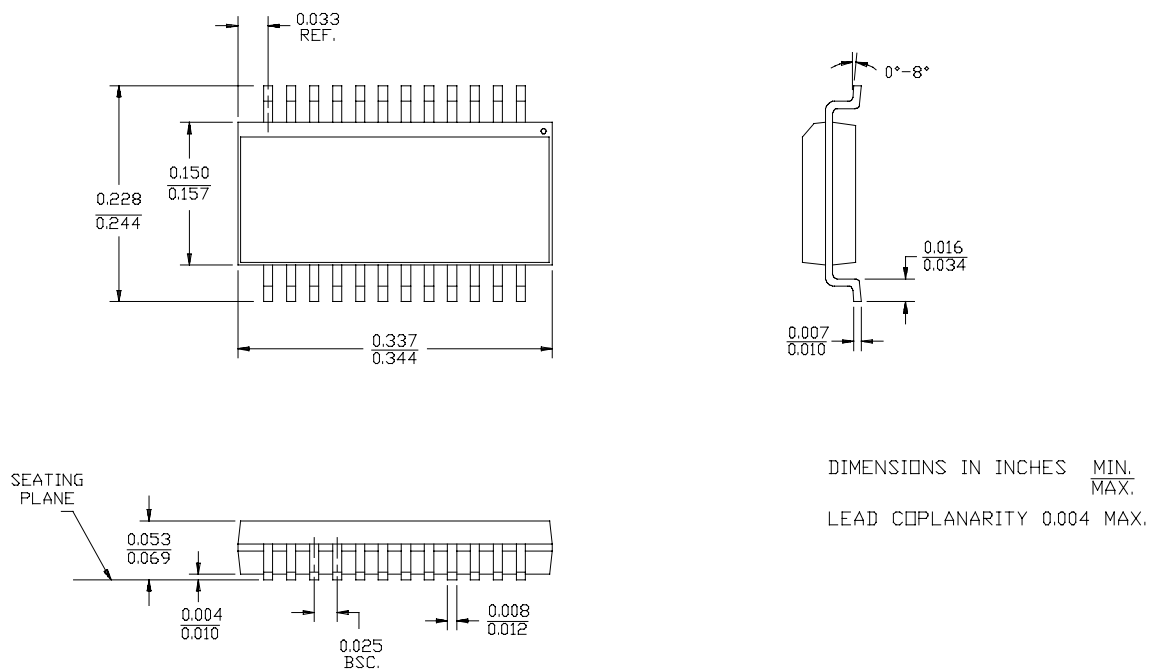| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 4.4 | CY74FCT2827CTQCT | Q13 | 24-Lead (150-Mil) QSOP | Commercial |
| 8.0 | CY74FCT2827ATQCT | Q13 | 24-Lead (150-Mil) QSOP | Commercial |

**Note:**
11. Minimum limits are specified but not tested on Propagation Delays.
12. See "Parameter Measurement Information" in the General Information section.

Document #: 38-00347-A

## Package Diagram

**24-Lead  Quarter Size Outline Q13**



0.033
REF.

0.150
0.157

0.228
0.244

0.337
0.344

0°–8°

0.016
0.034

0.007
0.010

SEATING
PLANE

0.053
0.069

0.004
0.010

0.025
BSC.

0.008
0.012

DIMENSIONS IN INCHES    MIN.
                        MAX.

LEAD COPLANARITY 0.004 MAX.

5

**IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.