

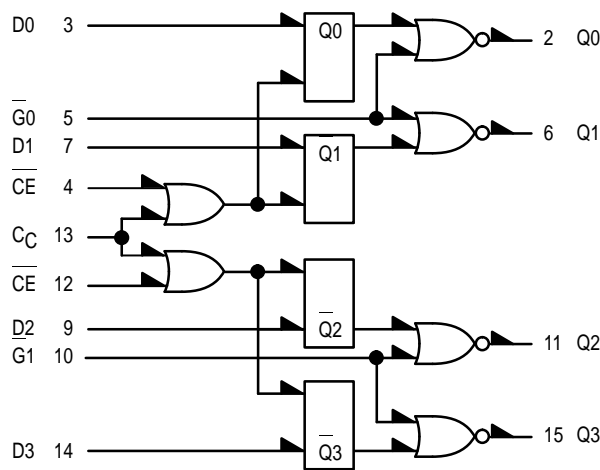
Quad Latch

The MC10133 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated when the output enable (G) is low. All four latches may be clocked at one time with the common clock (C_C), or each half may be clocked separately with its clock enable (CE).

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



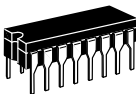
TRUTH TABLE

| \overline{G} | C | D | Q _{n+1} |
|----------------|---|---|------------------|
| H | X | X | L |
| L | L | X | Q _n |
| L | H | L | L |
| L | H | H | H |

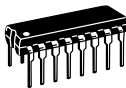
C = C_C + CE

V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

MC10133

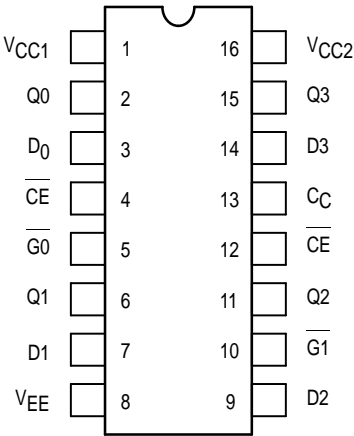


L SUFFIX
CERAMIC PACKAGE
CASE 620–10



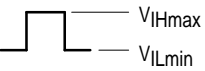
P SUFFIX
PLASTIC PACKAGE
CASE 648–08

DIP
PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Pin Under Test | Test Limits | | | | | | | Unit |
|----------------------------------|--------------------|----------------|-------------|--------|--------|-----|--------|--------|--------|------|
| | | | −30°C | | +25°C | | | +85°C | | |
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Power Supply Drain Current | I _E | 8 | | 82 | | | 75 | | 82 | mAdc |
| Input Current | I _{inH} | 3 | | 390 | | | 245 | | 245 | μAdc |
| | | 4 | | 425 | | | 265 | | 265 | |
| | | 5 | | 560 | | | 350 | | 350 | |
| | | 13 | | 560 | | | 350 | | 350 | |
| | I _{inL} | 3 | 0.5 | | 0.5 | | | 0.3 | | μAdc |
| Output Voltage Logic 1 | V _{OH} | 2 | −1.060 | −0.890 | −0.960 | | −0.810 | −0.890 | −0.700 | Vdc |
| | | 2 | −1.060 | −0.890 | −0.960 | | −0.810 | −0.890 | −0.700 | |
| Output Voltage Logic 0 | V _{OL} | 2 | −1.890 | −1.675 | −1.850 | | −1.650 | −1.825 | −1.615 | Vdc |
| | | 2 | −1.890 | −1.675 | −1.850 | | −1.650 | −1.825 | −1.615 | |
| | | 2 | −1.890 | −1.675 | −1.850 | | −1.650 | −1.825 | −1.615 | |
| Threshold Voltage Logic 1 | V _{OHA} | 2 | −1.080 | | −0.980 | | | −0.910 | | Vdc |
| | | 2 | −1.080 | | −0.980 | | | −0.910 | | |
| | | 2 | −1.080 | | −0.980 | | | −0.910 | | |
| | | 2† | −1.080 | | −0.980 | | | −0.910 | | |
| | | 2‡ | −1.080 | | −0.980 | | | −0.910 | | |
| | | 2‡ | −1.080 | | −0.980 | | | −0.910 | | |
| | | 2 | −1.080 | | −0.980 | | | −0.910 | | |
| | | 2 | −1.080 | | −0.980 | | | −0.910 | | |
| Threshold Voltage Logic 0 | V _{OLA} | 2 | | −1.655 | | | −1.630 | | −1.595 | Vdc |
| | | 2 | | −1.655 | | | −1.630 | | −1.595 | |
| | | 2 | | −1.655 | | | −1.630 | | −1.595 | |
| | | 2† | | −1.655 | | | −1.630 | | −1.595 | |
| | | 2‡ | | −1.655 | | | −1.630 | | −1.595 | |
| | | 2‡ | | −1.655 | | | −1.630 | | −1.595 | |
| Switching Times (50Ω Load) | | | | | | | | | ns | |
| Propagation Delay | t ₃₊₂₊ | 2 | 1.0 | 5.6 | 1.0 | 4.0 | 5.4 | 1.1 | 5.9 | |
| | t ₄₊₂₊ | 2 | 1.0 | 5.4 | 1.0 | 4.0 | 5.4 | 1.2 | 6.0 | |
| | t _{5−2+} | 2 | 1.0 | 3.2 | 1.0 | 2.0 | 3.1 | 1.0 | 3.4 | |
| | t _{setup} | 3 | 2.5 | | 2.5 | 0.7 | | 2.5 | | |
| | t _{hold} | 3 | 1.5 | | 1.5 | 0.7 | | 1.5 | | |
| Rise Time (20 to 80%) | t ₂₊ | 2 | 1.0 | 3.6 | 1.1 | 2.0 | 3.5 | 1.1 | 3.8 | |
| Fall Time (20 to 80%) | t _{2−} | 2 | 1.0 | 3.6 | 1.1 | 2.0 | 3.5 | 1.1 | 3.8 | |

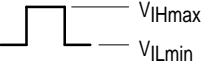
† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4) 

‡ Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

* Latch set to zero state before test.

ELECTRICAL CHARACTERISTICS (continued)

| @ Test Temperature | | | TEST VOLTAGE VALUES (Volts) | | | | | (V _{CC}) Gnd |
|----------------------------|--------------------|----------------|---|--------------------|---------------------|---------------------|-----------------|---------------------------|
| | | | V _{IHmax} | V _{ILmin} | V _{IHAmin} | V _{ILAmax} | V _{EE} | |
| | | | −30°C | −0.890 | −1.890 | −1.205 | −1.500 | −5.2 |
| | | | +25°C | −0.810 | −1.850 | −1.105 | −1.475 | −5.2 |
| | | | +85°C | −0.700 | −1.825 | −1.035 | −1.440 | −5.2 |
| Characteristic | Symbol | Pin Under Test | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | (V _{CC}) Gnd |
| | | | V _{IHmax} | V _{ILmin} | V _{IHAmin} | V _{ILAmax} | V _{EE} | |
| Power Supply Drain Current | I _E | 8 | | 13 | | | 8 | 1, 16 |
| Input Current | I _{inH} | 3 | 3 | | | | 8 | 1, 16 |
| | | 4 | 4 | | | | 8 | 1, 16 |
| | | 5 | 5 | | | | 8 | 1, 16 |
| | | 13 | 13 | | | | 8 | 1, 16 |
| | I _{inL} | 3 | | 3 | | | 8 | 1, 16 |
| Output Voltage Logic 1 | V _{OH} | 2 | 3, 4 | | | | 8 | 1, 16 |
| | | 2 | 3, 13 | | | | 8 | 1, 16 |
| Output Voltage Logic 0 | V _{OL} | 2 | 13 | 3 | | | 8 | 1, 16 |
| | | 2 | 3, 5, 13 | | | | 8 | 1, 16 |
| | | 2 | 4 | 3 | | | 8 | 1, 16 |
| Threshold Voltage Logic 1 | V _{OHA} | 2 | 3, 4 | | | 5 | 8 | 1, 16 |
| | | 2 | 4 | | 3 | | 8 | 1, 16 |
| | | 2 | 3, 4 | | | | 8 | 1, 16 |
| | | 2† | 3 | | | | 8 | 1, 16 |
| | | 2‡ | | | | | 8 | 1, 16 |
| | | 2‡ | | | | 4 | 8 | 1, 16 |
| | | 2 | 3 | | 4 | | 8 | 1, 16 |
| | | 2 | 3 | | 13 | | 8 | 1, 16 |
| Threshold Voltage Logic 0 | V _{OLA} | 2 | 3, 4 | | 5 | | 8 | 1, 16 |
| | | 2 | 4 | | | | 8 | 1, 16 |
| | | 2 | 4 | | | 3 | 8 | 1, 16 |
| | | 2† | | | | | 8 | 1, 16 |
| | | 2‡ | 3 | | | | 8 | 1, 16 |
| | | 2‡ | 3 | | | 13 | 8 | 1, 16 |
| Switching Times (50Ω Load) | | | +1.11V | | Pulse In | Pulse Out | −3.2 V | +2.0 V |
| Propagation Delay | t ₃₊₂₊ | 2 | 4 | | 3 | 2 | 8 | 1, 16 |
| | t ₄₊₂₊ | 2 | 3* | | 4 | 2 | 8 | 1, 16 |
| | t _{5−2+} | 2 | | | 5 | 2 | 8 | 1, 16 |
| | t _{setup} | 3 | | | 3 | 2 | 8 | 1, 16 |
| | t _{hold} | 3 | | | 3 | 2 | 8 | 1, 16 |
| Rise Time (20 to 80%) | t ₂₊ | 2 | 4 | | 3 | 2 | 8 | 1, 16 |
| Fall Time (20 to 80%) | t _{2−} | 2 | 4 | | 3 | 2 | 8 | 1, 16 |

† Output level to be measured after a clock pulse has been applied to the clock input (Pin 4) 

‡ Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

* Latch set to zero state before test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

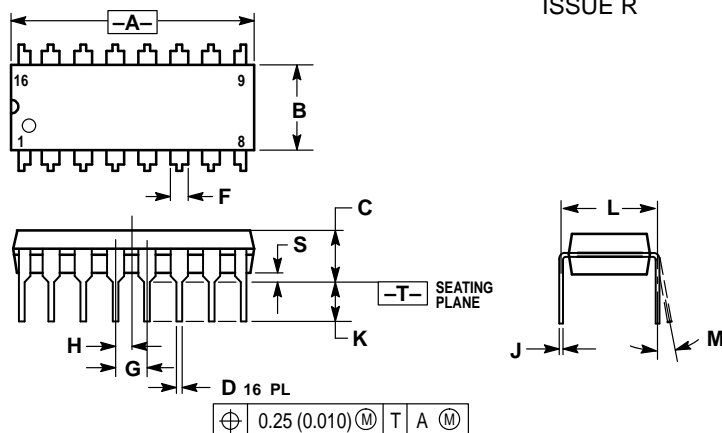
OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 620-10
ISSUE V


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | — | 0.200 | — | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE R


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

