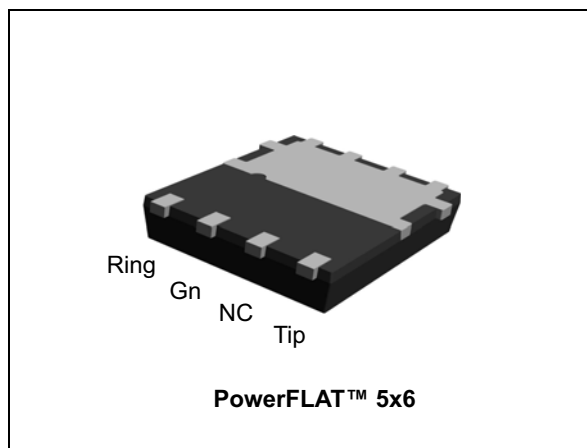


Programmable transient voltage suppressor for SLIC protection

Datasheet - production data



Description

This device has been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

LCP154DJF is specified to comply with ITU-T K20/21/45 and GR1089-Core when associated with Cooper Bussmann Telecom Circuit Protector fuse TCP 1.25 A.

LCP154DJF is packaged in a PowerFLAT™ 5x6 to meet IEC/UL 60950 clearance requirements.

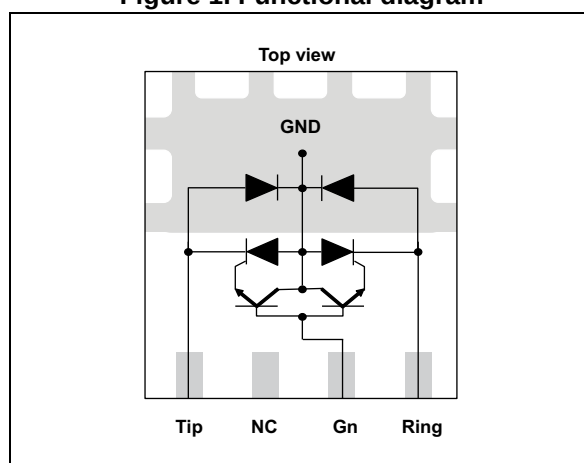
Features

- Programmable transient suppressor
- Wide negative firing voltage range: $V_{Gn} = -175\text{ V max.}$
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: $I_{GT} = 5\text{ mA max.}$
- Peak pulse current:
 - $I_{PP} = 100\text{ A (10/1000 }\mu\text{s)}$
 - $I_{PP} = 150\text{ A (5/310 }\mu\text{s)}$
 - $I_{PP} = 500\text{ A (2/10 }\mu\text{s)}$
- Holding current: $I_H = 150\text{ mA min.}$

Benefits

- Trisil™ is not subject to ageing and provides a fail safe mode in short-circuit for a better level of protection.
- Trisils are used to ensure equipment meets various standards such as UL60950, IEC 60950 / CSA C22.2, UL1459, TIA-968-A (formerly FCC part 68)
- Trisils have UL94 V0 approved resin (Trisils are UL497B approved [file: E136224]).

Figure 1. Functional diagram



TM: Trisil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Standards compliance

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10 μs 10/1000 μs	500 100	2/10 μs 10/1000 μs	0 0
GR-1089 Core Second level	5000	2/10 μs	500	2/10 μs	0
GR-1089 Core Intra-building	1500	2/10 μs	100	2/10 μs	0
ITU-T-K20/K21	6000 1500	10/700 μs	150 37.5	5/310 μs	0 0
ITU-T-K20 (IEC 61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
IEC 61000-4-5	4000 4000	10/700 μs 1.2/50 μs	100 100	5/310 μs 8/20 μs	0 0
TIA-968-A, lightning surge type A	1500 800	10/160 μs 10/560 μs	200 100	10/160 μs 10/560 μs	0 0
TIA-968-A, lightning surge type B	1000	9/720 μs	25	5/320 μs	0

Table 2. Absolute ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current ⁽¹⁾	10/1000 μs	100	A
		8/20 μs	400	
		10/560 μs	140	
		5/310 μs	150	
		10/160 μs	200	
		1/20 μs	400	
		2/10 μs	500	
I_{TSM}	Non repetitive surge peak on-state current (50 Hz sinusoidal) ⁽¹⁾	t = 10 ms	35	A
		t = 0.2 s	18	
		t = 1 s	12	
		t = 2 s	10	
		t = 15 min	4	
		t = 30 min	3	
V_{GN}	Negative battery voltage		-175	V
T_{stg}	Storage temperature range		-55 to +150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		-55 to +150	
T_L	Maximum lead temperature for soldering during 10 s.		260	$^{\circ}\text{C}$

1. The rated current values may be applied either to the RING to GND or to the Tip to GND terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the GND terminal current will be twice the rated current value of an individual terminal pair).

Figure 2. Electrical characteristics (definitions)

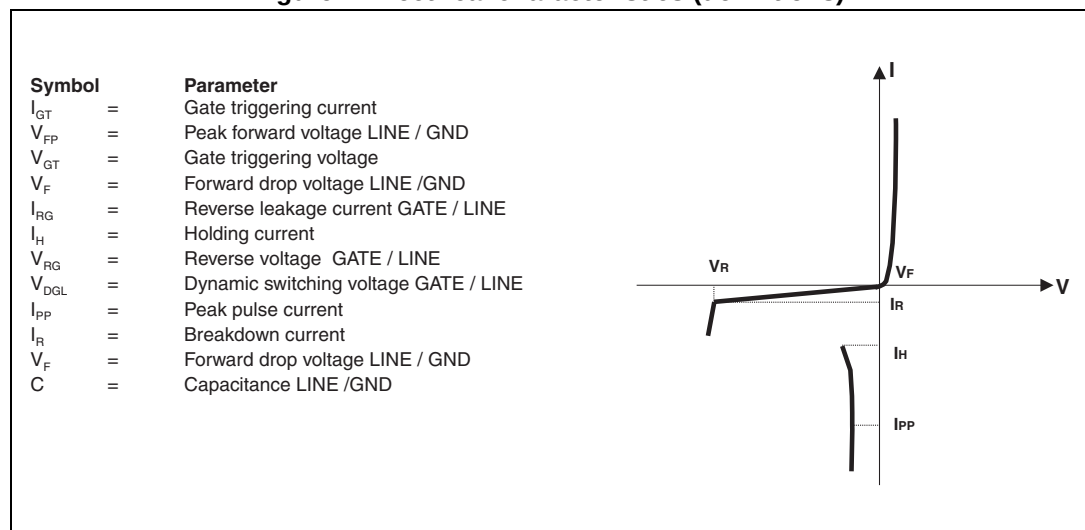
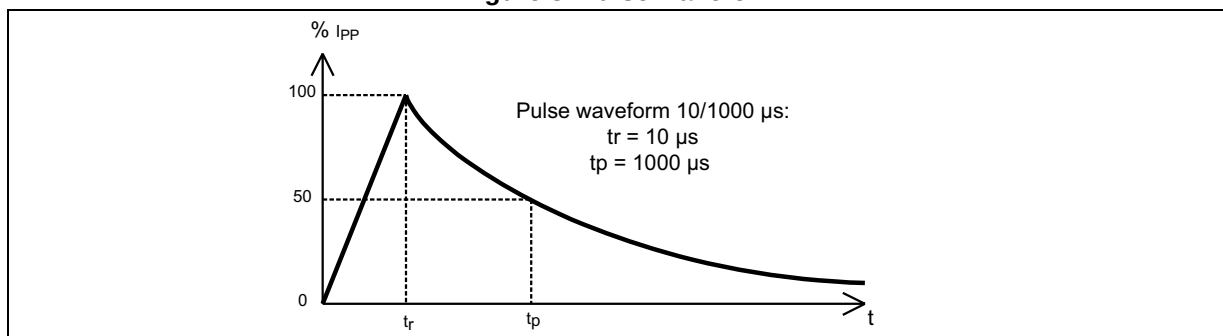


Figure 3. Pulse waveform

Table 3. Parameters ($T_{amb} = 25\text{ °C}$ unless otherwise specified)

Symbol	Test conditions		Min	Typ	Max	Unit
I_{GT}	$V_{LINE} = -48\text{ V}$		0.1		5	mA
I_H	$V_{Gn} = -48\text{ V}$		150			mA
$V_{GT}^{(1)}$	at I_{GT}				2.5	V
I_{RG}	$V_{RG} = -175\text{ V}$ $V_{RG} = -175\text{ V}$	$T_j = 25\text{ °C}$ $T_j = 85\text{ °C}$			5 50	μA
$V_{DGL}^{(1)}$	$V_{Gn} = -48\text{ V}^{(1)}$	10/700 μs 2/10 μs			12 20	V
V_F	$I_F = 5\text{ A}$				3	V
$V_{FP(I)}$	10/700 μs 2/10 μs	$I_{pp} = 150\text{ A}$ $I_{pp} = 200\text{ A}$			7 10	V
I_R	$V_{Gn} / LINE = -1\text{ V}$ $V_{LINE} = -175\text{ V}$ $V_{Gn} / LINE = -1\text{ V}$ $V_{LINE} = -175\text{ V}$	$T_j = 25\text{ °C}$ $T_j = 85\text{ °C}$			5 50	μA
C	$V_{LINE} = -50\text{ V}$, $V_{RMS} = 1\text{ V}$, $f = 1\text{ MHz}$ $V_{LINE} = -2\text{ V}$, $V_{RMS} = 1\text{ V}$, $f = 1\text{ MHz}$			35 100		pF
C_G	Gate decoupling capacitance		100	220		nF

1. The oscillations with a time duration lower than 50 ns are not taken into account.

2 Technical information

Figure 4. Example of PCB layout based on LCP154DJF protection

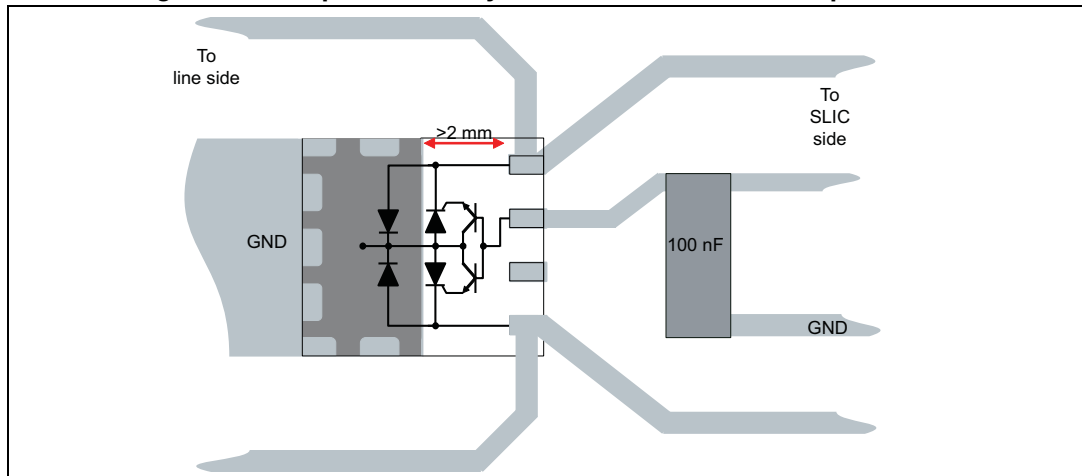


Figure 4 shows the classical PCB layout used to optimize line protection. The 2 mm distance is used to comply with IEC/UL 60950 clearance requirements.

The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.

This allows minimization of the dynamic breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - Vbat pin.

So to be efficient it has to be as close as possible from the LCP Gate pin and from the reference ground track (or plan).

The schematics of *Figure 5* give the topology used to protect all SLICs according to ITU-T K20/21/45 and GR1089-Core.

Figure 5. Protection of high voltage SLIC

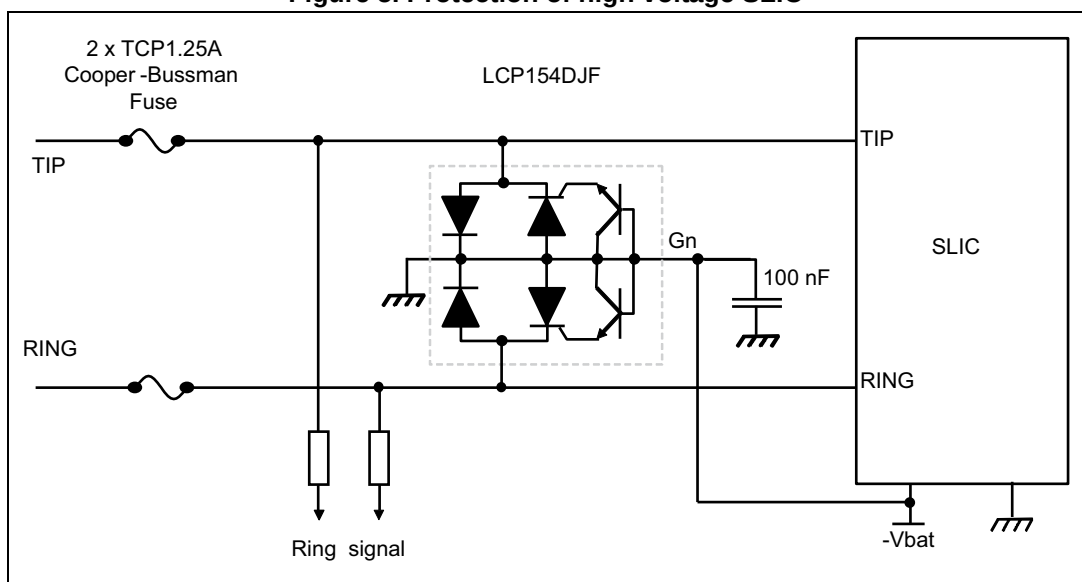


Figure 6. Surge peak current versus duration

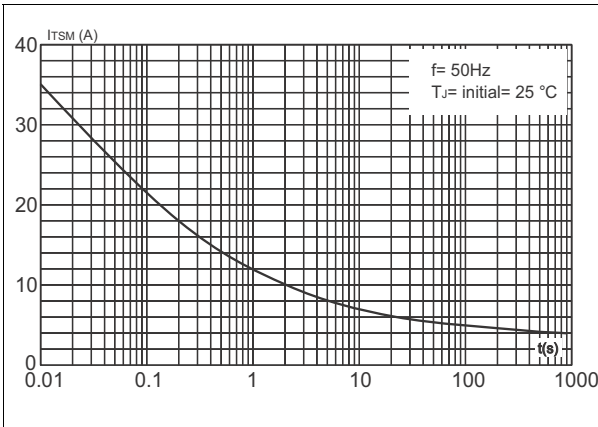
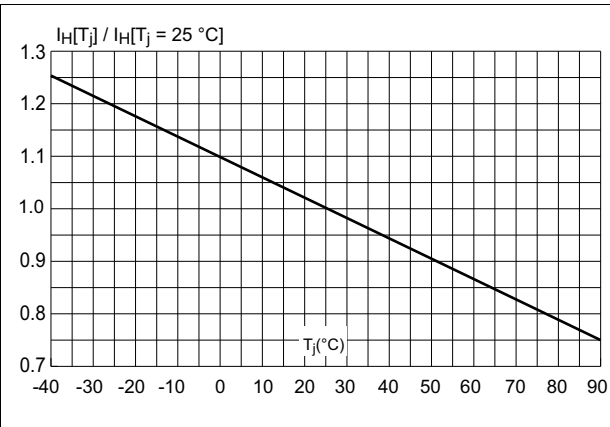


Figure 7. Relative variation of holding current versus junction temperature



3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

3.1 PowerFLAT™ 5x6 package information

Figure 8. PowerFLAT™ 5x6 package outline

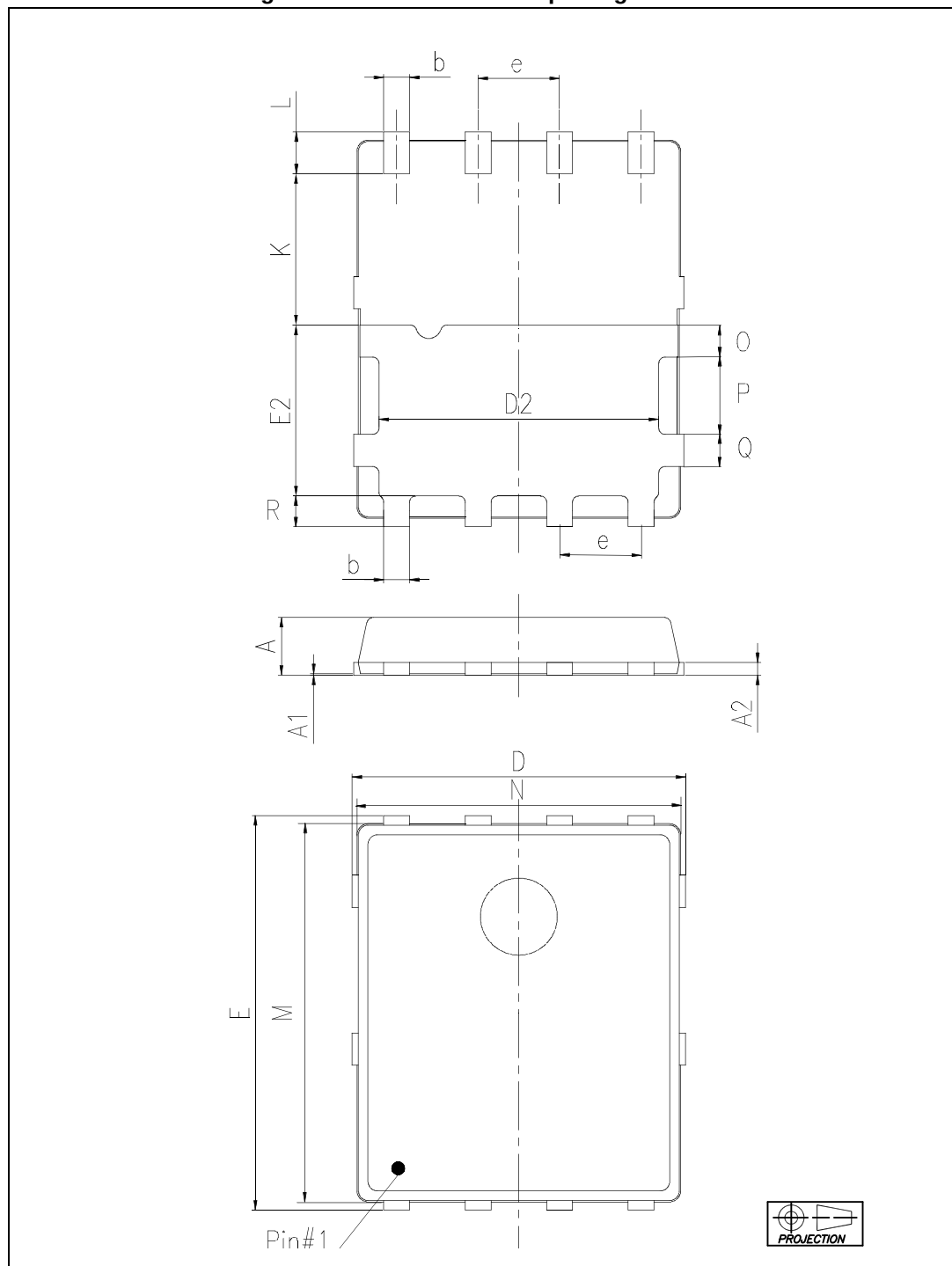


Table 4. PowerFLAT™ 5x6 mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.315		0.394
A1	0.02		0.05	0.008		0.020
A2		0.25			0.098	
b	0.30		0.50	0.118		0.197
D	5.0		5.4	1.969		2.126
E	5.95		6.35	2.343		2.500
D2	4.25		4.45	1.673		1.752
E2	2.56		2.76	1.008		1.087
e		1.27			0.500	
L	0.50		0.80	0.197		0.315
K	2.25			0.886		
M	5.75		5.95	2.264		2.343
N	4.90		5.10	1.929		2.008
O	0.40		0.60	0.157		0.236
P	1.10		1.30	0.433		0.512
Q	0.40		0.60	0.157		0.236
R	0.35		0.65	0.138		0.256

Figure 9. PowerFLAT™ 5x6 recommended footprint (all dimensions are in mm.)

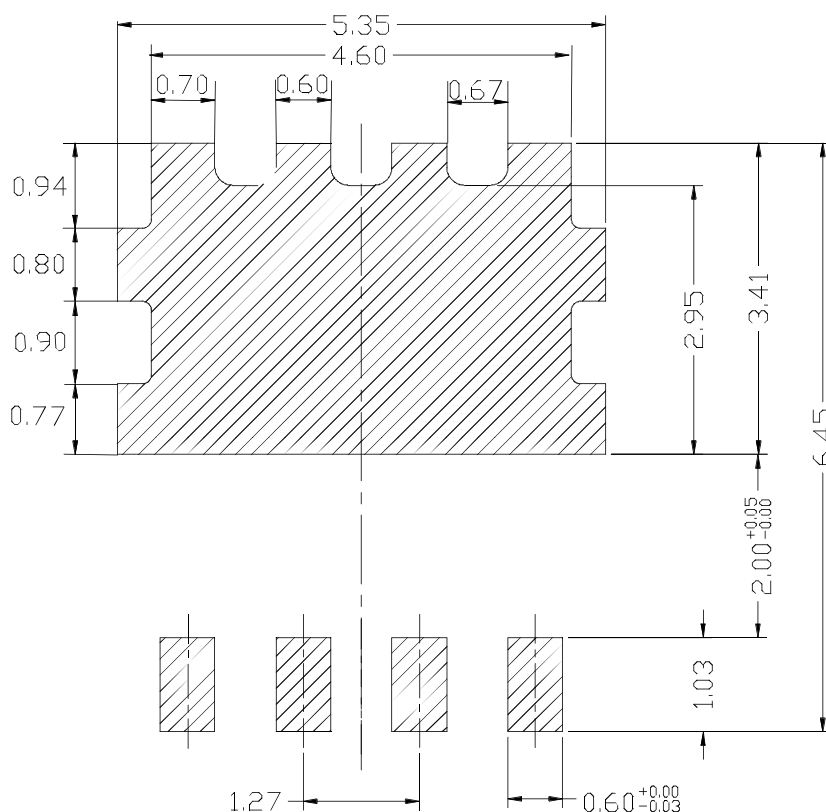
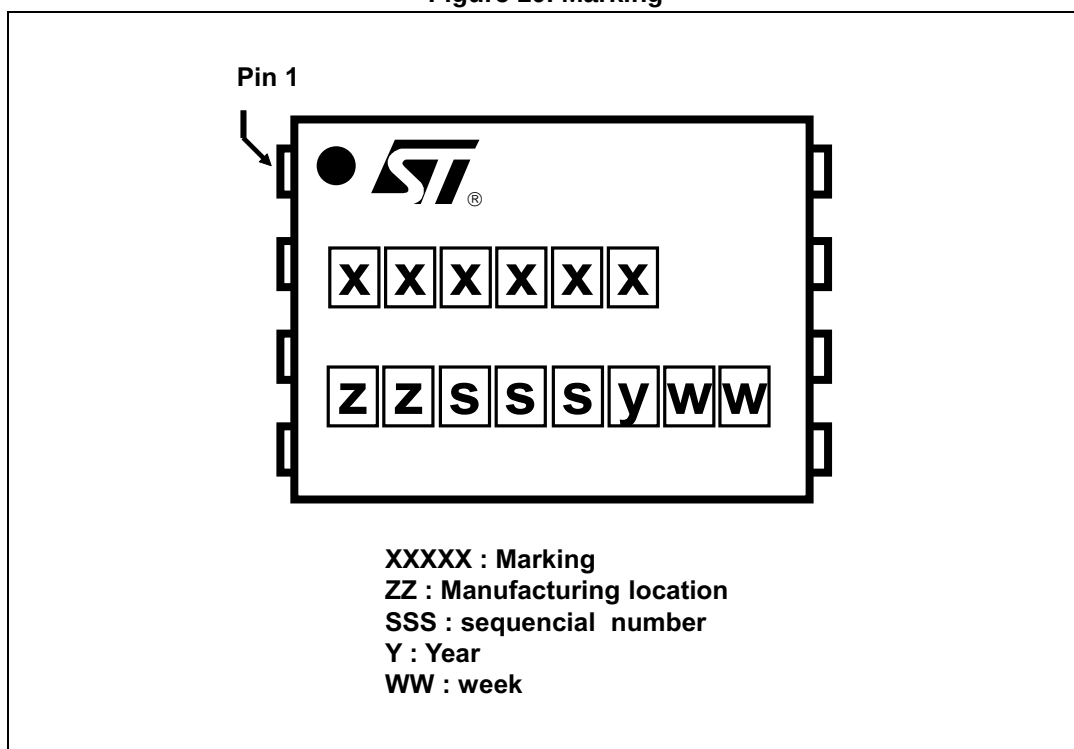


Figure 10. Marking



4 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LCP154DJF	CP154	PowerFLAT 5x6	91 mg	3000	Tape and reel

5 Revision history

Table 6. Document revision history

Date	Revision	Changes
13-Oct-2015	1	First issue.

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