- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses With Parity**
- **Buffered Control Inputs to Reduce dc Loading Effects**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

**SN74ALS841, SN74AS841A . . . DW OR NT PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| $\overline{OE}$ | 1 | 24 | $V_{CC}$ |
| 1D | 2 | 23 | 1Q |
| 2D | 3 | 22 | 2Q |
| 3D | 4 | 21 | 3Q |
| 4D | 5 | 20 | 4Q |
| 5D | 6 | 19 | 5Q |
| 6D | 7 | 18 | 6Q |
| 7D | 8 | 17 | 7Q |
| 8D | 9 | 16 | 8Q |
| 9D | 10 | 15 | 9Q |
| 10D | 11 | 14 | 10Q |
| GND | 12 | 13 | LE |

**SN74ALS842 . . . DW OR NT PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| $\overline{OE}$ | 1 | 24 | $V_{CC}$ |
| $1\overline{D}$ | 2 | 23 | 1Q |
| $2\overline{D}$ | 3 | 22 | 2Q |
| $3\overline{D}$ | 4 | 21 | 3Q |
| $4\overline{D}$ | 5 | 20 | 4Q |
| $5\overline{D}$ | 6 | 19 | 5Q |
| $6\overline{D}$ | 7 | 18 | 6Q |
| $7\overline{D}$ | 8 | 17 | 7Q |
| $8\overline{D}$ | 9 | 16 | 8Q |
| $9\overline{D}$ | 10 | 15 | 9Q |
| $10\overline{D}$ | 11 | 14 | 10Q |
| GND | 12 | 13 | LE |

## description

These 10-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.
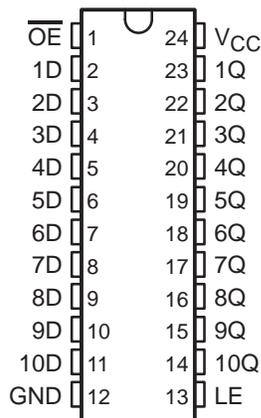
The ten latches are transparent D-type latches. The SN74ALS841 and SN74AS841A have noninverting data (D) inputs. The SN74ALS842 has inverting $\overline{D}$ inputs.

A buffered output-enable ($\overline{OE}$) input places the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.
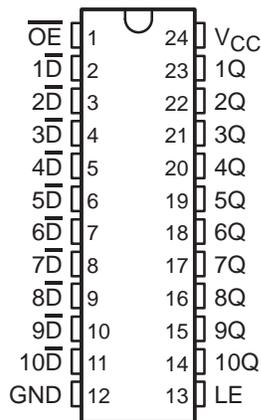
$\overline{OE}$ does not affect the internal operation of the latches. Previously stored data can be retained or new data can be entered while the outputs are off.

The SN74ALS841, SN74AS841A, and SN74ALS842 are characterized for operation from 0°C to 70°C.

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**TEXAS INSTRUMENTS**

**Function Tables**

**SN74ALS841, SN74AS841A**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

**SN74ALS842**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | $\overline{D}$ | Q |
| L | H | H | L |
| L | H | L | H |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbols[†]

**SN74ALS841, SN74AS841A**

| | | |
|---|---|---|
| $\overline{OE}$ 1 | EN | |
| LE 13 | C1 | |
| 1D 2 | 1D ▷ ▽ | 23 1Q |
| 2D 3 | | 22 2Q |
| 3D 4 | | 21 3Q |
| 4D 5 | | 20 4Q |
| 5D 6 | | 19 5Q |
| 6D 7 | | 18 6Q |
| 7D 8 | | 17 7Q |
| 8D 9 | | 16 8Q |
| 9D 10 | | 15 9Q |
| 10D 11 | | 14 10Q |

**SN74ALS842**

| | | |
|---|---|---|
| $\overline{OE}$ 1 | EN | |
| LE 13 | C1 | |
| 1$\overline{D}$ 2 | 1D ▷ ▽ | 23 1Q |
| 2$\overline{D}$ 3 | | 22 2Q |
| 3$\overline{D}$ 4 | | 21 3Q |
| 4$\overline{D}$ 5 | | 20 4Q |
| 5$\overline{D}$ 6 | | 19 5Q |
| 6$\overline{D}$ 7 | | 18 6Q |
| 7$\overline{D}$ 8 | | 17 7Q |
| 8$\overline{D}$ 9 | | 16 8Q |
| 9$\overline{D}$ 10 | | 15 9Q |
| 10$\overline{D}$ 11 | | 14 10Q |
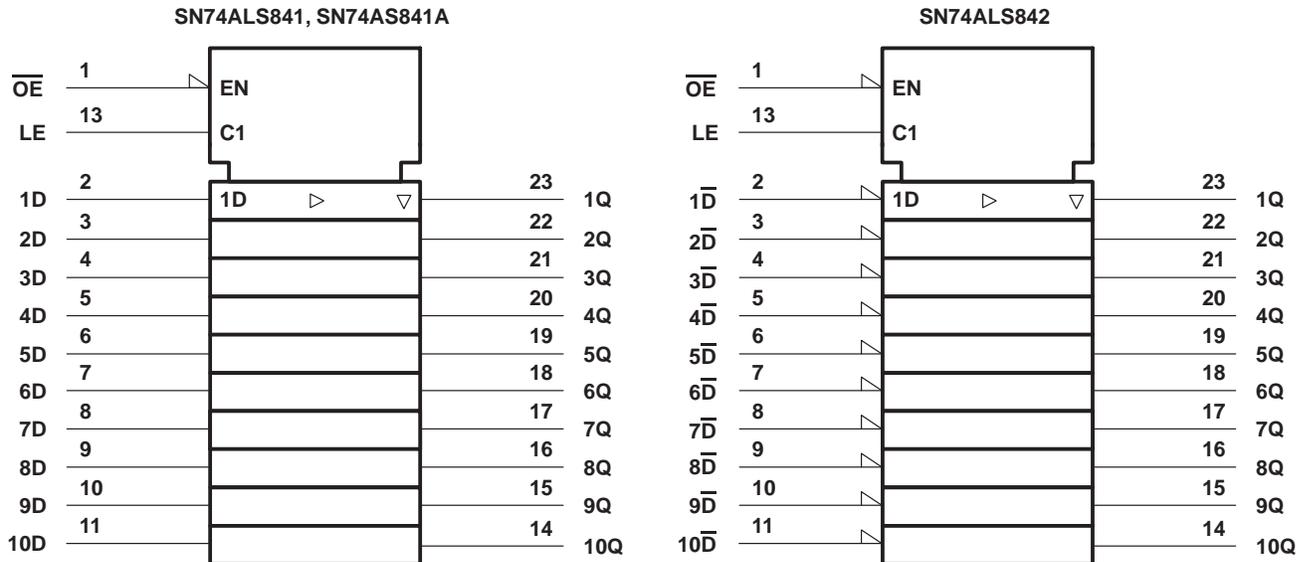
[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagrams (positive logic)
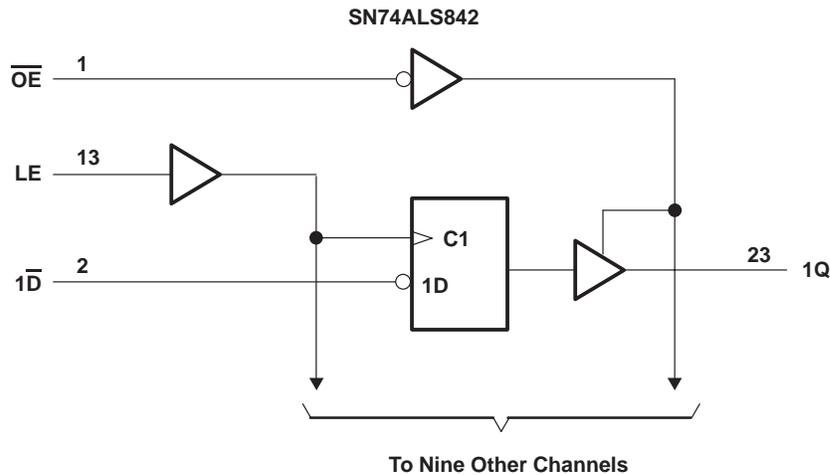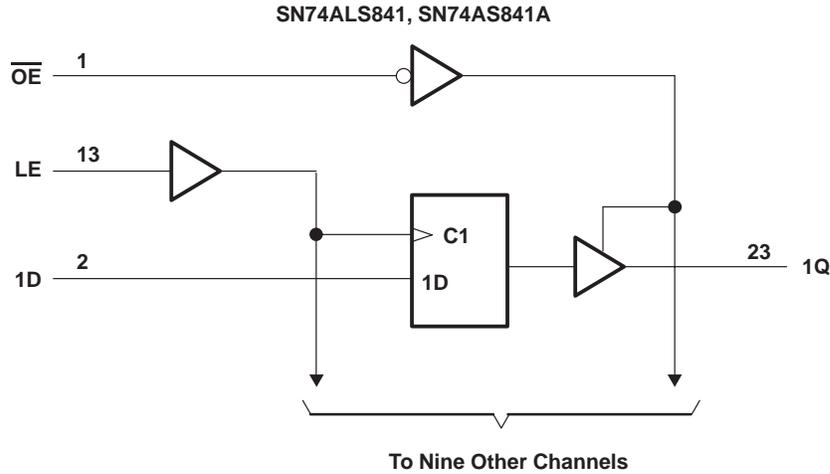
**SN74ALS841, SN74AS841A**



**To Nine Other Channels**

**SN74ALS842**



**To Nine Other Channels**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .......................................................................... 7 V
Input voltage, $V_I$ .............................................................................. 7 V
Voltage applied to a disabled 3-state output ................................................ 5.5 V
Operating free-air temperature range, $T_A$:  SN74ALS841, SN74ALS842 .................... 0°C to 70°C
Storage temperature range ................................................................ −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | SN74ALS841 SN74ALS842 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −2.6 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $t_w$ | Pulse duration, LE high | 20 | | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 10 | | | ns |
| $t_h$ | Hold time, data after LE↓ | 5 | | | ns |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN74ALS841 SN74ALS842 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −0.4 mA | $V_{CC}$ −2 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = −2.6 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −20 | µA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.1 | mA |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | SN74ALS841 | $V_{CC}$ = 5.5 V | Outputs high | | 19 | 30 | mA |
| | | | Outputs low | | 38 | 62 | |
| | | | Outputs disabled | | 23 | 40 | |
| | SN74ALS842 | $V_{CC}$ = 5.5 V | Outputs high | | 20 | 35 | |
| | | | Outputs low | | 48 | 74 | |
| | | | Outputs disabled | | 27 | 44 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 $\Omega$, R2 = 500 $\Omega$, $T_A$ = MIN to MAX[†] SN74ALS841 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{PLH}$ | D | Q | 2 | 13 | ns |
| $t_{PHL}$ | | | 2 | 13 | |
| $t_{PLH}$ | LE | Q | 7 | 21 | ns |
| $t_{PHL}$ | | | 8 | 26 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 2 | 12 | ns |
| $t_{PZL}$ | | | 2 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 2 | 10 | ns |
| $t_{PLZ}$ | | | 2 | 12 | |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 $\Omega$, R2 = 500 $\Omega$, $T_A$ = MIN to MAX[†] SN74ALS842 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{PLH}$ | $\overline{D}$ | Q | 4 | 18 | ns |
| $t_{PHL}$ | | | 3 | 13 | |
| $t_{PLH}$ | LE | Q | 8 | 27 | ns |
| $t_{PHL}$ | | | 6 | 20 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 2 | 12 | ns |
| $t_{PZL}$ | | | 2 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 1 | 10 | ns |
| $t_{PLZ}$ | | | 2 | 12 | |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7 V
Input voltage, $V_I$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V
Operating free-air temperature range, $T_A$: SN74AS841A . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0°C to 70°C
Storage temperature range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . −65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | SN74AS841A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −24 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | mA |
| $t_w$ | Pulse duration, LE high | 4 | | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 2.5 | | | ns |
| $t_h$ | Hold time, data after LE↓ | 2.5 | | | ns |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN74AS841A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = −2 mA | $V_{CC}$−2 | | | V |
| | $V_{CC}$ = 4.5 V | $I_{OH}$ = −15 mA | 2.4 | 3.2 | | |
| | | $I_{OH}$ = −24 mA | 2 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | 0.35 | 0.5 | V |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | −50 | μA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | −0.5 | mA |
| $I_O$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | −30 | | −112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 36 | 60 | mA |
| | | Outputs low | | 58 | 94 | |
| | | Outputs disabled | | 56 | 93 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

**switching characteristics (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 $\Omega$, R2 = 500 $\Omega$, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|
| | | | SN74AS841A | | |
| | | | MIN | MAX | |
| $t_{PLH}$ | D | Q | 1 | 6.5 | ns |
| $t_{PHL}$ | | | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | 2 | 12 | ns |
| $t_{PHL}$ | | | 2 | 12 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 2 | 14 | ns |
| $t_{PZL}$ | | | 2 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 1 | 8 | ns |
| $t_{PLZ}$ | | | 1 | 8 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

**LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**
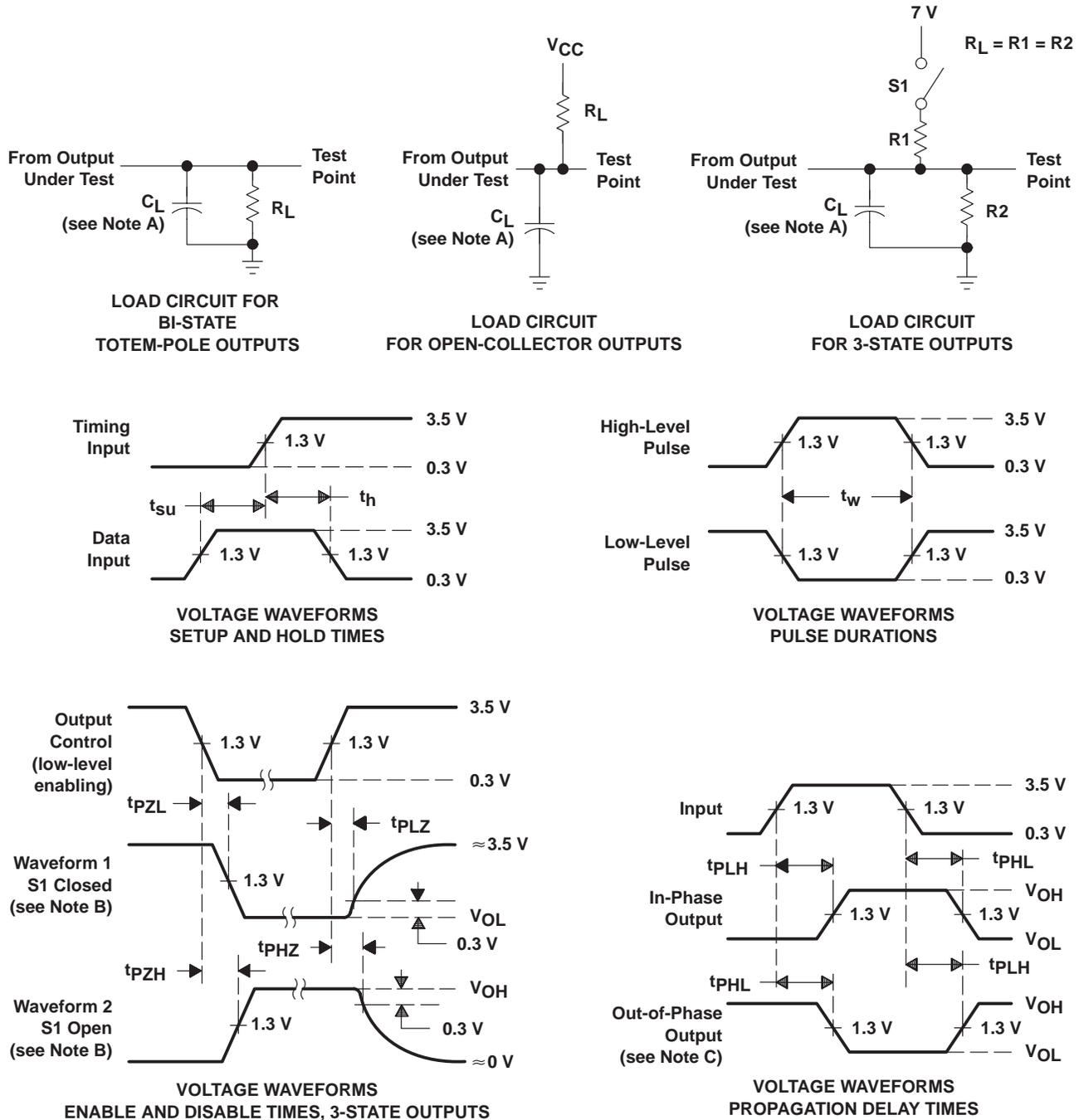
NOTES:  A.  $C_L$ includes probe and jig capacitance.
        B.  Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
            Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
        C.  When measuring propagation delay items of 3-state outputs, switch S1 is open.
        D.  All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
        E.  The outputs are measured one at a time with one transition per measurement.

## Figure 1. Load Circuits and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| SN74ALS841DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS841DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS841DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS841DWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALS841NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ALS841NTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ALS842DW | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI |
| SN74ALS842NT | OBSOLETE | PDIP | NT | 24 | | TBD | Call TI | Call TI |
| SN74AS841ADW | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI |
| SN74AS841ADWR | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI |
| SN74AS841ANT | OBSOLETE | PDIP | NT | 24 | | TBD | Call TI | Call TI |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
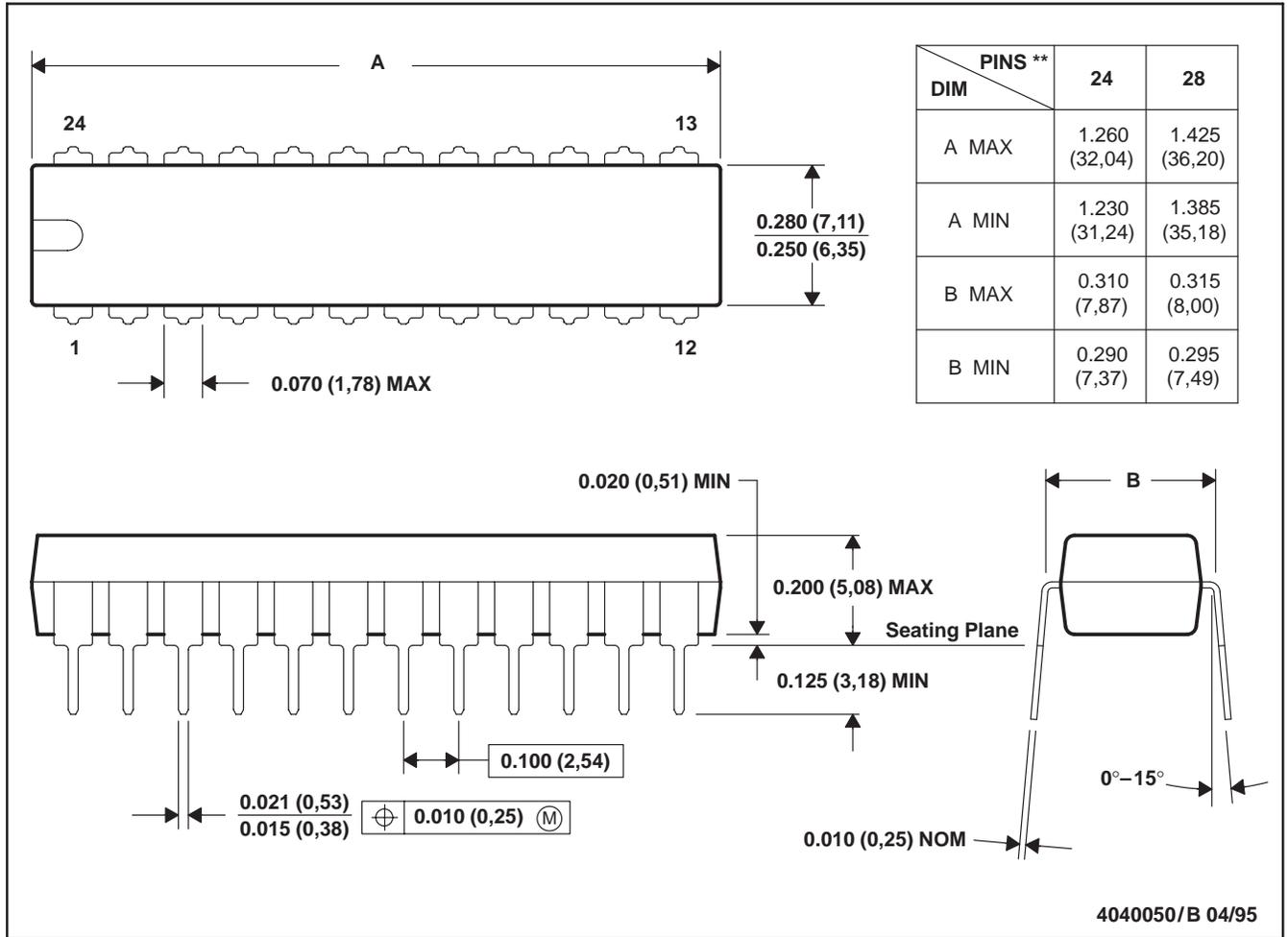
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## NT (R-PDIP-T**)

**PLASTIC DUAL-IN-LINE PACKAGE**

**24 PINS SHOWN**

| PINS ** DIM | 24 | 28 |
|---|---|---|
| A  MAX | 1.260 (32,04) | 1.425 (36,20) |
| A  MIN | 1.230 (31,24) | 1.385 (35,18) |
| B  MAX | 0.310 (7,87) | 0.315 (8,00) |
| B  MIN | 0.290 (7,37) | 0.295 (7,49) |

A

24    13

0.280 (7,11)
0.250 (6,35)

1    12

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

B

0°–15°

0.021 (0,53)
0.015 (0,38)    ⊕ 0.010 (0,25) Ⓜ

0.100 (2,54)

0.010 (0,25) NOM

4040050/B 04/95

NOTES:  A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.

## DW (R−PDSO−G24)  PLASTIC SMALL−OUTLINE PACKAGE

0.614 (15,60)
0.598 (15,20)

24        13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1        12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/F 06/2004

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D.  Falls within JEDEC MS−013 variation AD.

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