KSZ8463MLI/RLI Evaluation Board User Guide

Preliminary Revision 1.03 / September 23, 2011

Table of Contents

List of Figures

List of Tables

Introduction

The KSZ8463MLI/RLI Evaluation Board provides a platform in which to test or explore the functionally of the KSZ8463MLI and KSZ8463RLI IEEE 1588 Precision Time Protocol (PTP) enabled switch products.

The KSZ8463MLI and KSZ8463RLI devices are highly integrated 2-port 10/100Base-T/TX/FX managed Ethernet switch with MII and RMII interface connectivity to a Host on Port 3. They are the ideal solution in industrial applications where real time clock synchronization using Ethernet connectivity across a network is desired. The KSZ8463MLI/RLI includes all the functions of a 10/100Base-T/TX/FX switch system that combines switch engine, frame buffers management, addresses look-up table, queue management, MIB counters, media access controllers (MAC) and PHY transceiver interfaces. The KSZ8463MLI/RLI is fully compliant with the IEEE 1588 (Version 2) Precision Time Protocol, IEEE 802.3 (10/100Base-T/TX) and IEEE 802.3u (100Base-FX) standards. The KSZ8463MLI device has Port 3 configured for MII mode while the KSZ8463RLI device has Port 3 configured for RMII mode.

This KSZ8463MLI/RLI Evaluation Board User Guide provides the information necessary to configure and set up the board to evaluate or test the KSZ8463MLI and KSZ8463RLI devices in different environments.

1 Board Features

The KSZ8463MLI/RLI Evaluation Board encompasses the following features.

- Micrel's KSZ8463MLI or KSZ8463RLI Integrated 3-Port 10/100 Managed Ethernet Switch
- Two RJ-45 Jacks for Ethernet LAN Interfaces with corresponding Isolation Magnetics (Port 1 & 2)
- Auto MDI/MDI-X for automatic detection and correction for straight-through and crossover cables
- 1 PHY Mode and 1 MAC Mode MII Connector for the Switch RMII/MII Interface (Port 3)
- Provisioning for 2 100Base-FX fiber interfaces (optional)
- Provisioning for line side and chip side over-voltage protection
- Onboard 3.3V and 1.8V/2.5V regulators
- Configurable for VDDIO of 3.3V, 2.5V, or 1.8V operation
- 1 USB port to emulate an MIIM or SPI Interface
- LED indicators for link status and activity of the RJ45 ports
- Onboard 25 MHz crystal
- An on-board 50 MHz Oscillator (Y2) for RMII
- Jumpers to configure strapping pins for power up configuration of the device
- Jumpers for GPIO pins, I/O voltage selection and serial-port connections
- 5V DC voltage required for operation
- Reset switch
- Various test points

2 KSZ8463MLI/RLI Evaluation Board Kit

The KSZ8463MLI/RLI Evaluation Board kit includes the following:

- KSZ8463MLI/RLI Evaluation Board
- KSZ8463MLI/RLI Evaluation Board User's Guide (This document)
- KSZ8463MLI/RLI Evaluation Board Schematic (Contact your Micrel FAE for the latest schematic)

3 Hardware Description

The KSZ8463MLI/RLI Evaluation board is a small form-factor board (5.2” x 4.75”) that can be configured through its USB port. There are two options for configuration: Strap-in mode and SPI mode. Strap-in mode configuration occurs at power on time where the voltage level on certain pins is automatically sampled and used to configure various features in the device. This is accomplished with the on board jumper options. SPI mode is facilitated via the onboard USB port interface. The SPI interface can be used to read or write the registers within the KSZ8463MLI/RLI device. An FT2232D chip is used for the USB interface. Configuration options are explained in detail in the following sections. Figure 1 is a picture of the KSZ8463MLI/RLI Evaluation board.

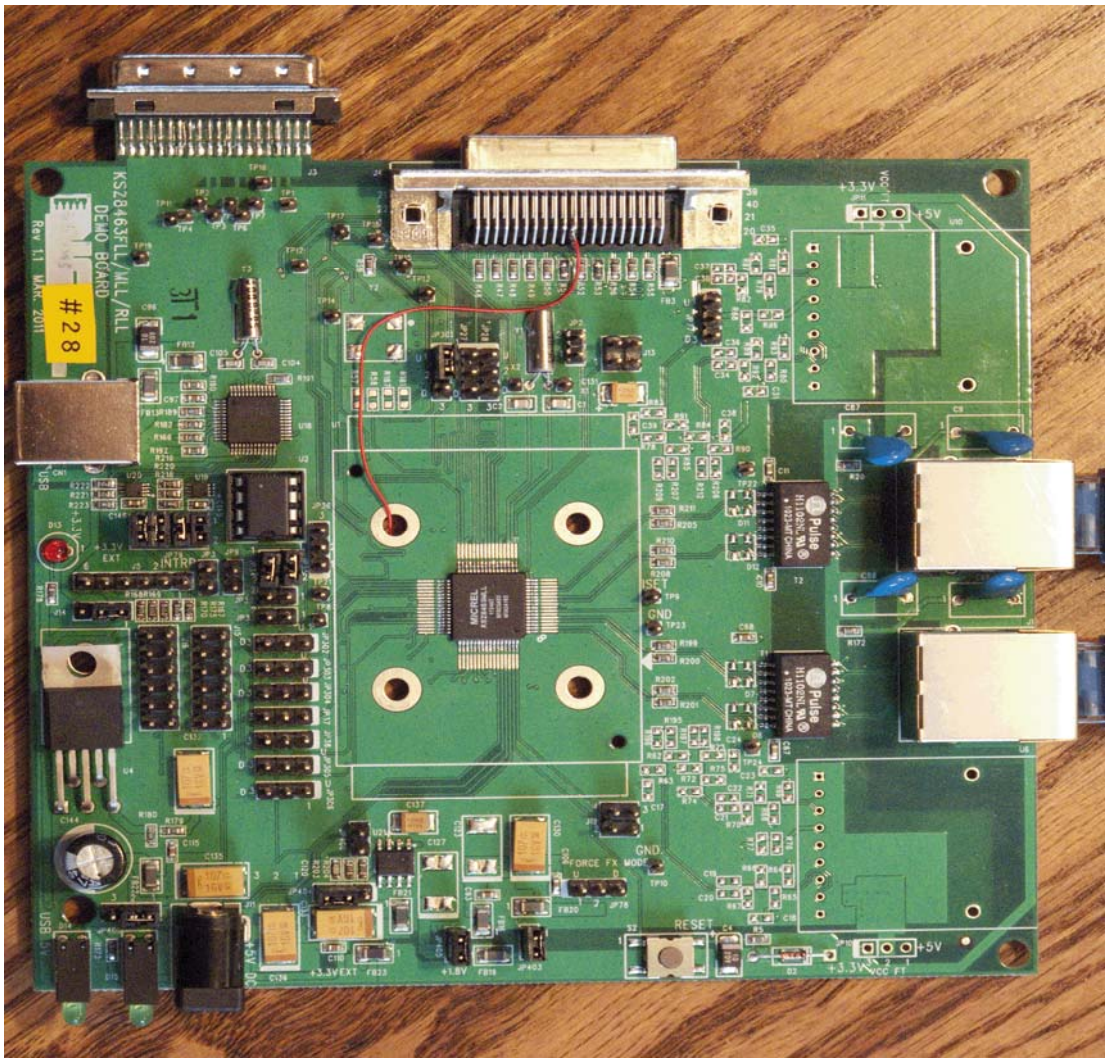

Figure 1 KSZ8463MLI/RLI Evaluation Board

3.1 Configuration Options

3.1.1 Strap-in Mode

Strap-in configuration mode is the quickest and easiest way to get started. In this mode, the KSZ8463MLI/RLI acts as a standalone 3-port switch. This is accomplished by setting available configuration jumpers which are used at device power-up. Simply set the board's configuration jumpers to the desired settings and apply power to the board. The configuration can be changed while power is applied to the board by changing the jumper settings and pressing the convenient manual reset button for the new settings to take effect. Note that even if no external strap-in values are set, internal pull-up and pull-down resistors will set the KSZ8463MLI/RLI to the default configuration. The following table covers each jumper used for the strap-in option and describes its function.

JUMPER	FUNCTION	SETTING			DEFAULT
JP301	PHY/MAC mode select for MII port	Pins 1-2 closed: PHY MII mode Pins 2-3 closed: MAC MII mode			PHY MII mode
JP302	High-speed/Low-speed SPI selection	Pins 1-2 closed: High speed (up to 50 MHz) Pins 2-3 closed: Low speed (up to 12.5 MHz)			High speed
	Serial Bus Mode Selection		**SPI Slave**	**MIIM (MDIO)**	SPI Slave
JP303			Pins 1-2 closed	Pins 1-2 closed	
JP304			Pins 2-3 closed	Pins 1-2 closed	
JP305	Xclk Frequency	Pins 1-2 closed: 25MHz from X1/X2 Pins 2-3 closed: 50MHz from REFCLK_I			25MHz

Table 1 Strap-In Configuration Jumpers

3.1.2 USB Mode (SPI Slave or MDIO)

With the Micrel software that runs on a PC, it is possible to access the full register set of the device through the USB port provided on the evaluation board. The USB interface can be programmed to make use of KSZ8463's serial interface, which is configurable as an SPI (slave) or an MDIO port.

The FT2232D controller on the evaluation board can be used for accessing any other MDIO enabled device connected through the MII connector. MDIO data and clock signals on the MII connectors are enabled by closing jumpers JP32 and 33.

For proper MDIO operation a jumper needs to be inserted between pins 3 and 4 of the connector J5. For a description of all related jumpers please refer to Table 9.

3.2 Power Supplies

The board requires a single 5V DC supply, which can be provided through a standard power-supply jack (J11) or through the USB port. JP400 is used for selecting the 5V source to the board. There is a 3.3V regulator on the board supplying power for the KSZ8463 and other components. A separate on-board voltage regulator is provided for the optional 2.5V and 1.8V supplies for KSZ8463's I/O interface (VDD_IO). JP404 and JP406 are used for VDD_IO selection. JP403 and JP405 must be in place and other options properly selected before powering up the board.

JUMPER	FUNCTION	SETTING		
JP400	+5V supply source selection	Pins 1-2 closed: Connector (J11) Pins 2-3 closed: USB port		
JP403	+3.3V supply for KSZ8463 analog circuits	Must be closed		
JP405	+1.2V supply for KSZ8463 analog circuits	Must be closed		
	VDD_IO selection	**3.3V**	**2.5V**	**1.8V**
JP404		Pins 2-3 closed	Pins 1-2 closed	Pins 1-2 closed
JP406		X	open	Closed

Table 2 Power Supply Related Jumpers

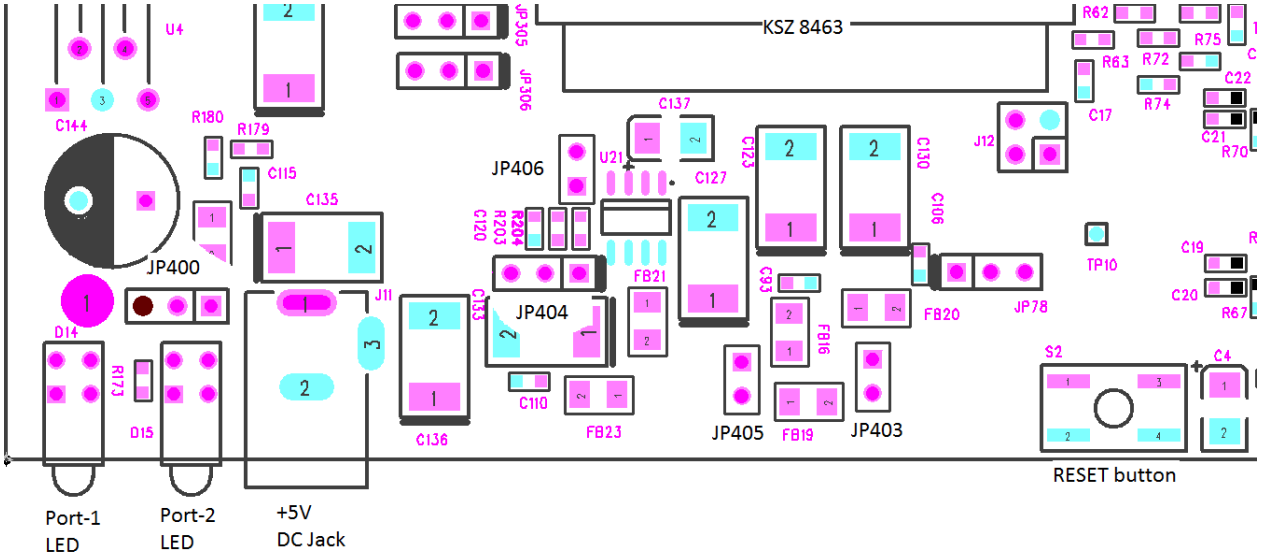

Figure 2 Power Supply Section and Related Jumper Locations

3.3 Port-3 Configuration

The board features two Media Independent Interface (MII) connectors, for interfacing the MAC of Port-3 on the KSZ8463MLI/RLI to either an external PHY or MAC. The female MII connector (J4) is used for interfacing to a PHY, such as Micrel KSZ8051 and the male MII connector (J3) is used for interfacing to any host processor's MAC interface. E.g. in order to evaluate the IEEE1588 PTP functionality, a host processor board such as the Micrel KSZ9692 SOC board has to be connected to the MII interface. A jumper is provided (JP301) to set Port-3 in PHY or MAC mode of operation at power-up.

The KSZ8463MLI provides a bypass feature in the MII PHY mode. JP27 is used to enable the MII bypass mode. In the bypass mode, MII (port 3) is shut down and no new ingress frames from either Port 1 or Port 2 will be sent out through Port 3. Only the switch between Port 1 and Port 2 is active for all ingress packets, and the frames for Port 3 already in packet memory will be flushed out.

The KSZ8463MLI uses the full MII signaling pins of the connectors, whereas the KSZ8463RLI makes use of a subset of the available pins, as defined by the RMII standard. The RMII standard requires a 50 MHz clock which can be generated by the KSZ8463RLI chip, or supplied externally. The KSZ8463MLI/RLI

Evaluation board provides both options. JP28 enables or disables the generation of the 50 MHz clock by the KSZ8463RLI. An on-board 50 MHz Oscillator (Y2) is also provided.

JUMPER	FUNCTION	SETTING
JP301	MAC/PHY mode selection for MII on Port-3	Pins 1-2 closed: PHY mode (default) Pins 2-3 closed: MAC mode
JP27	Bypass mode for MII PHY mode link	Pins 1-2 closed: Bypass enabled Pins 2-3 closed: Normal operation (default)
JP28	50 MHz Reference clock generation	Pins 1-2 closed: Enabled (EN_REFCLKO pin = 1) Pins 2-3 closed: Disabled (default) (EN_REFCLKO pin = 0)

Table 3 MII Port Configuration Settings

3.3.1 MII Port Configuration (KSZ8463MLI)

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3u Standard. It provides a common interface between PHY layer and MAC layer devices. The MII provided by the KSZ8463MLI is connected to the device's third MAC (Port 3). The interface contains two distinct groups of signals, one for transmission and the other for reception. The following table describes the signals used by the MII interface to connect either external MAC or external PHY.

Signal Name on MII connectors	Description	Pin numbers	Signal direction in PHY mode: (Connector J3)	Signal direction in MAC mode: (Connector J4)	Test Points
TX_EN	Transmit enable	13	input	output	TP6
TX_ER	Transmit error	11	input	GND	TP15
TXD3	Transmit data bit 3	17	input	output	TP18
TXD2	Transmit data bit 2	16	Input	output	TP17
TXD1	Transmit data bit 1	15	Input	output	TP16
TXD0	Transmit data bit 0	14	input	output	TP7
TX_CLK	Transmit clock	12	output	input	TP5
COL	Collision detection	18	output	input	TP1
CRS	Carrier sense	19	output	input	-
RX_DV	Receive data valid	8	output	input	TP2
RX_ER	Receive error	10	GND	input	-
RXD3	Receive data bit 3	4	output	input	TP13
RXD2	Receive data bit 2	5	output	input	TP12
RXD1	Receive data bit 1	6	output	input	TP11
RXD0	Receive data bit 0	7	output	input	TP4
RX_CLK	Receive clock	9	output	input	TP3
MDIO	Data I/O		Bi-directional	Bi-directional	-
MDC	Clock		input	input	-

VCC		1, 20, 21, 40	No connection	VCC (+5V)	
GND		22 - 39	GND	GND	TP14, TP19

The KSZ8463MLI does not provide the RX_ER signal in PHY mode operation and the TX_ER signal in MAC mode operation. Normally, RX_ER indicates a receive error coming from the physical layer device and TX_ER indicates a transmit error from the MAC device. Since the switch filters error frames, these MII error signals are not used by the KSZ8463MLI. So, for PHY mode operation, if the device interfacing with the KSZ8463MLI has an RX_ER input pin, it needs to be tied low. And, for MAC mode operation, if the device interfacing with the KSZ8463MLI has a TX_ER input pin, it also needs to be tied low.

3.3.2 RMII Port Configuration (KSZ8463RLI)

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). RMII provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports data rate either 10Mbps or 100Mbps.
- Uses a single 50 MHz clock reference (provided internally or externally) for both transmit and receive data.
- Provides independent 2-bit wide transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

As shown in Table 3, JP28 is used for enabling or disabling the generation of 50MHz reference clock from the REFCLK_O pin of the KSZ8463RLI. Register CFGR bit [3] is used to select internal or external reference clock. Internal reference clock means that the clock for the RMII interface will be provided by the KSZ8463RLI internally and the REFCLK_I (pin 27) is unconnected. For the external reference clock, the clock will provide to KSZ8463RLI via REFCLK_I (pin 27).

CFGR (0x0D8) Bit 3	**JP28 Setting** (EN_REFCLKO pin)	**Clock Source**	**Note**
1 (ext 50MHz)	Pins 2-3 closed (EN_REFCLKO = 0)	External 50MHz OSC input to REFCLK_I	EN_REFCLKO = “0” to Disable REFCLK_O for better EMI
1 (ext 50MHz)	Pins 1-2 closed (EN_REFCLKO = 1)	REFCLK_O output is feedback to REFCLK_I	EN_REFCLKO = “1” to enable REFCLK_O
0 (int 50MHz)	Pins 1-2 closed (EN_REFCLKO = 1)	Internal clock source REFCLK_I is unconnected	EN_REFCLKO = “1” to enable REFCLK_O
Other settings are not recommended			

Table 4 RMII Clock Setting

The RMII provided by the KSZ8463RLI is connected to the device's third MAC. It complies with the RMII Specification. The following table describes the signals used by the RMII interface. Refer to RMII Specification for full detail on the signal description.

RMII Signal Name	RMII Signal Description	Pin number on MII connectors	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Test Points
REFCLK	Synchronous 50 MHz clock reference for receive, transmit and control interface	12	Input	Input or Output	TP5
CRS_DV	Carrier sense/ Receive data valid	8	Output	Input	TP6
RXD0	Receive data bit 0	7	Output	Input	TP4
RXD1	Receive data bit 1	6	Output	Input	TP11
TX_EN	Transmit enable	13	Input	Output	TP6
TXD0	Transmit data bit 0	14	Input	Output	TP7
TXD1	Transmit data bit 1	15	Input	Output	TP16
RX_ER	Receive error	10	Output	Input or not required	TP15

Table 5 RMII Signal Description

The KSZ8463RLI filters error frames, and thus does not implement the RX_ER output signal. To detect error frames from RMII PHY devices, the TX_ER input signal of the KSZ8463RLI is connected to the RX_ER output signal of the RMII PHY device.

Collision detection is implemented in accordance with the RMII Specification.

In RMII mode, tie MII signals (TXD [3:2], RXD [3:2] and TX_ER) to ground if they are not used.

The KSZ8463RLI can interface either RMII PHY or RMII MAC device. The RMII MAC device allows two KSZ8463RLI devices to be connected back-to-back.

3.4 GPIO pins

KSZ8463MLI/RLI chip has up to 12 General Purpose I/O (GPIO) pins which are available on the evaluation board at connectors J15 and J16. The KSZ8463RLI device has all 12 GPIO pins available. Three GPIO pins of the KSZ8463MLI device are shared with Port1/2 LED activity signals and are user programmable. By default the LED signals are enabled, therefore 9 GPIO pins are available. If more than 9 GPIO pins are required, the user needs to program IOMXSEL register (0x0D6) as follows:

IOMXSEL register (0x0D6)	Description	Setting
Bit 10	Selection of P2LED1 or GPIO9	1 = This pin is used for P2LED1 (default) 0 = This pin is used for GPIO9
Bit 9	Selection of P2LED0 or GPIO10	1 = This pin is used for P2LED0 (default) 0 = This pin is used for GPIO10
Bit 8	Selection of P1LED1 or GPIO7	1 = This pin is used for P1LED1 (default) 0 = This pin is used for GPIO7

Table 6 GPIO pin selection for KSZ8463MLI

GPIO signals are on the odd numbered pins of connectors J15 and J16. All even numbered pins are GND connections. GPIO7, 9 and 10 pins are connected to jumpers JP36, 37 and 38 respectfully.

For the KSZ8463RLI device, pins 1 and 2 of all three jumpers need to be closed. In case of KSZ8463MLI, GPIO7, 9 and 10 are Port1/2 LED activity signals by default and no strapping is needed. If the user enables GPIO functionality instead, pins 2 and 3 of the corresponding jumpers have to be closed.

The GPIO pins can be used for any general purpose I/O as well as to support IEEE1588 PTP functionality.

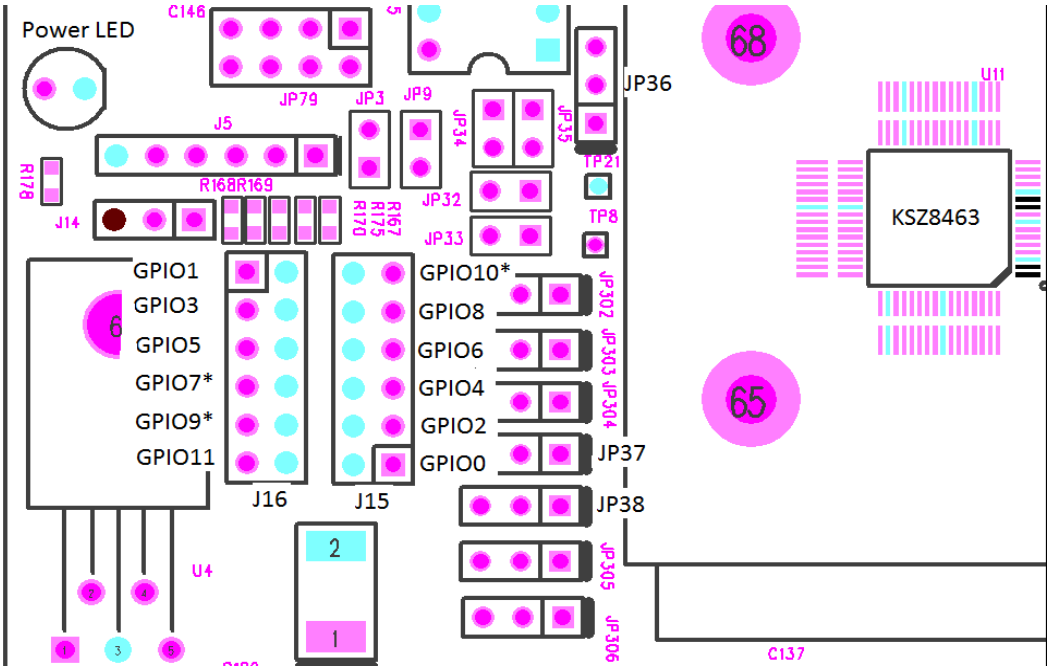

Figure 3 GPIO Connectors and Related Jumper Locations

3.5 10/100 Ethernet PHY Ports

There are two 10/100 Ethernet PHY ports on the KSZ8463MLI/RLI evaluation board. The ports can be connected to an Ethernet traffic generator or analyzer via standard RJ-45 connectors using CAT-5 cables. Each port can be used as either an uplink or downlink. Both ports support auto MDI/MDI-X, eliminating the need for cross-over cables.

Transformers are utilized for proper interfacing to an Ethernet network. In addition, at component locations D5 thru D12 provisions are made for installation of over voltage protection devices to protect the KSZ8463MLI/RLI device in the event of an over voltage condition. The board will have one set installed.

3.6 100FX Fiber Port Option

There are two 100FX PHY ports on the KSZ8463MLI/RLI evaluation board, which are not populated with necessary components. The ports can be connected to an Ethernet traffic generator or analyzer via fiber transceiver and fiber cable. In 100BASE-FX operation, both fiber signal detect input FXSD1 and FXSD2 are usually connected to the fiber transceiver SD (signal detect) output pin. The fiber signal detect threshold is set to 1.7V internally, When FXSD is less than the threshold, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD is over the threshold, the fiber signal is detected. To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD pin's input voltage threshold.

Alternatively, the designer may choose not to implement the FEF feature. In this case, the FXSD input pin is tied high to force 100BASE-FX mode.

3.7 LED Indicators

The KSZ8463MLI/RLI evaluation board provides two LEDs (PxLED1, PxLED0) for each PHY port. The LED indicators are programmable to four different states. LED mode is selected through bits [12:11] of the SGCR7 register (0x00E). The status of the current LED settings are available in bits [9:8] of the same register.

The LED mode definitions are specified in Table 7. See **Error! Reference source not found.** for the LEDs' orientation on the KSZ8463MLI/RLI evaluation board in the power supply section.

SGCR7 Control Register (@0x00E) Bit[12:11] Write, Bit[9:8] Read			
00	**01**	**10**	**11**
PxLED1 = Speed	PxLED1 = Active	PxLED1 = Duplex	PxLED1 = Duplex
PxLED0 = Link/Active	PxLED0 = Link	PxLED0 = Link/Active	PxLED0 = Link

Table 7 LED Functions

The KSZ8463MLI/RLI evaluation board also has a power LED (D3) for the 3.3V power supply. When D3 is illuminated, the board's 3.3V power supply is "on".

The activity LED indicators for Port-1 and Port-2 are powered by VDD_IO, which can be set to 3.3V, 2.5V or 1.8V. In the case of 2.5V and 1.8V selection, these LED indicators will be dimly lit or not illuminated because of inadequate voltage across the LED.

3.8 List of Jumpers and Connectors

Jumper	Description	Setting
JP2	PWRDN Chip Power-down	Place Jumper for full chip power-down
JP3, 9	Factory Usage	Install no jumpers
JP10, 11	Power selection for the Fiber module	Leave open when no Fiber Module present
JP27	MII bypass	Pins 1-2 closed: Enable MII bypass mode Pins 2-3 closed: MII PHY mode normal operation
JP28	Enable RMII mode reference clock output from REFCLK_O pin	Pins 1-2 closed: Enable Pins 2-3 closed: Disable

JP32, 33	Enable MDIO interface through MII connector	Place both jumpers to connect MDIO signals from MII connector to KSZ8463MLI/RLI serial port.
JP34, 35	KSZ8463MLI/RLI serial port connections	Place both jumpers for USB port access and SPI interface
JP36-38	GPIO7, GPIO9 and GPIO10 pin source selection on GPIO Headers	Pins 1-2 closed for KSZ8463RLI Pins 2-3 closed for KSZ8463MLI
JP77, 78	FXSD1, FXSD2 Fiber signal detect input for Port 1 and Port 2 (not used)	Pins 1-2 closed: FX mode Pins 2-3 closed: TX mode
JP79	Enable USB controller interface	Close pins 1-2, 3-4, 5-6 and 7-8 to connect USB controller to serial bus
JP301-305	Strapping options	See Table 1
JP400	5V DC input selection	See Table 2
JP403-406	Power-supply strapping options	See Table 2

Table 8 List of Jumpers and Connectors

3.9 Board Layout

The layout of the board is shown in Figure 3. The key areas are indicated.

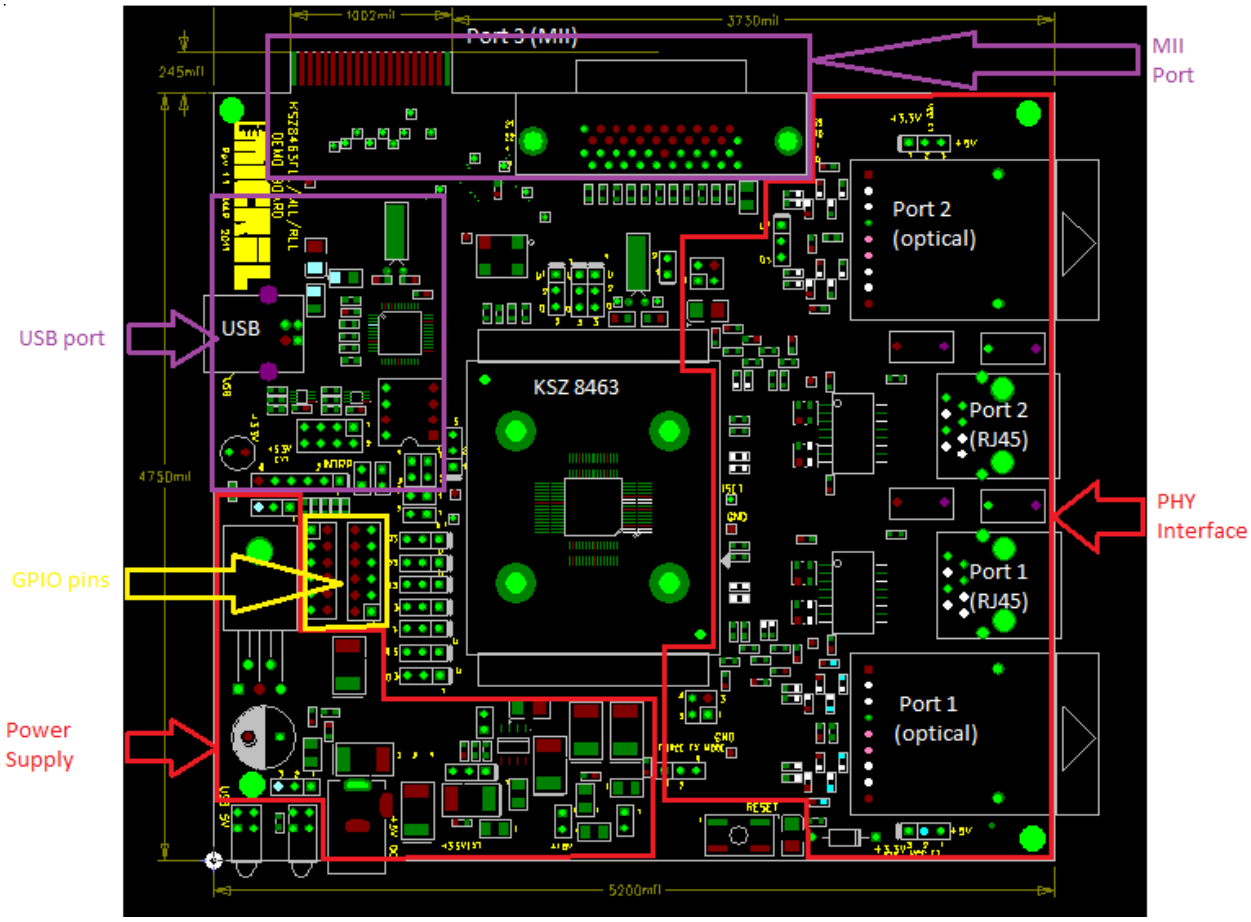

Figure 4 Topside Layout of the Board

The KSZ8463MLI/RLI Evaluation board together with the KSZ9692PB SOC provides a complete evaluation platform for the IEEE1588 PTP functionality. In this setup, Port 3 of the KSZ8463 evaluation board is configured in PHY mode and connected to the SOC board through its MII port. In addition to the MII connection, the SOC accesses the KSZ8463 through the SPI port. An interrupt line is also used for PTP software functionality. For more details on this configuration, refer to the KSZ8463MLI Evaluation Kit User Guide.

4 Using the KSZ8463MLI/RLI Evaluation Board

The Evaluation Kit is intended to provide a platform that enables designers to investigate and evaluate the capabilities of the KSZ8463 device. It is not intended to be a complete development system to be used for an entire product design effort.

5 Reference Documents

KSZ8463MLI/RLI Datasheet (Contact Micrel for latest Datasheet)
KSZ8463MLI/RLI Evaluation Board Schematic (Contact Micrel for latest Schematic)
KSZ8463MLI/RLI Evaluation Board Gerber files
IEEE802.3 Specification
RMII Specification by RMII Consortium
KSZ8463MLI Evaluation Kit User Guide

6 Revision History

Revision	Date	Summary of Changes
1.00	06/16/11	- Initial Release
1.01	08/30/11	- Removed eval kit information
1.02	09/19/11	- Updated text. - Added new board Figure 1.
1.03	09/23/11	- Changed MLLRLL to MLI/RLI, MLL to MLI, RLL to RLI

© Micrel, Inc. 2011
All rights reserved

Micrel is a registered trademark of Micrel and its subsidiaries in the United States and certain other countries. All other trademarks are the property of their respective owners.

The information furnished by Micrel in this datasheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer. Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is at Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.