8-Channel DAS with 16-Bit, Bipolar Input, Simultaneous Sampling ADC

Data Sheet

AD7606-EP

FEATURES

- 8 simultaneously sampled inputs
- True bipolar analog input ranges: ±10 V, ±5 V
- Single 5 V analog supply and 2.3 V to 5.25 V V_{DRIVE}
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - Second-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - 16-bit ADC with 150 kSPS on all channels
  - Oversampling capability with digital filter
- Flexible parallel/serial interface
  - SPI/QSPI™/MICROWIRE™/DSP compatible
- Performance
  - 7 kV ESD rating on analog input channels
  - 95.5 dB SNR, −107 dB THD
  - ±0.5 LSB INL, ±0.5 LSB DNL
  - Low power: 100 mW
  - Standby mode: 25 mW
- 64-lead LQFP package

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range −55°C to +125°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Power-line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

FUNCTIONAL BLOCK DIAGRAM

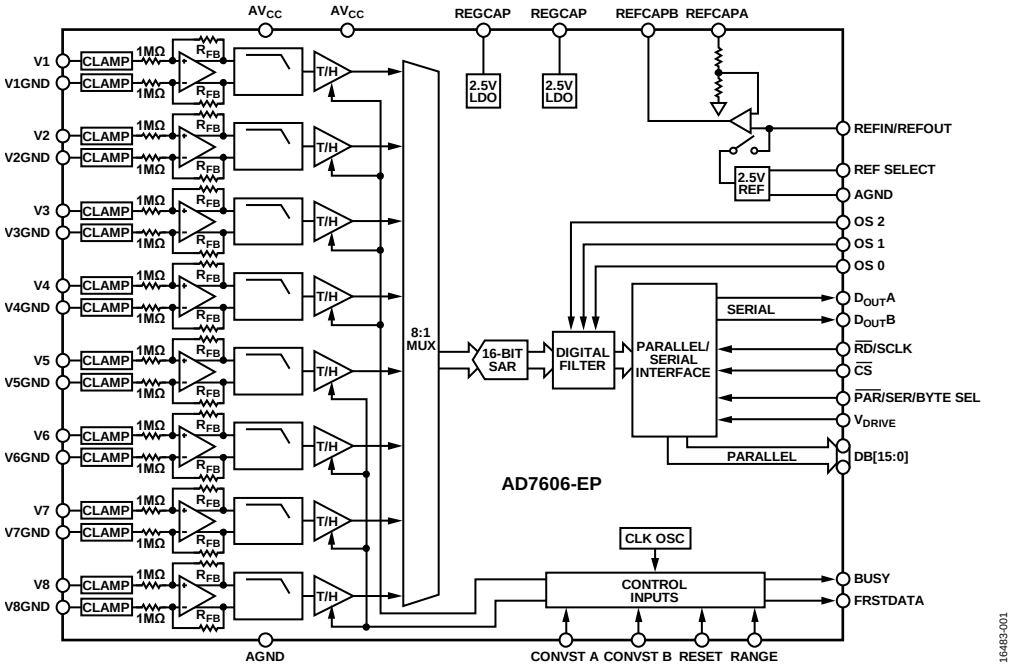

Figure 1.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

6/2018—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7606-EP[1] is a 16-bit, simultaneous sampling, analog-to-digital, data acquisition system (DAS) with eight channels. The device contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, a 16-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

The AD7606-EP operates from a single +5 V supply and can accommodate ±10 V and ±5 V true bipolar input signals while sampling at throughput rates up to 150 kSPS for all channels.

The input clamp protection circuitry can tolerate voltages up to ±16.5 V. The AD7606-EP has 1 MΩ analog input impedance regardless of sampling frequency. The single-supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies. The AD7606-EP antialiasing filter has a 3 dB cutoff frequency of 23 kHz. The flexible digital filter is pin driven, yields improvements in SNR, and reduces the 3 dB bandwidth.

Additional application and technical information can be found in the AD7606 data sheet.

[1] Protected by US Patent Number 8,072,360.

SPECIFICATIONS

Reference voltage (V_{REF}) = 2.5 V external/internal, AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, sampling frequency (f_{SAMPLE}) = 150 kSPS, T_A = −55°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	Input frequency (f_{IN}) = 1 kHz sine wave, unless otherwise noted				
Signal-to-Noise Ratio (SNR)[1, 2]	Oversampling by 16, ±10 V range, f_{IN} = 130 Hz	93	95.5		dB
	Oversampling by 16, ±5 V range, f_{IN} = 130 Hz	92	94.5		dB
	No oversampling, ±10 V range	87.5	90		dB
	No oversampling, ±5 V range	86.5	89		dB
Signal-to-(Noise + Distortion) (SINAD)[1]	No oversampling, ±10 V range	87	90		dB
	No oversampling, ±5 V range	86	89		dB
Dynamic Range	No oversampling, ±10 V range		90.5		dB
	No oversampling, ±5 V range		90		dB
Total Harmonic Distortion (THD)[1]			−107	−93	dB
Peak Harmonic or Spurious Noise (SFDR)[1]			−108		dB
Intermodulation Distortion (IMD)[1]	Tone frequencies = 1 kHz and 1.1 kHz				
Second-Order Terms			−110		dB
Third-Order Terms			−106		dB
Channel-to-Channel Isolation[1]	f_{IN} on unselected channels up to 160 kHz		−95		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±10 V range		23		kHz
	−3 dB, ±5 V range		15		kHz
	−0.1 dB, ±10 V range		10		kHz
	−0.1 dB, ±5 V range		5		kHz
Group Delay Time ($t_{GROUP\ DELAY}$)	±10 V range		11		µs
	±5 V range		15		µs
DC ACCURACY					
Resolution	No missing codes	16			Bits
Differential Nonlinearity[1]			±0.5	±0.99	LSB[3]
Integral Nonlinearity[1]			±0.5	±2	LSB[3]
Total Unadjusted Error (TUE)	±10 V range		±6		LSB[3]
	±5 V range		±12		LSB[3]
Positive Full-Scale Error[1, 4]	External reference		±8	±34	LSB[3]
	Internal reference		±8		LSB[3]
Positive Full-Scale Error Drift	External reference		±2		ppm/°C
	Internal reference		±7		ppm/°C
Positive Full-Scale Error Matching[1]	±10 V range		5	32	LSB[3]
	±5 V range		16	40	LSB[3]
Bipolar Zero Code Error[1, 5]	±10 V range		±1	±8	LSB[3]
	± 5 V range		±3	±14	LSB[3]
Bipolar Zero Code Error Drift	±10 V range		10		µV/°C
	± 5 V range		5		µV/°C
Bipolar Zero Code Error Matching[1]	±10 V range		1	8	LSB[3]
	±5 V range		6	22	LSB[3]
Negative Full-Scale Error[1, 4]	External reference		±8	±34	LSB[3]
	Internal reference		±8		LSB[3]
Negative Full-Scale Error Drift	External reference		±4		ppm/°C
	Internal reference		±8		ppm/°C
Negative Full-Scale Error Matching[1]	±10 V range		5	32	LSB[3]
	±5 V range		16	40	LSB[3]

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT					
Input Voltage Ranges	RANGE = 1			±10	V
	RANGE = 0			±5	V
Analog Input Current	10 V, see Figure 11		5.4		µA
	5 V, see Figure 11		2.5		µA
Input Capacitance[6]			5		pF
Input Impedance			1		MΩ
REFERENCE INPUT AND OUTPUT					
Reference Input Voltage Range		2.475	2.5	2.525	V
DC Leakage Current				±1	µA
Input Capacitance[6]	REF SELECT = 1		7.5		pF
Reference Output Voltage	REFIN/REFOUT		2.49/ 2.505		V
Reference Temperature Coefficient			±15		ppm/°C
LOGIC INPUTS					
Input High Voltage (V_{INH})		0.7 × V_{DRIVE}			V
Input Low Voltage (V_{INL})				0.3 × V_{DRIVE}	V
Input Current (I_{IN})				±2	µA
Input Capacitance (C_{IN})[6]			5		pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	Source current (I_{SOURCE}) = 100 µA	V_{DRIVE} − 0.2			V
Output Low Voltage (V_{OL})	Sink current (I_{SINK}) = 100 µA			0.2	V
Floating State Leakage Current			±1	±20	µA
Floating State Output Capacitance[6]			5		pF
Output Coding			Twos complement		
CONVERSION RATE					
Conversion Time	All eight channels included, see Table 2		4.5		µs
Track-and-Hold Acquisition Time			1.5		µs
Throughput Rate	Per channel, all eight channels included			150	kSPS
POWER REQUIREMENTS					
AV_{CC}		4.75		5.25	V
V_{DRIVE}		2.3		5.25	V
Total Current (I_{TOTAL})	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode (Static)			16	22	mA
Normal Mode (Operational)[7]	f_{SAMPLE} = 150 kSPS		20	27	mA
Standby Mode			5	8	mA
Shutdown Mode			2	7	µA
Power Dissipation					
Normal Mode (Static)			80	115.5	mW
Normal Mode (Operational)[7]	f_{SAMPLE} = 150 kSPS		100	142	mW
Standby Mode			25	42	mW
Shutdown Mode			10	36.8	µW

[1] See the Terminology section in the AD7606 datasheet.
[2] This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel mode with V_{DRIVE} = 5 V, SNR typically reduces by 1.5 dB and THD by 3 dB.
[3] LSB means least significant bit. With ±5 V input range, 1 LSB = 152.58 µV. With ±10 V input range, 1 LSB = 305.175 µV.
[4] These specifications include the full temperature range variation and contribution from the internal reference buffer but do not include the error contribution from the external reference.
[5] Bipolar zero code error is calculated with respect to the analog input voltage.
[6] Sample tested during initial release to ensure compliance.
[7] Operational power and current figure includes contribution when running in oversampling mode.

TIMING SPECIFICATIONS

AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, V_{REF} = 2.5 V external reference and internal reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Sample tested during initial release to ensure compliance. All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.

Table 2.

	Limit at T_{MIN}, T_{MAX}							
	0.1 × V_{DRIVE} and 0.9 × V_{DRIVE} Logic Input Levels			0.3 × V_{DRIVE} and 0.7 × V_{DRIVE} Logic Input Levels				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Description**
PARALLEL/SERIAL/BYTE MODE								
t_{CYCLE}								1/throughput rate
			6.65			6.65	µs	Parallel mode, reading during or after conversion; or serial mode: V_{DRIVE} = 3.3 V to 5.25 V, reading during a conversion using D_{OUT}A and D_{OUT}B lines
						11.1	µs	Serial mode reading after a conversion; V_{DRIVE} = 2.7 V
			11.4			12.4	µs	Serial mode reading after a conversion; V_{DRIVE} = 2.3 V, D_{OUT}A and D_{OUT}B lines
t_{CONV}								Conversion time
	4.1	4.5	5	4.1	4.5	5	µs	Oversampling off
	9.6		11.7	9.6		11.7	µs	Oversampling by 2
	20.5		25	20.5		25	µs	Oversampling by 4
	42		52	42		52	µs	Oversampling by 8
	86		105	86		105	µs	Oversampling by 16
	173		212	173		212	µs	Oversampling by 32
	347		424	347		424	µs	Oversampling by 64
t_{RESET}	50			50			ns	RESET high pulse width
t_1			40			45	ns	CONVST x high to BUSY high
t_2	25			25			ns	Minimum CONVST x low pulse
t_3	25			25			ns	Minimum CONVST x high pulse
t_4	0			0			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
t_5 [1]			0.5			0.5	ms	Maximum delay allowed between CONVST A, CONVST B rising edges
t_6			25			25	ns	Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge
t_7	25			25			ns	Minimum delay between RESET low to CONVST x high

[1] The delay between the CONVST x signals was measured as the maximum time allowed while ensuring a <10 LSB performance matching between channel sets.

Timing Diagrams

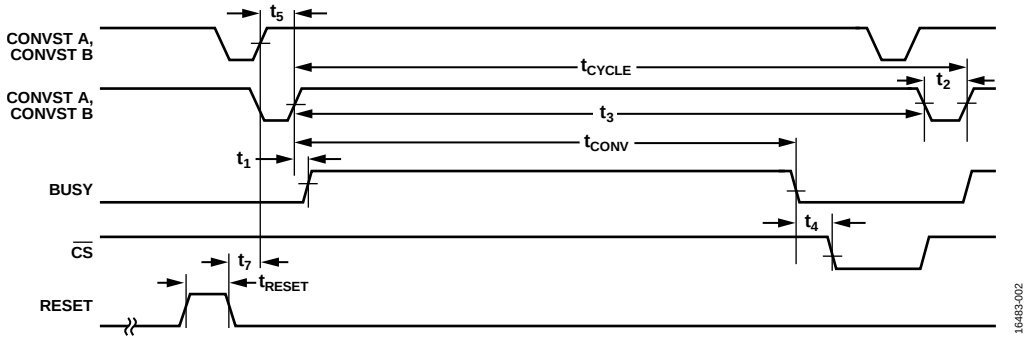

Figure 2. CONVST x Timing—Reading After a Conversion

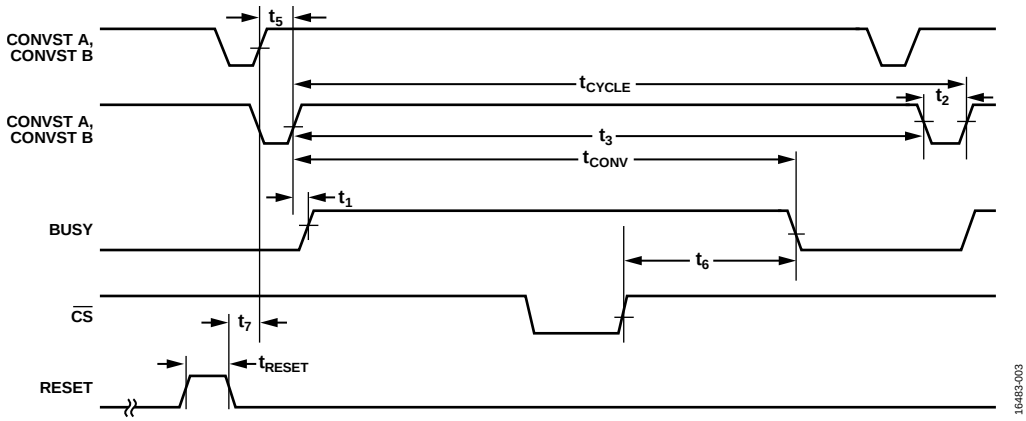

Figure 3. CONVST x Timing—Reading During a Conversion

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±16.5 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Soldering Reflow Temperature	260 (0)°C
Electrostatic Discharge (ESD)	
All Pins Except Analog Inputs	2 kV
Analog Input Pins Only	7 kV

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
ST-64-2[1]	45	11	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

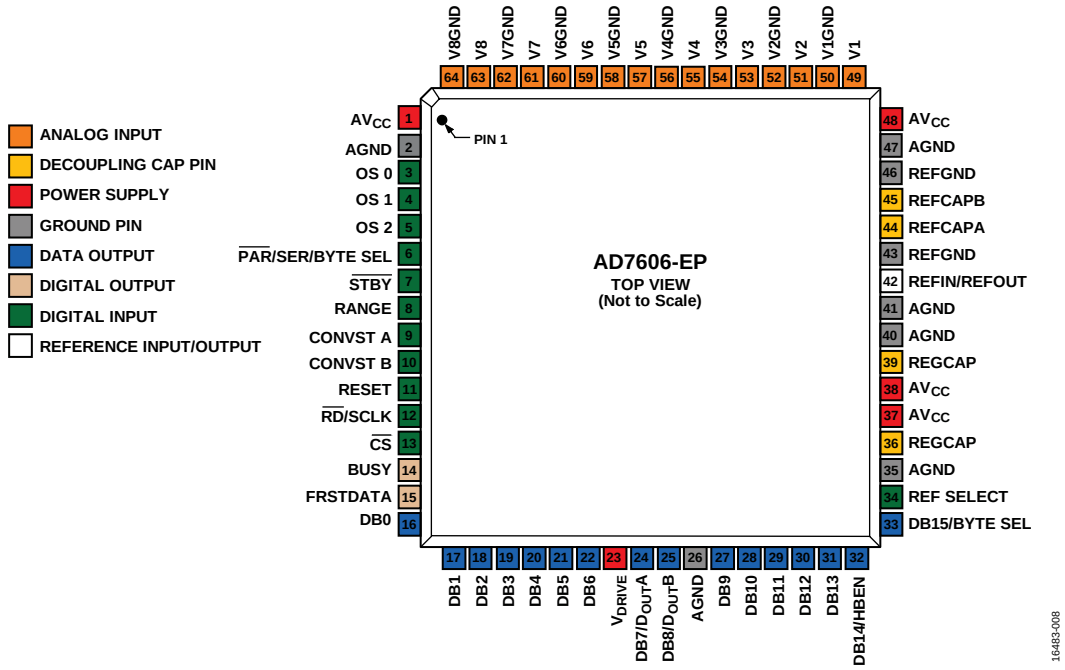

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
1, 37, 38, 48	P	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. Decouple these supply pins to AGND.
2, 26, 35, 40, 41, 47	P	AGND	Analog Ground. These pins are the ground reference points for all analog circuitry on the AD7606-EP. Refer all analog input signals and external reference signals to these pins. Connect the six AGND pins to the AGND plane of a system.
3, 4, 5	DI	OS 0, OS 1, OS 2	Oversampling Mode Pins. Logic inputs. These inputs are used to select the oversampling ratio. OS 2 is the most significant bit (MSB) control bit, and OS 0 is the least significant bit (LSB) control bit. See the Oversample Bit Decoding table and Digital Filter section in the AD7606 data sheet for more details about the logic states and oversampling mode of operation.
6	DI	$\overline{PAR}$/SER/ BYTE SEL	Parallel/Serial/Byte Interface Selection Input. Logic input. See the Interface Mode Selection table in the AD7606 data sheet. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. Parallel byte interface mode is selected when this pin is logic high and DB15/BYTE SEL is logic high. In serial mode, the $\overline{RD}$/SCLK pin functions as the serial clock input. The DB7/D_{OUT}A pin and the DB8/D_{OUT}B pin function as serial data outputs. When the serial interface is selected, tie the DB[15:9] and DB[6:0] pins to ground. In byte mode, DB15, in conjunction with $\overline{PAR}$/SER/BYTE SEL, is used to select the parallel byte mode of operation. DB14 is used as the HBEN pin. DB[7:0] transfer the 16-bit conversion results in two $\overline{RD}$ operations, with DB0 as the LSB of the data transfers.
7	DI	$\overline{STBY}$	Standby Mode Input. This pin is used to place the AD7606-EP into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin. When in standby mode, all circuitry, except the on-chip reference, regulators, and regulator buffers, is powered down. When in shutdown mode, all circuitry is powered down. See the Power-Down Mode Selection table in the AD7606 data sheet.

Pin No.	Type[1]	Mnemonic	Description
8	DI	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended for fast throughput rate applications. See the Analog Input section in the AD7606 data sheet for more information.
9, 10	DI	CONVST A, CONVST B	Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together, and a single convert start signal can be applied. Alternatively, CONVST A can be used to initiate simultaneous sampling: V1, V2, V3, and V4 for the AD7606-EP. CONVST B can be used to initiate simultaneous sampling on the other analog inputs: V5, V6, V7, and V8 for the AD7606-EP. This is possible only when oversampling is not switched on. When the CONVST A or CONVST B pin transitions from low to high, the front-end, track-and-hold circuitry for the respective analog inputs is set to hold.
11	DI	RESET	Reset Input. When set to logic high, the rising edge of RESET resets the AD7606-EP. The device receives a RESET pulse directly after power-up. The RESET high pulse is typically 50 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers reset to all zeros.
12	DI	$\overline{RD}$/SCLK	Parallel Data Read Control Input When Parallel Interface Selected ($\overline{RD}$)/Serial Clock Input When Serial Interface Selected (SCLK). When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{CS}$ falling edge takes the $D_{OUT}A$ and $D_{OUT}B$ data output lines out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the $D_{OUT}A$ and $D_{OUT}B$ serial data outputs. See the Conversion Control section in the AD7606 data sheet for more information.
13	DI	$\overline{CS}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the DB[15:0] output bus is enabled, and the conversion result is output on the parallel data bus lines. In serial mode, $\overline{CS}$ is used to frame the serial read transfer and clock out the MSB of the serial output data.
14	DO	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read after t_4. Any data read while BUSY is high must be completed before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high.
15	DO	FRSTDATA	Digital Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel, byte, or serial interface. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{CS}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{RD}$ corresponding to the result of V1 then sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the next falling edge of $\overline{RD}$. In serial mode, FRSTDATA goes high on the falling edge of $\overline{CS}$ because this pin clocks out the MSB of V1 on $D_{OUT}A$. FRSTDATA returns low on the 16th SCLK falling edge after the $\overline{CS}$ falling edge. See the Conversion Control section in the AD7606 data sheet for more information.
22 to 16	DO	DB[6:0]	Parallel Output Data Bits, DB6 to DB0. When $\overline{PAR}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input and output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB6 to DB0 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, tie these pins to AGND. When operating in parallel byte interface mode, DB[7:0] outputs the 16-bit conversion result in two $\overline{RD}$ operations. DB7 (Pin 24) is the MSB and DB0 is the LSB. See Pin 24 description for additional information.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage (2.3 V to 5.25 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, digital signal processor and field programmable gate array).

Pin No.	Type[1]	Mnemonic	Description
24	DO	DB7/D_{OUT}A	Parallel Output Data Bit 7 (DB7)/Serial Interface Data Output Pin (D_{OUT}A). When $\overline{PAR}$/SER/$\overline{BYTE}$ SEL = 0, this pin acts as a three-state parallel digital input and output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB7 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, this pin functions as D_{OUT}A and outputs serial conversion data. When operating in parallel byte mode, DB7 is the MSB of the byte. See the Conversion Control section in the AD7606 data sheet for more information.
25	DO	DB8/D_{OUT}B	Parallel Output Data Bit 8 (DB8)/Serial Interface Data Output Pin (D_{OUT}B). When $\overline{PAR}$/SER/$\overline{BYTE}$ SEL = 0, this pin acts as a three-state parallel digital input and output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB8 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, this pin functions as D_{OUT}B and outputs serial conversion data. See the Conversion Control section in the AD7606 data sheet for more information.
31 to 27	DO	DB[13:9]	Parallel Output Data Bits, DB13 to DB9. When $\overline{PAR}$/SER/$\overline{BYTE}$ SEL = 0, these pins act as three-state parallel digital input and output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB13 to DB9 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, tie these pins to AGND.
32	DO/DI	DB14/HBEN	Parallel Output Data Bit 14 (DB14)/High Byte Enable (HBEN). When $\overline{PAR}$/ SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB14 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the AD7606-EP operates in parallel byte interface mode. In parallel byte mode, the HBEN pin is used to select whether the MSB or the LSB of the conversion result is output first. When HBEN = 1, the MSB is output first, followed by the LSB. When HBEN = 0, the LSB is output first, followed by the MSB. In serial mode, tie this pin to GND.
33	DO/DI	DB15/BYTE SEL	Parallel Output Data Bit 15 (DB15)/Parallel Byte Mode Select (BYTE SEL). See the Interface Mode Selection table in the AD7606 data sheet. When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB15 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, the BYTE SEL pin is used to select between serial interface mode and parallel byte interface mode. When $\overline{PAR}$/SER/ $\overline{BYTE}$ SEL = 1 and DB15/BYTE SEL = 0, the AD7606-EP operates in serial interface mode. When $\overline{PAR}$/SER/ BYTE SEL = 1 and DB15/BYTE SEL = 1, the AD7606-EP operates in parallel byte interface mode.
34	DI	REF SELECT	Internal/External Reference Selection Input. Logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
36, 39	P	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple these output pins separately to AGND using a 1 µF capacitor. The voltage on these pins is in the 2.5 V to 2.7 V range.
42	REF	REFIN/REFOUT	Reference Input (REFIN)/Reference Output (REFOUT). See the Internal/External Reference section in the AD7606 data sheet for more information. The on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to logic low, and an external reference of 2.5 V can be applied to this input. Decoupling is required on this pin for both the internal and external reference options. Apply a 10 µF capacitor from this pin to ground close to the REFGND pins.
43, 46	REF	REFGND	Reference Ground Pins. Connect these pins to AGND.
44, 45	REF	REFCAPA, REFCAPB	Reference Buffer Output Force and Sense Pins. Connect these pins together, and decouple these pins to AGND using a low ESR, 10 µF ceramic capacitor. The voltage on these pins is typically 4.5 V.
49	AI	V1	Analog Input 1. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
50	AI GND	V1GND	Analog Input V1 Ground Pin. Connect all analog input AGND pins to the AGND plane of a system.
51	AI	V2	Analog Input 2. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
52	AI GND	V2GND	Analog Input V2 Ground Pin. Connect all analog input AGND pins to the AGND plane of a system.
53	AI	V3	Analog Input 3. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
54	AI GND	V3GND	Analog Input V3 Ground Pin. Connect all analog input AGND pins to the AGND plane of a system.

Pin No.	Type[1]	Mnemonic	Description
55	AI	V4	Analog Input 4. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
56	AI GND	V4GND	Analog Input V4 Ground Pin. Connect all analog input AGND pins to the AGND plane of a system.
57	AI	V5	Analog Input 5. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
58	AI GND	V5GND	Analog Input V5 Ground Pins. Connect all analog input AGND pins to the AGND plane of a system.
59	AI	V6	Analog Input 6. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
60	AI GND	V6GND	Analog Input V6 Ground Pin. Connect all analog input AGND pins to the AGND plane of a system.
61	AI	V7	Analog Input 7 Pin. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
62	AI GND	V7GND	Analog Input V7 Ground Pin. Connect all analog input AGND pins to the AGND plane of a system.
63	AI	V8	Analog Input 8 Pin. This pin is a single-ended analog input. The RANGE pin determines the analog input range of this channel.
64	AI GND	V8GND	Analog Input V8 Ground Pin. Connect all analog input AGND pins to the AGND plane of a system.

[1] P is power supply, DI is digital input, DO is digital output, REF is reference input and output, AI is analog input, and GND is ground.

TYPICAL PERFORMANCE CHARACTERISTICS

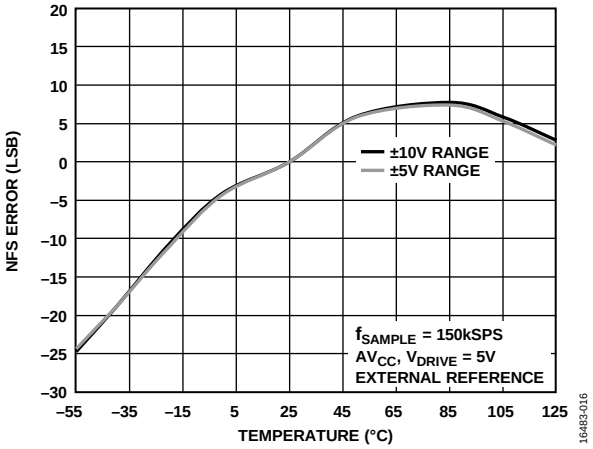

Figure 5. NFS Error vs. Temperature

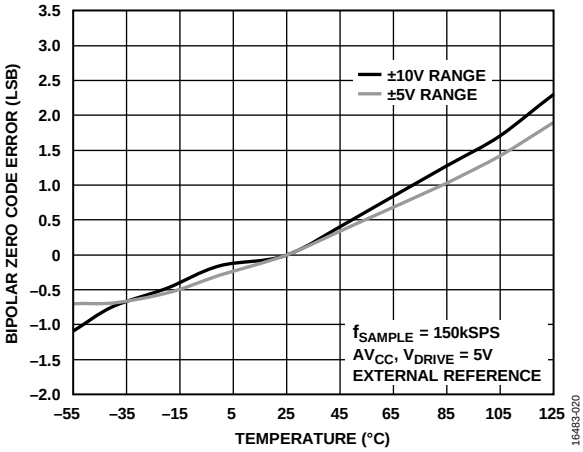

Figure 8. Bipolar Zero Code Error vs. Temperature

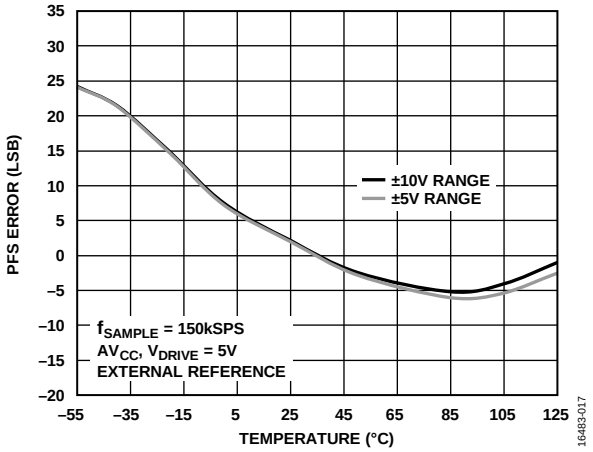

Figure 6. PFS Error vs. Temperature

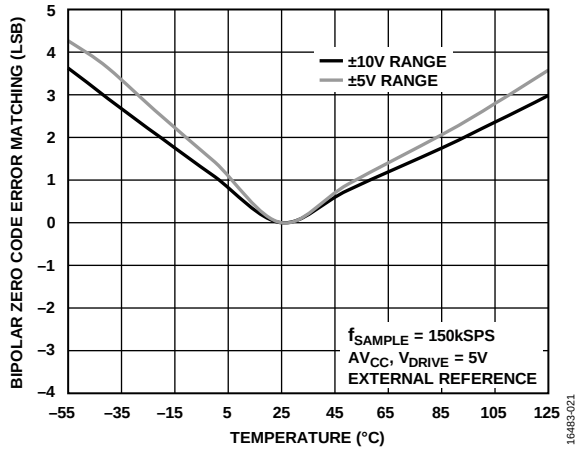

Figure 9. Channel to Channel Bipolar Zero Code Error Matching vs. Temperature

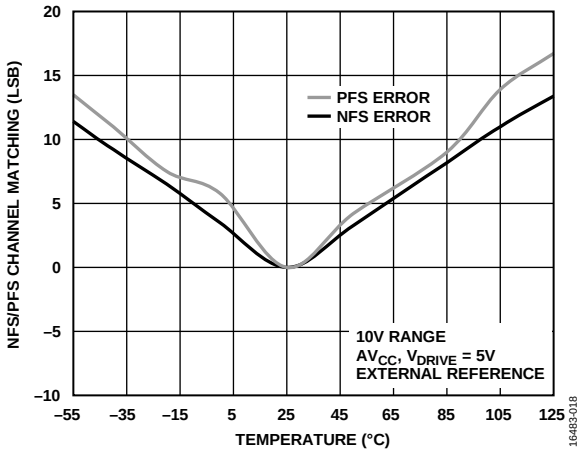

Figure 7. NFS and PFS Channel Matching vs. Temperature

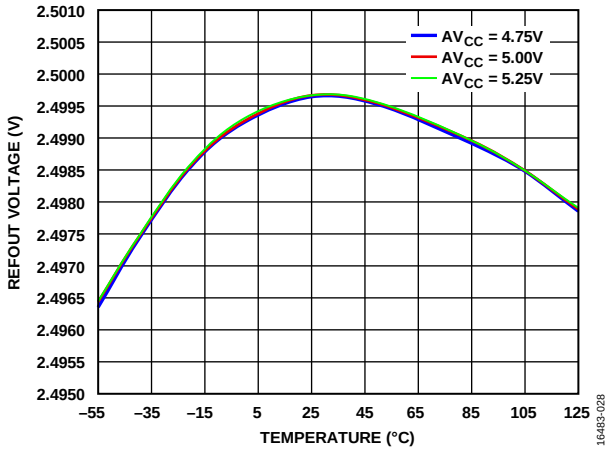

Figure 10. REFOUT Voltage vs. Temperature for Different Supply Voltages

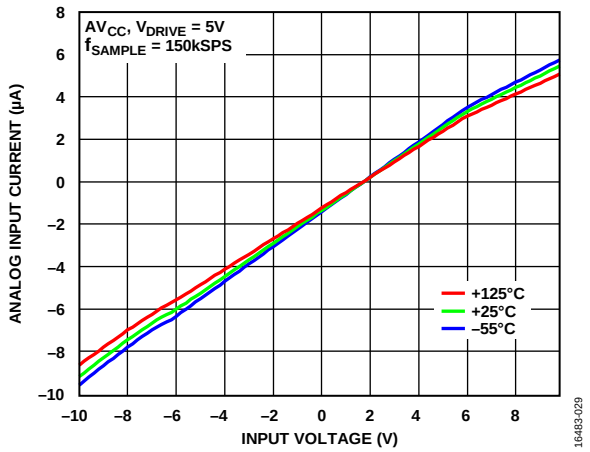

Figure 11. Analog Input Current vs. Input Voltage for Various Temperatures

OUTLINE DIMENSIONS

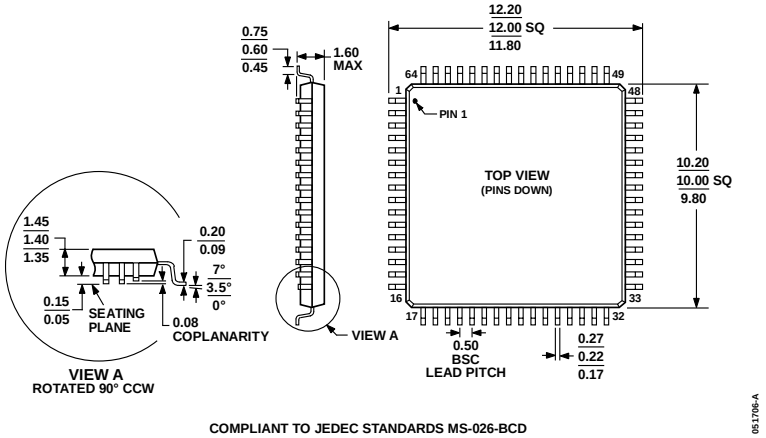

Figure 12. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7606TSTZ-EP	−55°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606TSTZ-EP-RL	−55°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2

[1] Z = RoHS Compliant Part.

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