MachXO2 Product Family Qualification Summary

Lattice Document # 25 – 106923 July 2013

Dear Customer,

Enclosed is Lattice Semiconductor's MachXO2 Product Family Qualification Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice. If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality & Product Development
Lattice Semiconductor Corporation

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1.0 INTRODUCTION

The MachXO2 family of ultra-low power, instant-on, non-volatile PLDs has six devices with densities ranging from 256 to 6864 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic these devices feature Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability and hardened versions of commonly used functions such as SPI controller, I2C controller and timer/counter. These features allow these devices to be used in low cost, high volume consumer and system applications.

The MachXO2 devices are designed on a 65nm non-volatile low power process. The device architecture has several features such as programmable low swing differential I/Os and the ability to turn off I/O banks, on-chip PLLs and oscillators dynamically. These features help manage static and dynamic power consumption resulting in low static power for all members of the family.

The MachXO2 devices are available in three options – ultra low power (ZE) and high performance (HC and HE) devices. The ultra-low power devices are offered in three speed grades -1, -2 and -3, with -3 being the fastest. Similarly, the high-performance devices are offered in three speed grades: -4, -5 and -6, with -6 being the fastest. HC devices have an internal linear voltage regulator which supports external VCC supply voltages of 3.3V or 2.5V. ZE and HE devices only accept 1.2V as the external VCC supply voltage. With the exception of power supply voltage all three types of devices (ZE, HC and HE) are functionally compatible and pin compatible with each other.

The MachXO2 PLDs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5x2.5 mm WLCSP to the 23x23 mm fpBGA. MachXO2 devices support density migration within the same package.

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The MachXO2 family is the third generation FPGA product family and first 65 nm (CS200FL) Flash Technology based product offering. The Lattice Semiconductor MachXO2 FPGA product family qualification efforts are based on the first MachXO2 devices in the family per the Lattice Semiconductor Qualification Procedure, doc#70-100164.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

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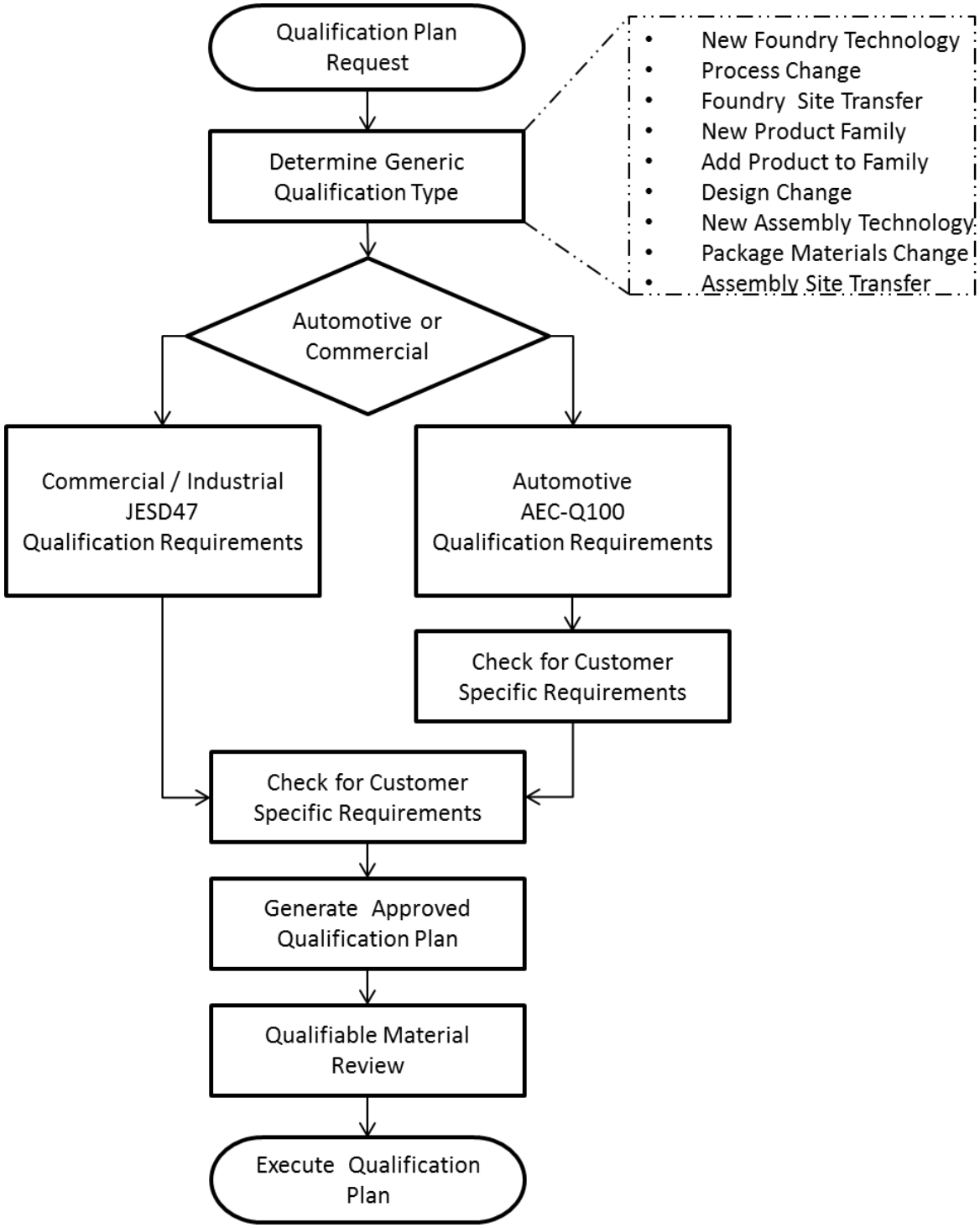
Figure 2.0.1 Lattice Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The MachXO2 Product Family was qualified using the Commercial / Industrial Qualification Option.



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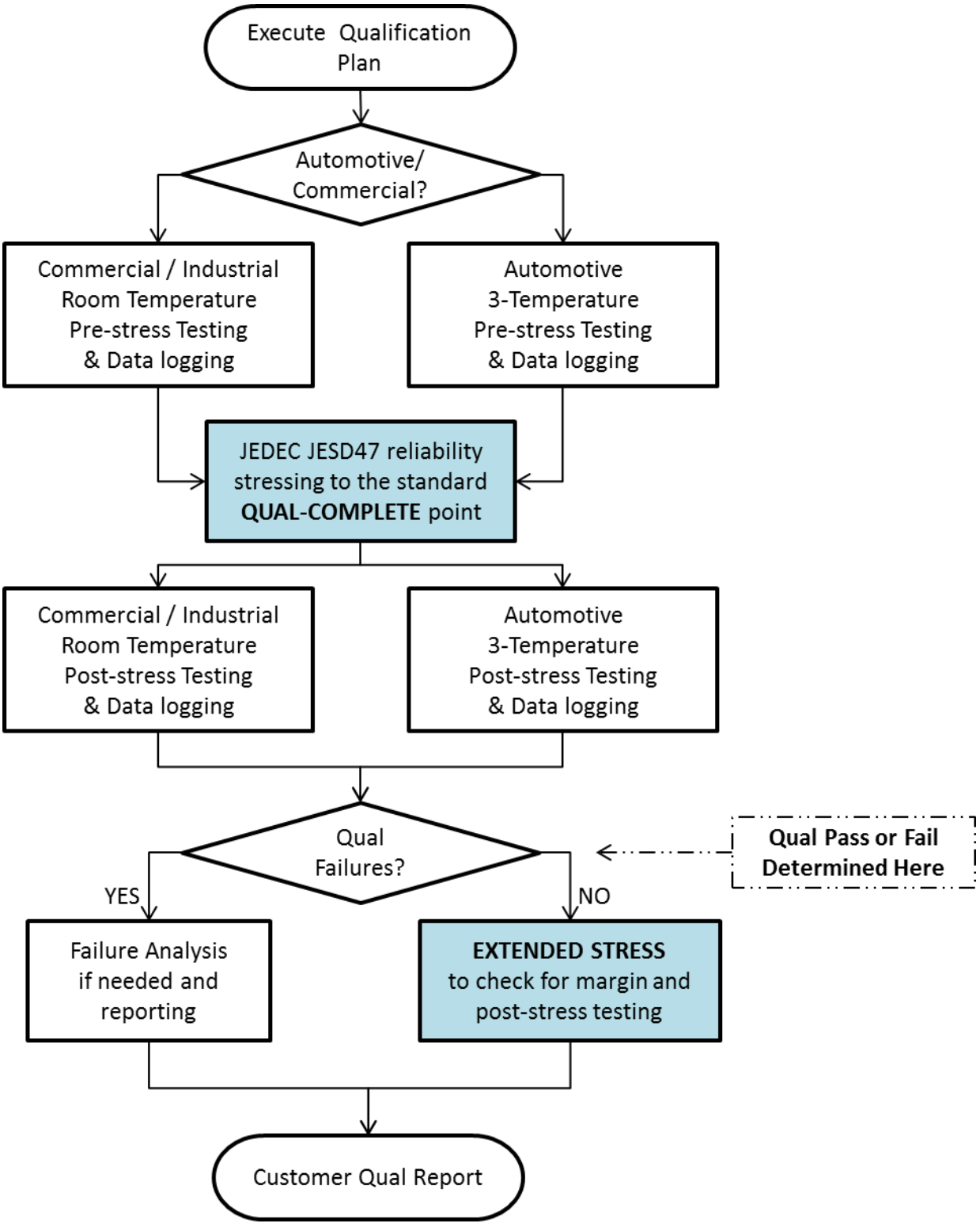

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Table 2.0.2 Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typical)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108C MachXO2	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103C MachXO2	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114E	Human Body Model	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD MM	JESD22-A115C	Machine Model (MM) sweep to 200 volts	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101D	Charged Device model	3 parts/lot 1-2 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78A	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-2 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113F MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104C	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Power Temperature Cycling PTC		(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment with asynchronous power on-off cycling.	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification. This test is required only for Automotive-qualified devices with maximum rated power $\geq$ 1 watt or DTJ $\geq$ 40ºC.
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 264 hrs, 110 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only

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TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typical)	PERFORMED ON
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101B JESD22-A110B	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours Or, Biased to maximum operating Vcc, 2atm. Pressure, 264 hrs, 110 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Ball Shear	Lattice Procedure # 70-104056 # 70-100433	Per Package Type	3 devices per package / 30 balls each unit	Package Qualification

Table 2.0.3 Industry Standard Qualification Testing for WLCSP Packages

STRESS TEST	STANDARD	TEST CONDITIONS	PASS CONDITION	SAMPLE SIZE	Equipment
Surface Mount Preconditioning Pre-BLR test board assembly	JEDEC JESD22-A113F IPC/JEDEC J-STD-020	24 hours 125°C bake; followed by 168 hours 85C/85%RH moisture soak; plus 1x reflow (260C) onto BLR test boards	Daisy chain continuity, Zero fails	25 per lot x 3 lots	Universal Instr. Corp: Vitronics Soltec XPM 1030 Solder Reflow (10 heating, 3 cooling zones)
Slow-Temperature Cycling	JEDEC JESD22-A104D IPC-JEDEC9701A	Condition G, soak mode 2 (-40C to 125C, 7.5 min soak) 1-2 CPH for 3000 cycles	1000 Cycles, Zero fails	25 per lot x 3 lots	Ransco Model# 7102-1
Bend Qualification	JEDEC JESD22-B113A IPC-JEDEC9702	200,000 bends of test boards at 1 to 3 Hz with maximum cross-head displacement of 4 mm	20,000 Bends, Zero fails	36 per lot x 3 lots	Test Resources Model# 1210OCCH-1K-B
Drop Qualification Condition B (Handheld apps)	JEDEC JESD22-B111 IPC-JEDEC9703	1500g drops 0.5 millisecond duration half-sine pulse	30 drops, Zero fails	60 per lot x 3 lots VIP	AVEX Shock Machine Type SM105 Model #MF
Drop Qualification Condition H (Shipping)	JEDEC JESD-B104C IPC-JEDEC9703	2900g drops 0.3 millisecond duration half-sine pulse	30 drops, Zero fails	25	AVEX Shock Machine Type SM105 Model #MF

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3.0 QUALIFICATION DATA MACHXO2 PRODUCT FAMILY

The MachXO2 devices are fabricated at Fujitsu on a 65nm non-volatile low power process, then assembled and tested at ASEM in Malaysia, ASET in Kaohsiung, Taiwan, and UTAC/ NEPES in Singapore. The MachXO2 devices are available in three options – ultra low power (ZE) and high performance (HC and HE) devices. The LCMXO2-1200 is the lead qualification vehicle for this product family.

Product Family: MachXO2
Packages offered: TQFP, µcBGA, csBGA, caBGA, ftBGA, fpBGA, QFN and WLCSP
Process Technology Node: 65 nm Flash

3.1 MachXO2 Product Family Life (HTOL) Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 “Temperature, Bias, and Operating Life”, a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type. The Early Life Failure Rate (ELFR) test uses large samples sizes for a short duration (48 Hours) HTOL stress to determine the infant mortality rate of a device family.

MachXO2 Life Test (HTOL) Conditions:

Devices Stressed: LCMXO2

Pre-conditioning: All Flash cells Program/Erase cycled 10,000 times prior to HTOL stress.

Stress Duration: 48, 168, 500, 1000, 2000 hours.

Stress Conditions: MachXO2 (LCMXO2): HTOL Pattern, Vcc=1.26V, Vccio=3.47V $T_{JUNCTION} = \geq 125°C$

Method: Lattice Document # 87-101943 and JESD22-A108C

The first 3 wafer lots of ELFR & HTOL stressed were **pre-production process development lots**.

Table 3.1.1 MachXO2 Product Family Life Results using **Pre-Production** Wafer Fab Process Development Lots

Product Name	Package	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2-1200ZE	MG132	Lot #1	293*	1_A	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200HE	MG132	Lot #1	300*	0	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200HC	MG132	Lot #1	299*	0	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200ZE	MG132	Lot #2	300*	1_A	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200HE	MG132	Lot #2	300*	0	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200HC	MG132	Lot #2	300*	0	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200ZE	MG132	Lot #3	300*	0	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200HE	MG132	Lot #3	299*	0	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200HC	MG132	Lot #3	300*	0	N/A	N/A	N/A	N/A	N/A
LCMXO2-1200ZE	MG132	Lot #1	58	N/A	0	0	0	N/A	58,000
LCMXO2-1200HE	MG132	Lot #1	59	N/A	0	0	0	N/A	59,000
LCMXO2-1200HC	MG132	Lot #1	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200ZE	TG144	Lot #1	50	N/A	0	0	0	N/A	50,000
LCMXO2-1200HE	TG144	Lot #1	50	N/A	0	0	0	N/A	50,000
LCMXO2-1200HC	TG144	Lot #1	47	N/A	0	0	0_B	N/A	47,000
LCMXO2-1200ZE	MG132	Lot #2	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200HE	MG132	Lot #2	56	N/A	0	0	0	N/A	56,000
LCMXO2-1200HC	MG132	Lot #2	40	N/A	0	0	0	N/A	40,000
LCMXO2-1200ZE	TG144	Lot #2	49	N/A	0	0	0	0_D	98,000
LCMXO2-1200HE	TG144	Lot #2	49	N/A	0	0	0	0	98,000
LCMXO2-1200HC	TG144	Lot #2	47	N/A	0	0	0	0	94,000

Product Name	Package	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2-1200ZE	MG132	Lot #3	59	N/A	0	0	0	N/A	59,000
LCMXO2-1200HE	MG132	Lot #3	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200HC	MG132	Lot #3	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200ZE	TG144	Lot #3	50	N/A	0	0	0	0	100,000
LCMXO2-1200HE	TG144	Lot #3	49	N/A	0	0	1C	0	98,000
LCMXO2-1200HC	TG144	Lot #3	50	N/A	0	0	0	0	100,000

* ELFR units did not receive Flash cell pre-condition cycling prior to stress.
A: Two (2) pre-production ELFR failures due to too-thin ILD0. A pre-production corrective & preventive process change was incorporated and then validated using Flash Extended Endurance, High Temperature Data Retention, and High Temperature Operating Life stresses.
B: FAR#1389: One temperature-sensitive device was a test escape Pre-HTOL stress. Not an HTOL failure. Unit removed from sample size.
C: FAR#1390: One working unit at 1k hr failed for flash “readback. Flash verified as good. Intermittent “Read” circuit. Not able to localize.
D: No FAR. One unit mechanically damaged due to handling. No longer able to retest that device. Unit removed from sample size.

Table 3.1.2 MachXO2 Product Family Life Results Run on **Production-Process** Wafer Fabrication Lots

Product Name	Package	Lot #	Qty	48 Hrs Result	168 Hrs Result	500 Hrs Result	1000 Hrs Result	2000 Hrs Result	Cumulative Hours
LCMXO2-1200ZE	MG132	Lot #6	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200HE	MG132	Lot #6	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200HC	MG132	Lot #6	60	N/A	0	0	0	N/A	60,000
LCMXO2-1200ZE	TG144	Lot #6	48	N/A	0	0	0	N/A	48,000
LCMXO2-1200HE	TG144	Lot #6	49	N/A	0	0	0	N/A	49,000
LCMXO2-1200HC	TG144	Lot #6	50	N/A	0	0	0	N/A	50,000
LCMXO2-7000ZE	FTG256	Lot #1	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HE	FTG256	Lot #1	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HC	FTG256	Lot #1	40*	N/A	0	0	0	0	80,000
LCMXO2-7000ZE	TG144	Lot #1	50	N/A	0	0	0	0	100,000
LCMXO2-7000HE	TG144	Lot #1	48	N/A	0	0	0	0	96,000
LCMXO2-7000HC	TG144	Lot #1	48	N/A	0	0	0	0	96,000
LCMXO2-7000ZE	FTG256	Lot #2	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HE	FTG256	Lot #2	40*	N/A	0	0	0	0	80,000
LCMXO2-7000HC	FTG256	Lot #2	40*	N/A	0	0	0	0	80,000
LCMXO2-7000ZE	TG144	Lot #2	50	N/A	0	0	0	0	100,000
LCMXO2-7000HE	TG144	Lot #2	48	N/A	0	0	0	0	96,000
LCMXO2-7000HC	TG144	Lot #2	48	N/A	0	0	0	0	96,000

* FTG256 packaged units did not receive Flash cell pre-condition cycling prior to stress.

MachXO2 Product Family Life Results Run on Production-Process Wafer Fabrication Lots

MachXO2 Cumulative Life Testing Device Hours = 1,391,000
MachXO2 Cumulative Result = 0 failures at 1000 & 2000 hours
MachXO2 Long Term Failure Rate = 9 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

MachXO2 ELFR (168Hrs) Cumulative Result / Sample Size = 0 / 859
MachXO2 HTOL (1000 Hrs) Cumulative Result / Sample Size = 0 / 859
MachXO2 HTOL (2000 Hrs) Cumulative Result / Sample Size = 0 / 532

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3.2 MachXO2 Product Family High Temperature Retention (HTRX) Data

High Temperature Data Retention (HTRX)

The High Temperature Data Retention test measures the Flash cell reliability while the High Temperature Operating Life test is structured to measure functional operating circuitry failure mechanisms. The High Temperature Data Retention test is specifically designed to accelerate charge gain on to or charge loss off of the floating gates in the device's array. Since the charge on these gates determines the actual pattern and function of the device, this test is a measure of the reliability of the device in retaining programmed information. In High Temperature Data Retention, the Flash cell reliability is determined by monitoring the cell margin after biased static operation at 150°C ambient. Flash cells in the arrays are life tested with half the samples programmed with a checkerboard pattern and half with checkerboard-not patterns. Prior to data retention testing all Flash cells are pre-conditioned with 10,000 program/erase cycles.

MachXO2 Data Retention (HTRX) Conditions:

Stress Duration: 168, 500, 1000 hours.

Temperature: 150°C ambient

Stress Voltage MachXO2: V_{CC}=1.26V/ V_{CCIO}=3.47V

Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A

Table 3.2.1 MachXO2 High Temperature Retention Results

Product Name	Package	Assembler	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	Cumulative Hours
LCMXO2-1200ZE	MG132	ASEM	Lot #3	76	0	0	0	NA	76,000
LCMXO2-1200ZE	MG132	ASEM	Lot #4	26*	0	0	0	NA	26,000
LCMXO2-1200ZE	MG132	ASEM	Lot #4	26*	0	0	0	NA	26,000
LCMXO2-1200ZE	MG132	ASEM	Lot #4	26*	0	0	0	NA	26,000
LCMXO2-1200ZE	MG132	ASEM	Lot #5	80	0	0	0	NA	80,000
LCMXO2-1200ZE	MG132	ASEM	Lot #6	80	0	0	0	0	120,000
LCMXO2-1200ZE	MG132	ASEM	Lot #6	80	0	0	0	0	120,000
LCMXO2-7000ZE	TG144	ASEM	Lot #1	80	0	0	0	0	120,000
LCMXO2-7000ZE	TG144	ASEM	Lot #2	80	0	0	0	0	120,000

* Qual lot #4 includes tunnel oxide (TOX) process splits: nominal, thick and thin TOX respectively. All passed qual.
Note: A detailed MachXO2 Flash Data Retention report is available upon request. Lattice Semiconductor Corp. document #25-106925.

MachXO2 Cumulative HTRX Failure Rate = 0 / 554
MachXO2 Cumulative HTRX Device Hours = 714,000

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3.3 MachXO2 Product Family Flash Endurance Cycling Data

Flash Extended Endurance testing measures the durability of the device through programming and erase cycles. Endurance testing consists of repeatedly programming and erasing all cells in the array at 25°C ambient to simulate programming cycles the user would perform. This test evaluates the integrity of the thin tunnel oxide through which current passes to program the floating gate in each cell of the array.

MachXO2 Flash Extended Endurance Test Conditions:

Stress Duration: 1K, 10K, 20K, 50K, 100K Cycles

Temperature: 25°C ambient

Stress Voltage MachXO2: V_{CC}=1.26V / V_{CCIO}=3.47V

Method: Lattice Document # 70-104633 and JESD22-A117A

Table 3.3.1 MachXO2 Flash Extended Endurance Results

Product Name	Lot #	Qty	Cycling Temp	1K CYC	10K CYC	20K CYC	50K CYC	100K CYC
LCMXO2-1200ZE	Lot #6	54	25C	0	0	0	0	0
LCMXO2-7000ZE	Lot #1	60	25C	0	0	0	0	0
LCMXO2-7000ZE	Lot #2	60	25C	0	0	0	0	0
LCMXO2-256ZE	Lot #1	30	25C	0	0	0	0	0
LCMXO2-256ZE	Lot #2	30	25C	0	0	0	0	0
LCMXO2-640ZE	Lot #1	30	25C	0	0	0	0	0
LCMXO2-2000ZE	Lot #1	30	25C	0	0	0	0	0
LCMXO2-4000ZE	Lot #1	30	25C	0	0	0	0	0

The MachXO2 family uses the exact same Flash cell on all product densities and speed-power versions. The results above includes 8 separate foundry lots of the same flash cell.

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3.4 MachXO2 Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

MachXO2 product family was tested per the JESD22-A114E Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.1 MachXO2 ESD-HBM Data

Product	25-WLCSP (2.5x2.5m, 0.4mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184csBGA (8x8mm, 0.5 mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-7000ZE					HBM>2000V Class 2		HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2
LCMXO2-4000ZE				HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2 by extension	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2
LCMXO2-2000ZE			HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2		HBM>2000V Class 2	HBM>2000V Class 2		
LCMXO2-1200ZE	HBM>2000V Class 2		HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2					
LCMXO2-640ZE			HBM>2000V Class 2	HBM>2000V Class 2						
LCMXO2-256ZE		HBM>2000V Class 2*	HBM>2000V Class 2*	HBM>2000V Class 2* by extension						

- The LCMXO2-256ZE HBM is JESD22-A114E Class 2 starting with die code revision B. See Lattice PCN-07A-12 for details.
- Qual-by-Extension HBM uses the smallest package for a given product because the lowest package parasitics have the worst-case performance. All larger packages for a given product are qualified by an extension.
- WLCSP HBM performance is the lowest package inductance and exceeds 2000V. This characterization exceeds the JEDEC requirements which is device specific in a single package.

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Table 3.4.1 MachXO2 ESD-HBM Data (continued)

Product	32-QFN (5x5mm, 0.5mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184csBGA (8x8mm, 0.5mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-7000HC/HE					HBM>2000V Class 2		HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2
LCMXO2-4000HC/HE				HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2 by extension	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2
LCMXO2-2000HC/HE			HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2		HBM>2000V Class 2	HBM>2000V Class 2		
LCMXO2-1200HC			HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2					
LCMXO2-640HC			HBM>2000V Class 2	HBM>2000V Class 2						
LCMXO2-256HC	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2	HBM>2000V Class 2						

- HBM classification for Commercial/Industrial products, per JESD22-A114E
- All HBM levels indicated are dual-polarity (±)
- Qual-by-Extension HBM uses the smallest package for a given product because the lowest package parasitics have the worst-case performance. All larger packages for a given product are qualified by an extension.

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Electrostatic Discharge-Machine Model:

MachXO2 product family was tested per the JESD22-A115C Electrostatic Discharge (ESD) Sensitivity Testing, Machine Model (MM) procedure.

All units were tested at 25°C and +105°C prior to reliability stress and after reliability stress. No failures were observed within the passing stress level.

Table 3.4.2 MachXO2 ESD-MM Data

Product	32-QFN (5x5mm, 0.5mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184-csBGA (8x8mm, 0.5mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)*	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-2000HC/HE								>50V		
LCMXO2-2000HC/HE								>100V		
LCMXO2-2000HC/HE								>200V		

- All ESD-MM levels indicated are dual-polarity (±)
- ESD-MM stress level for Commercial/Industrial products, per JESD22-A115C
- ESD-MM stress level was performed at 3 voltages to ensure full coverage

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Electrostatic Discharge-Charged Device Model:

MachXO2 product family was tested per the JESD22-C101D, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.3 MachXO2 ESD-CDM Data

Product	32-QFN (5x5mm, 0.5mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184-csBGA (8x8mm, 0.5mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-7000ZE					CDM>1kV Class IV		CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV
LCMXO2-4000ZE				CDM>900V Class III	CDM>900V Class III	CDM>900V Class III by extension	CDM>900V Class III	CDM>1kV Class IV	CDM>750V Class III	CDM>750V Class III
LCMXO2-2000ZE			CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV		CDM>1kV Class IV	CDM>1kV Class IV		
LCMXO2-1200ZE			CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV					
LCMXO2-640ZE			CDM>1kV Class IV	CDM>1kV Class IV						
LCMXO2-256ZE		CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV						

- CDM classification for Commercial/Industrial products, per JESD22-C101D
- All CDM levels indicated are dual-polarity (±)
- Qual-by-Extension CDM uses the largest package for a given product because the largest bulk package capacitance has the worst-case CDM performance. All smaller packages for a given product are qualified by an extension.

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Table 3.4.3 MachXO2 ESD-CDM Data (continued)

Product	32-QFN (5x5mm, 0.5mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184-csBGA (8x8mm, 0.5mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-7000HC/HE					CDM>1kV Class IV		CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV
LCMXO2-4000HC/HE				CDM>800V Class III	CDM>800V Class III	CDM>800V Class III by extension	CDM>800V Class III	CDM>900V Class III	CDM>800V Class III	CDM>1kV Class IV
LCMXO2-2000HC/HE			CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV		CDM>1kV Class IV	CDM>1kV Class IV		
LCMXO2-1200HC			CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV					
LCMXO2-640HC			CDM>1kV Class IV	CDM>1kV Class IV						
LCMXO2-256HC	CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV	CDM>1kV Class IV						

- CDM classification for Commercial/Industrial products, per JESD22-C101D
- All CDM levels indicated are dual-polarity (±)
- Qual-by-Extension CDM uses the largest package for a given product because the largest bulk package capacitance has the worst-case CDM performance. All smaller packages for a given product are qualified by an extension.

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Latch-Up:

MachXO2 product family was tested per the JEDEC EIA/JESD78A IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were Class tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.4.4 MachXO2 I/O Latch Up >100mA @ HOT (105°C) Data

Product	32-QFN (5x5mm, 0.5mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184-csBGA (8x8mm, 0.5mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-7000					> +/-100mA Class II Level A		> +/-100mA Class II Level A	> +/-100mA Class II Level A	> +/-100mA Class II Level A	> +/-100mA Class II Level A
LCMXO2-4000				> +/-100mA Class II Level A	> +/-100mA Class II Level A	> +/-100mA Class II Level A by extension	> +/-100mA Class II Level A	> +/-100mA Class II Level A	> +/-100mA Class II Level A	> +/-100mA Class II Level A
LCMXO2-2000			> +/-100mA Class II Level A	> +/-100mA Class II Level A	> +/-100mA Class II Level A		> +/-100mA Class II Level A	> +/-100mA Class II Level A		
LCMXO2-1200			> +/-100mA Class II Level A	Class II Level A by extension	> +/-100mA Class II Level A					
LCMXO2-640			> +/-100mA Class II Level A	> +/-100mA Class II Level A						
LCMXO2-256	> +/-100mA Class II Level A	Class II Level A by extension	Class II Level A by extension	> +/-100mA Class II Level A						

- All IO-LU levels indicated are dual-polarity (±)
- Qual-by-Extension Latch Up uses the largest package for a given product because it has access to the most pins. All smaller packages for a given product are qualified by an extension.

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Table 3.4.5 MachXO2 Vcc Latch Up >1.5X @ HOT (105°C) Data

Product	32-QFN (5x5mm, 0.5mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184-csBGA (8x8mm, 0.5mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-7000					> 1.5x Vcc Class II		> 1.5x Vcc Class II	> 1.5x Vcc Class II	> 1.5x Vcc Class II	> 1.5x Vcc Class II
LCMXO2-4000				> 1.5x Vcc Class II	> 1.5x Vcc Class II	> 1.5x Vcc Class II by extension	> 1.5x Vcc Class II	> 1.5x Vcc Class II	> 1.5x Vcc Class II	> 1.5x Vcc Class II
LCMXO2-2000			> 1.5x Vcc Class II	> 1.5x Vcc Class II	> 1.5x Vcc Class II		> 1.5x Vcc Class II	> 1.5x Vcc Class II		
LCMXO2-1200			> 1.5x Vcc Class II	Class II by extension	> 1.5x Vcc Class II					
LCMXO2-640			> 1.5x Vcc Class II	> 1.5x Vcc Class II						
LCMXO2-256	> 1.5x Vcc Class II	Class II by extension	Class II by extension	> 1.5x Vcc Class II						

- Qual-by-Extension Latch Up uses the largest package for a given product because it has access to the most pins. All smaller packages for a given product are qualified by an extension.

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4.0 PACKAGE QUALIFICATION DATA FOR MACHXO2 PRODUCT FAMILY

The MachXO2 product family is offered in TQFP, uc/cs/ca/ftBGA, fpBGA, QFN and WLCSP packages assembled and tested at ASEM in Malaysia, ASET in Kaohsiung, Taiwan, and UTAC/ NEPES in Singapore. This report details the package qualification results of the initial MachXO2 product introductions. Package qualification tests include Surface Mount Pre-Conditioning (SMPC), Temperature Cycling (T/C), Un-biased HAST (UHAST), Biased HAST (BHAST) and High Temperature Storage (HTSL). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection. SMPC is used prior to all other package stresses.

The generation and use of generic data applied across a family of packages emanating from one base assembly process is a Family Qualification, or Qualification by Extension. For the package stresses BHAST, UHAST and HTSL, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package stresses qualification matrix.

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Table 4.0.1 Product-Package Qualification-By-Extension Matrix

Product-Package Combinations	Stress Test	ASET	Advanced Semiconductor Engineering, Malaysia (ASEM)								
		32-QFN (5x5mm, 0.5mm pitch)	64-ucBGA (4x4mm, 0.4mm pitch)	100-TQFP (14x14mm, 0.5mm pitch)	132-csBGA (8x8mm, 0.5mm pitch)	144-TQFP (20x20mm, 0.5mm pitch)	184-csBGA (8x8mm, 0.5mm pitch)	256-caBGA (14x14mm, 0.8mm pitch)	256-ftBGA (17x17mm, 1.0mm pitch)	332-caBGA (17x17mm, 0.8mil pitch)	484-fpBGA (23x23mm, 1.0mm pitch)
LCMXO2-7000	SMPC	Package not offered	Package not offered	Package not offered	Package not offered	MSL3	Package not offered	2	2	MSL3	MSL3
	T/C					1K cycles		2	2	1K cycles	1K cycles
	BHAST					1		2	2	2	264 hours
	UHAST					1		2	2	2	264 hours
	HTSL					1		2	2	2	1K hours
LCMXO2-4000	SMPC	Package not offered	Package not offered	Package not offered	2	1	MSL3	2	2	2	3
	T/C				2	1	1K cycles	2	2	2	3
	BHAST				2	1	264 hours	2	2	2	3
	UHAST				2	1	2	2	2	2	3
	HTSL				2	1	1K cycles	2	2	2	3
LCMXO2-2000	SMPC	Package not offered	Package not offered	1	2	1	Package not offered	2	2	Package not offered	Package not offered
	T/C			1	2	1		2	2		
	BHAST			1	2	1		2	2		
	UHAST			1	2	1		2	2		
	HTSL			1	2	1		2	2		
LCMXO2-1200	SMPC	Package not offered	Package not offered	1	MSL3	MSL3	Package not offered	Package not offered	Package not offered	Package not offered	Package not offered
	T/C			1	1K cycles	1K cycles					
	BHAST			1	264 hours	264 hours					
	UHAST			1	264 hours	264 hours					
	HTSL			1	1K hours	1K hours					
LCMXO2-640	SMPC	Package not offered	Package not offered	1	2	Package not offered	Package not offered	Package not offered	Package not offered	Package not offered	Package not offered
	T/C			1	2						
	BHAST			1	2						
	UHAST			1	2						
	HTSL			1	2						
LCMXO2-256	SMPC	MSL3	MSL3	1	2	Package not offered	Package not offered	Package not offered	Package not offered	Package not offered	Package not offered
	T/C	1K cycle	1K cycle	1	2						
	BHAST	96 hours	2	1	2						
	UHAST	N/A	2	1	2						
	HTSL	1K hours	1K hours	1	2						

Notes: 1, 2 & 3 – Qualified by extension from one of the other product-packages within the same packaging technology

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4.1 MachXO2 Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)

(10 Temperature Cycles, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, 260°C Reflow Simulation, 3 passes) performed before all package tests.

MSL3 Packages: TQFP, µcBGA, csBGA, caBGA, ftBGA, fpBGA and QFN

Method: Lattice Procedure # 70-103467, J-STD-020D.1 and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LCMXO2-256	32-QFN	ASET	Lot #1	245**	0	260°C
LCMXO2-256	32-QFN	ASET	Lot #2	246	0	260°C
LCMXO2-256	32-QFN	ASET	Lot #3	246	0	260°C
LCMXO2-256	64ucBGA	ASEM	Lot #1	169	0	260°C
LCMXO2-256	64ucBGA	ASEM	Lot #2	169	0	260°C
LCMXO2-1200	132csBGA	ASEM	Lot #1	308	0	260°C
LCMXO2-1200	132csBGA	ASEM	Lot #2	308	0	260°C
LCMXO2-1200	132csBGA	ASEM	Lot #3	308	0	260°C
LCMXO2-4000	184csBGA	ASEM	Lot #1	255	0	260°C
LCMXO2-4000	184csBGA	ASEM	Lot #2	255	0	260°C
LCMXO2-4000	184csBGA	ASEM	Lot #3	255	0	260°C
LCMXO2-4000	184csBGA	ASEM	Lot #4	80	0	260°C
LCMXO2-4000	184csBGA	ASEM	Lot #5	80	0	260°C
LCMXO2-7000	332caBGA	ASEM	Lot #1	77	0	260°C
LCMXO2-7000	332caBGA	ASEM	Lot #2	77	0	260°C
LCMXO2-1200	144TQFP	ASEM	Lot #1	308	0	260°C
LCMXO2-1200	144TQFP	ASEM	Lot #2	308	0	260°C
LCMXO2-1200	144TQFP	ASEM	Lot #3	308	0	260°C
LCMXO2-7000	144TQFP	ASEM	Lot #1	77	0	260°C
LCMXO2-7000	144TQFP	ASEM	Lot #2	77	0	260°C
LCMXO2-7000	484fpBGA	ASEM	Lot #1	307*	0	250°C
LCMXO2-7000	484fpBGA	ASEM	Lot #2	306*	0	250°C
LCMXO2-7000	484fpBGA	ASEM	Lot #3	305*	0	250°C

* 6 units had 1 corner solder ball knocked off due to handling damage. Sample size reduced accordingly for each of three assembly lots.
** 1 unit failed for "package damage "due to handling damage. Sample size reduced by one.

MachXO2 Cumulative SMPC Failure Rate = 0 / 5,074

4.2 MachXO2 Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 “Temperature Cycling”, Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, csBGA, QFN

Stress Duration: 1000 cycles

Stress Conditions: Temperature cycling between -55°C to 125°C

Method: Lattice Procedure # 70-101568 and JESD22-A104C, Condition B

Table 4.2.1 Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	500 Cycles	1000 Cycles
LCMXO2-256	32QFN	ASET	Lot #1	82	0	0
LCMXO2-256	32QFN	ASET	Lot #2	82	0	0
LCMXO2-256	32QFN	ASET	Lot #3	82	0	0
LCMXO2-256	64ucBGA	ASEM	Lot #1	80	0	0
LCMXO2-256	64ucBGA	ASEM	Lot #2	78	0	0
LCMXO2-1200	132csBGA	ASEM	Lot #1	77	0	0
LCMXO2-1200	132csBGA	ASEM	Lot #2	77	0	0
LCMXO2-1200	132csBGA	ASEM	Lot #3	77	0	0
LCMXO2-4000	184csBGA	ASEM	Lot #1	78	0	0
LCMXO2-4000	184csBGA	ASEM	Lot #2	78	0	0
LCMXO2-4000	184csBGA	ASEM	Lot #3	78	0	0
LCMXO2-7000	332caBGA	ASEM	Lot #1	77	0	0
LCMXO2-7000	332caBGA	ASEM	Lot #2	77	0	0
LCMXO2-1200	144TQFP	ASEM	Lot #1	77	0	0
LCMXO2-1200	144TQFP	ASEM	Lot #2	77	0	0
LCMXO2-1200	144TQFP	ASEM	Lot #3	76*	0	0
LCMXO2-7000	144TQFP	ASEM	Lot #1	77	0	0
LCMXO2-7000	144TQFP	ASEM	Lot #2	77	0	0
LCMXO2-7000	484fpBGA	ASEM	Lot #1	76**	0	0
LCMXO2-7000	484fpBGA	ASEM	Lot #2	76	0	0
LCMXO2-7000	484fpBGA	ASEM	Lot #3	75**	0	0

* 1 unit had a broken lead due to handling damage. Sample size reduced by one.

** 2 units had 1 corner solder ball knocked off due to handling damage. Sample size reduced by one for each of two assembly lots.

MachXO2 Cumulative Temp Cycle Failure Rate = 0 / 1,634

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4.3 MachXO2 Product Family Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity (Condition A), or 264 hours exposure at 110°C and 85% relative humidity (Condition B). Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, csBGA
Stress Conditions: 110°C and 85% RH (Condition B)
Stress Duration: 264 Hrs (Condition B)
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.3.1 Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Temperature	Stress Duration
LCMXO2-1200	132csBGA	ASEM	Lot #1	77	0	110°C	264 Hrs
LCMXO2-1200	132csBGA	ASEM	Lot #2	77	0	110°C	264 Hrs
LCMXO2-1200	132csBGA	ASEM	Lot #3	77	0	110°C	264 Hrs
LCMXO2-1200	144TQFP	ASEM	Lot #1	77	0	110°C	264 Hrs
LCMXO2-1200	144TQFP	ASEM	Lot #2	77	0	110°C	264 Hrs
LCMXO2-1200	144TQFP	ASEM	Lot #3	77	0	110°C	264 Hrs
LCMXO2-7000	484fpBGA	ASEM	Lot #1	76	0	110°C	264 Hrs
LCMXO2-7000	484fpBGA	ASEM	Lot #2	77	0	110°C	264 Hrs
LCMXO2-7000	484fpBGA	ASEM	Lot #3	76	0	110°C	264 Hrs

MachXO2 Cumulative Unbiased HAST failure Rate = 0 / 691

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4.4 MachXO2 Product Family THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are either 96 hours exposure at 130°C and 85% relative humidity (Condition A), or 264 hours exposure at 110°C and 85% relative humidity (Condition B). Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, csBGA, QFN

Stress Conditions: Vcc= 1.26V/ V_{CCIO} = 3.3V, 110°C and 85% RH (Condition B)

Stress Duration: 264 Hrs (Condition B)

Method: Lattice Procedure # 70-101571 and JESD22-A110B

Table 4.4.1 Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Temperature	Stress Duration
LCMXO2-256	32QFN	ASET	Lot #1	81*	0	130°C	96 Hrs
LCMXO2-256	32QFN	ASET	Lot #2	82	0	130°C	96 Hrs
LCMXO2-256	32QFN	ASET	Lot #3	82	0	130°C	96 Hrs
LCMXO2-1200	132csBGA	ASEM	Lot #1	45	0	110°C	264 Hrs
LCMXO2-1200	132csBGA	ASEM	Lot #2	45	0	110°C	264 Hrs
LCMXO2-1200	132csBGA	ASEM	Lot #3	77	0	110°C	264 Hrs
LCMXO2-4000	184csBGA	ASEM	Lot #3	85	0	110°C	264 Hrs
LCMXO2-4000	184csBGA	ASEM	Lot #4	80	0	110°C	264 Hrs
LCMXO2-4000	184csBGA	ASEM	Lot #5	80	0	110°C	264 Hrs
LCMXO2-1200	144TQFP	ASEM	Lot #1	77	0	110°C	264 Hrs
LCMXO2-1200	144TQFP	ASEM	Lot #2	45	0	110°C	264 Hrs
LCMXO2-1200	144TQFP	ASEM	Lot #3	45	0	110°C	264 Hrs
LCMXO2-7000	484fpBGA	ASEM	Lot #1	77	0	110°C	264 Hrs
LCMXO2-7000	484fpBGA	ASEM	Lot #2	76	0	110°C	264 Hrs
LCMXO2-7000	484fpBGA	ASEM	Lot #3	76	0	110°C	264 Hrs

* 1 unit failed for "package damage "due to handling damage. Sample size reduced by one.

MachXO2 Cumulative BHAST failure Rate = 0 / 1,053

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4.5 MachXO2 Product Family High Temperature Storage Life (HTSL)

High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103C, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours. Prior to High Temperature Storage, all MachXO2 devices are subjected to Surface Mount Preconditioning as mentioned in Table 4.1.1. This is a relatively new requirement consistent with JESD47F for Pb-free, wirebonded packages.

MSL3 Packages: TQFP, csBGA, QFN

Stress Duration: 168, 500, 1000, 1500 hours.

Temperature: 150°C (ambient)

Method: Lattice Document # 87-101925 and JESD22-A103C / JESD22-A117A

Table 4.5.1 MachXO2 High Temperature Storage Life Results

Product Name	Package	Lot #	Lot Number	Quantity	# of Fails	500 Hrs Result	1000 Hrs Result	1500 Hrs Result	Cumulative Hours
LCMXO2-256	32QFN	ASET	Lot #1	81**	0	0	0	N/A	81,000
LCMXO2-256	32QFN	ASET	Lot #2	82	0	0	0	N/A	82,000
LCMXO2-256	32QFN	ASET	Lot #3	82	0	0	0	N/A	82,000
LCMXO2-256	64ucBGA	ASEM	Lot #1	77	0	0	0	0	115,500
LCMXO2-256	64ucBGA	ASEM	Lot #2	80	0	0	0	0	120,000
LCMXO2-1200	132csBGA	ASEM	Lot #1	77	0	0	0	0	115,500
LCMXO2-1200	132csBGA	ASEM	Lot #2	77	0	0	0	0	115,500
LCMXO2-1200	132csBGA	ASEM	Lot #3	77	0	0	0	N/A	77,000
LXMXO2-4000	184csBGA	ASEM	Lot #1	80	0	0	0	0	80,000
LXMXO2-4000	184csBGA	ASEM	Lot #2	80	0	0	0	0	80,000
LXMXO2-4000	184csBGA	ASEM	Lot #3	80	0	0	0	0	80,000
LCMXO2-1200	144TQFP	ASEM	Lot #1	77	0	0	0	0	115,500
LCMXO2-1200	144TQFP	ASEM	Lot #2	77	0	0	0	N/A	77,000
LCMXO2-1200	144TQFP	ASEM	Lot #3	77	0	0	0	N/A	77,000
LCMXO2-7000	484fpBGA	ASEM	Lot #1	76*	0	0	0	0	114,000
LCMXO2-7000	484fpBGA	ASEM	Lot #2	77	0	0	0	0	115,500
LCMXO2-7000	484fpBGA	ASEM	Lot #3	77	0	0	0	0	115,500

* 1 unit failed for “opens” due to handling damage. Sample size reduced by one.
** 1 unit failed for “opens” due to handling damage. Sample size reduced by one.

MachXO2 Cumulative HTSL failure Rate = 0 / 1,334
MachXO2 Cumulative HTSL device hours = 1,643,000

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5.0 BOARD LEVEL RELIABILITY (BLR) STRESS METHODS

Reliability testing methods for surface mount electronic components in Wafer Level Chip Scale Packaging (WLCSP) assembled onto printed circuit boards (PCB) are focused on the stresses observed by the manufacturing and test processes and the applications associated with handheld electronic products. The handheld electronic products fit into the consumer and portable market segments with products such as cameras, calculators, cell phones, pagers, palm size PCs, PCMCIA cards, and the like.

Special daisy chain electronic components are constructed for board level reliability (BLR) testing to emulate as closely as possible, the design, material sets and assembly processes of the actual product being qualified.

BLR PCB test boards are designed per JEDEC JESD22-B111 requirements: 1mm thick board with 1+6+1 stack (8 layers) layup coated with OSP “Organic Surface Protection”. Units are arranged in a 3x5 configuration on the board measuring 77mm x 132mm. One side provides VIP “Via-In-Pad” connections to the BGA and the flip side provides NVIP “No-VIP” (surface-trace) connections. The design of pad to surface traces must avoid trace cracks. BGA balls mount to NSMD “Non Solder Mask Defined” pads on the PCB.

Board Level Slow-Temperature Cycling (the slowest speed BLR stress) is intended to evaluate and compare the PCB performance of surface mount electronics components in an environment that accelerates solder joint fatigue and creep for handheld electronic products and applications. Pass/fail event detection is accomplished using resistance measurements. All stress tests are performed in accordance with IPC-JEDEC9701A & JESD22-A104D, condition G, soak mode 2. Repeated slow-temperature cycling of printed circuit boards from -40C to +125C, for up to 3,000 cycles. Handheld electronic products passing criteria is 1,000 cycles.

Board Level Cyclic Bend Test (the medium speed BLR stress) is intended to evaluate and compare the PCB performance of surface mount electronics components in an environment that accelerates various assembly and test operations and actual use conditions such as repeated key-presses in mobile phone during the life of the product for handheld electronic products and applications. Pass/fail event detection is accomplished using datalogging ‘opens’ detectors. All stress tests are performed in accordance with IPC-JEDEC9702 & JEDEC JESD22-B113A. Repeated bending of printed circuit boards at 1 to 3 Hz cyclic frequency for up to 200,000 cycles with maximum cross-head displacement of 4 mm. Handheld electronic products passing criteria is 20,000 cycles.

Board Level Drop & Mechanical Shock (the instantaneous BLR stress) is intended to evaluate and compare PCB drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment determine the compatibility of the component(s) to withstand moderately severe shocks as a result of suddenly applied forces or abrupt change in motion produced by handling, transportation or field operation. Further, handheld electronic products are more prone to being dropped during

their useful service life because of their size and weight. Pass/fail event detection is accomplished using datalogging 'opens' detectors. All stress tests are performed in accordance with IPC-JEDEC9703 & JEDEC JESD22-B111 (drop) and JESD-B104C (shock). Repeated drop testing of printed circuit boards at 1500g, 0.5 millisecond half-sine pulse and 2900g, 0.3 millisecond half-sine pulse for up to 1,000 drops. Handheld electronic products passing criteria is 30 drops.

All devices stressed through Board Level Reliability Slow-TC, Bend and Drop Testing were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113F "Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing", Moisture Sensitivity Level 1 (MSL1) and 1x 260°C Solder Reflow.

Slow-TC 1st fail is >1,000 cycles = PASS.
Bend testing did not fail after 20,000 cycles = PASS.
Drop testing did not fail after 30 drops = PASS.
Mechanical Shock testing 1st fail is >30 drops = PASS.

Table 5.0.1 Slow-Temperature Cycling, IPC-JEDEC9701A & JEDEC JESD22-A104D condition G, soak mode 2

Assembly Site	Package	Die Size (mm)	Ball Pitch (mm)	Temp Range (C) & Dwell time (min)	Cycles per hour	Sample Size	1st Fail (Cycles)	N (63.2%) (Cycles)	% Fails @ 3000 Cycles
UTAC / NEPES	25-WLCSP	2.546 x 2.492	0.4	-40C to +125C & 7.5 min at each endpoint	1.2	100/lot x 3 lots	1,568	2,785	67.3%

Table 5.0.2 Bend Testing, IPC-JEDEC9702 & JEDEC JESD22-B113A

Assembly Site	Package	Die Size (mm)	Ball Pitch (mm)	Cross-head Displacement & Strain	Frequency (Hz)	Sample Size	1st Fail (Cycles)	N (63.2%) (Cycles)	% Fails @ 200k Cycles
UTAC / NEPES	25-WLCSP	2.546 x 2.492	0.4	4 mm & 1100 ppm strain tensile and compressive	1-3	36/lot x 3 lots	No fails	No fails	No fails

Table 5.0.3 Drop & Mechanical Shock Testing, IPC-JEDEC9703 & JEDEC JESD22-B111 / JESD-B104C

Assembly Site	Package	Die Size	Ball Pitch (mm)	Drop & Shock Waveform	Cycles per hour	Sample Size	1st Fail (Drops)	N (63.2%) (Drops)	% Fails @ 1000 Drops
UTAC / NEPES	25-WLCSP	2.546 x 2.492	0.4	1500 g, 0.5 ms half-sine pulse	450-600	96/lot x 3 lots VIP	No fails @ 30 drops	TBD	TBD
UTAC / NEPES	25-WLCSP	2.546 x 2.492	0.4	2900 g, 0.3 ms half-sine pulse	450-600	45/lot x 1 lots	644	N/A	2.2%

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6.0 MACHXO2 PROCESS WAFER LEVEL RELIABILITY (WLR)

Several key fabrication process related parameters affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 6.0.1 Wafer Level Reliability (WLR) Results

HCI

Device	LVN	LVP	MVN	MVP	HVN	HVP
delta Ids	-10%	-10%	-10%	-10%	-10%	-10%
Celsius	25	25	25	25	25	25
Vgstress	Vd/2	Vd	Vd/2	Vd	Vd/2	Vd
Vds	1.26	-1.26	3.465	-3.465	5.25	-5.25
TTF	3 lots>34yr DC	3 lots>71yr	3 lots>20yr AC	3 lots>684yr	3 lots >3.5e6 s DC*	3 lots >1e9 s DC*

TDDB

Device	LVN	LVP	MVN	MVP	HVN	HVP	Intermediate IMD	Semi-Global IMD
Celsius	100	100	100	100	100	100	100	100
Vg	1.26	-1.26	3.465	-3.465	5.25	-5.25	3.465	3.465
Max Area	2.2 cm^2	22 cm^2	1 cm^2	2.5 cm^2	5e-4 cm^2	5e-4 cm^2	L/S=100nm	L/S=200nm
0.1% TTF	3 lots>2.5e5 yr	3 lots>1.4e3 yr	3 lots>25yr	3 lots>390 yr	3 lots>1.2e3 yr	3 lots>20 yr	3 lots>229yr	3 lots>6690yr

NBTI

Device	LVP	MVP
delta Vth	50mv	100mv
Celsius	100	100
Vg	-1.26	-3.465
TTF	3 lots>5.8e5 yr	3 lots>4.2e3 yr

EML

Device	Intermediate	Semi-Global	Global	Top Al
Celsius	100	100	100	100
delta R	+5%	+5%	+5%	+5%
Jmax	6.65E+05	6.65E+05	6.65E+05	2.85E+05
0.1% TTF	3 lots>380 yr	3 lots>77 yr	3 lots>22 yr	3 lots>70yr

SM

Device	Intermediate	Semi-Global	Global
delta R	+100%	+100%	+100%
Celsius	100	100	100
TTF	3 lots>2400 yr	3 lots>328 yr	3 lots>1.1e4 yr

Note: Reliability life times are based on listed temperature and use conditions. A Detailed WLR report is available upon request. Lattice Semiconductor Corporation document #73-106883.

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7.0 MACHXO2 SOFT ERROR RATE DATA

Soft Error Rate (SER) testing is conducted to characterize the sensitivity of SRAM storage and device logic elements to High Energy Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device, and result in changes in the internal electrical states of the device. While these changes do not cause physical damage to the device, they can cause a logical error in device operation.

Neutron SRAM SER Rate – This characteristic is the rate of upset of Configuration RAM and Embedded Block RAM (EBR) cells during neutron testing. Devices were configured with a logic pattern, exposed to measured neutron doses, and the device configuration was read back from the device. Changed bits are identified through pattern comparison. Neutron testing is normalized to the published neutron flux rate for New York City at sea level. This rate is measured as Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities.

Alpha SRAM SER Rate – This characteristic is the rate of upset of Configuration RAM and Embedded Block RAM (EBR) cells during Alpha particle testing. Devices were configured with a logic pattern, exposed for a fixed time period to a calibrated Alpha particle source, and the device configuration was read back from the device. Changed bits are identified through pattern comparison. Alpha particle testing is normalized to a background rate of 0.001Alpha/cm2-hr based on characterization of packaging materials. This rate is measured at Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities as Failures in Time (FITs) normalized per million bits in the device to allow for translation across the device families densities.

All testing conforms to JEDEC JESD-89.

Table 7.0.1 MachXO2 MEASURED FITs / Mb

Stress / Structure	SRAM Type	MachXO2 Measured Fuses	Failures in Time per Megabit (FITs/Mb)
High Energy Neutron	Configuration RAM	359,640	363
	* EBR	73,728	611
Alpha Particle	Configuration RAM	359,640	128
	* EBR	73,728	363

* The EBR SER data was taken on the ECP3. The ECP3 shares the same base technology and SRAM cell.

Note: Detailed MachXO2 and ECP3 SER reports are available upon request. Lattice Semiconductor Corporation documents #25-106920 and #25-106669 respectively.

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8.0 MACHXO2 ADDITIONAL FAMILY DATA

Table 8.0.1 MachXO2 Package Assembly Data – BGA & TQFP

Package Attributes / Assembly Sites	UTAC/NEPES	ASET	ASEM	ASEM	ASEM
Die Family (Product Line)	LCMXO2	LCMXO2	LCMXO2	LCMXO2	LCMXO2
Fabrication Process Technology	65nm CMOS (CS200FL)	65nm CMOS (CS200FL)	65nm CMOS (CS200FL)	65nm CMOS (CS200FL)	65nm CMOS (CS200FL)
Package Assembly Site	Singapore	Kaohsiung, Taiwan	Malaysia	Malaysia	Malaysia
Package Type	WLCSP	QFN	ucBGA, csBGA, caBGA & ftBGA	TQFP	fpBGA
Ball/Lead Counts	25	32	64, 132, 184, 256/332 & 256 respectively	100 & 144	484
Die Preparation / Singulation	wafer saw	wafer saw / full cut	wafer saw / full cut	wafer saw / full cut	wafer saw / full cut
Die Attach Material	n/a	Hitachi EN-4900F	Ablebond 2100A	Ablebond 3230	Ablebond 2100A
Mold Compound Supplier/ID	n/a	Sumitomo EME-G631H	Hitachi CEL9750ZHF10 ALKU	Hitachi CEL9510HF10	Hitachi 9750HF10A KLU
Wire Bond Material	n/a	Gold (Au)	Gold (Au)	Gold (Au)	Gold (Au)
Wire Bond Methods	n/a	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball	Thermosonic Ball
Substrate Material or Lead Frame	n/a	CU C194	Bismaleimide Triazine HL83X Series	n/a	Bismaleimide Triazine HL83X Series
Lead Finish Plating or BGA Ball	SAC405	Matte Sn	SAC305	Matte Sn	SAC305
Marking	Laser	Laser	Laser	Laser	Laser

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9.0 REVISION HISTORY

Table 9.0.1 MachXO2 Product Family Qualification Summary revisions

Date	Revision	Section	Change Summary
April 2011	A	---	Initial document release.
October 2011	B	3.0 Silicon & 4.0 Package	Added LCMXO2-7000 qual data. Also added LCMXO2-256/640/2000/4000/7000 ESD/LU data.
March 2012	C	3.1 Life Test 3.4 ESD/LU 3.4 ESD/LU	Added LCMXO2-7000 HTOL 2000 hour data. Added ESD/LU data for the caBGA packages. Added ESD/LU data in support of PCN 07A-12 in section 3.4 for the LCMXO2-256ZE device.
October 2012	D	3.0 QUAL DATA 3.4 ESD/LU 4.0 PACKAGE 4.1 SMPC 4.2 TC 4.4 BHAST 4.5 HTSL 7.0 FAMILY DATA	Added LCMXO2-256-32QFN qual data. Updated SMPC, TC, BHAST, ESD-HBM/CDM, LU data and additional family data.
November 2012	E	3.4 ESD/LU	Updated ESD-MM data.
February 2013	F	4.1 SMPC 4.2 T/C 4.4 BHAST 4.5 HTSL	Added LCMXO2-4000-184csBGA qual data. Updated SMPC, TC, BHAST, HTSL data.
July 2013	G		Updated LCMXO2-4000-184csBGA qual data with the latest results. Added LCMXO2-1200-25WLCSP Board Level Reliability (BLR) stress methods & data. Corrected typographical errors in prior data sets.

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