

Octal Bus Transceiver

With 5 V-Tolerant Inputs

MC74LVX245

The MC74LVX245 is an advanced high speed CMOS octal bus transceiver.

It is intended for two-way asynchronous communication between data buses. The direction of data transmission is determined by the level of the T/ $\bar{R}$ input. The output enable pin ($\overline{OE}$) can be used to disable the device, so that the buses are effectively isolated.

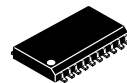
All inputs are equipped with protection circuits against static discharge.

Features

- High Speed: $t_{PD} = 4.7$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25$ °C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V
- These Devices are Pb-Free and are RoHS Compliant

Application Notes

- Do Not Force a Signal on an I/O Pin when it is an Active Output, Damage May Occur
- All Floating (High Impedance) Input or I/O Pins must be Fixed by Means of Pullup or Pulldown Resistors or Bus Terminator ICs
- A Parasitic Diode is Formed between the Bus and V_{CC} Terminals Therefore, the LVX245 cannot be Used to Interface 5.0 V to 3.0 V Systems Directly

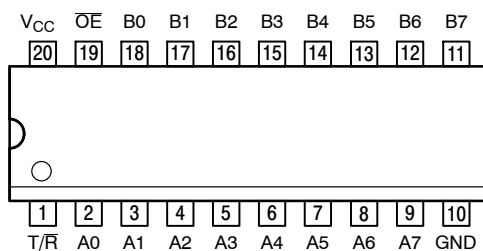


SOIC-20
DW SUFFIX
CASE 751D



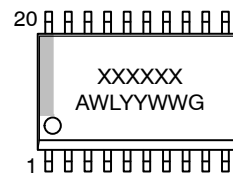
TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT

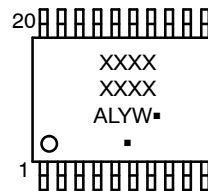


20-Lead (Top View)

MARKING DIAGRAMS



SOIC-20



TSSOP-20

XXXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MC74LVX245

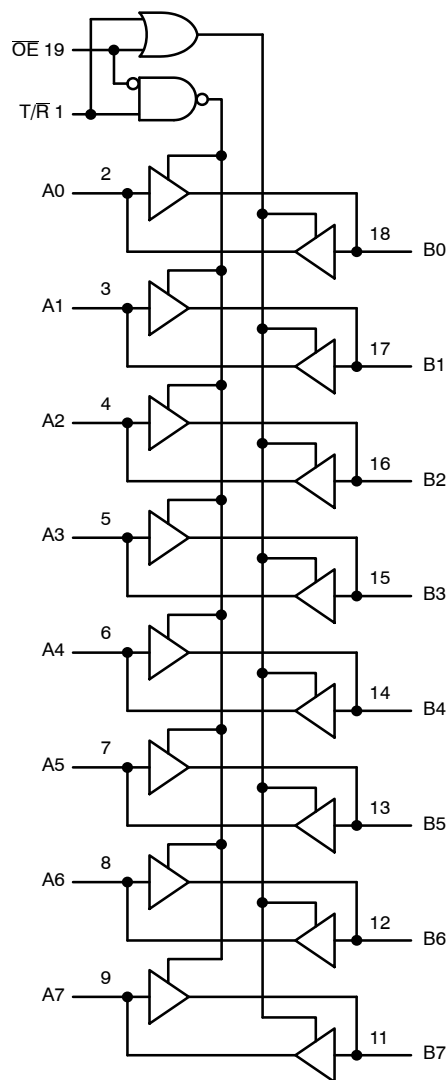


Figure 1. Logic Diagram

Table 1. PIN NAMES

Pins	Function
OE	Output Enable Input
T/R	Transmit/Receive Input
A0–A7	Side A 3-State Inputs or 3-State Outputs
B0–B7	Side B 3-State Inputs or 3-State Outputs

Inputs		Operating Mode Non-Inverting
OE	T/R	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level;
L = Low Voltage Level;
Z = High Impedance State;
X = High or Low Voltage Level and Transitions are Acceptable;
For I_{CC} reasons, Do Not Float Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	–0.5 to +6.5	V	
V _{IN}	DC Input Voltage	–0.5 to +6.5	V	
V _{OUT}	DC Output Voltage	–0.5 to V _{CC} +0.5	V	
I _{IN}	DC Input Current, per Pin	±20	mA	
I _{OUT}	DC Output Current, Per Pin	±25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA	
I _{IK}	Input Clamp Current	–20	mA	
I _{OK}	Output Clamp Current	±20	mA	
T _{STG}	Storage Temperature Range	–65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T _J	Junction Temperature Under Bias	+150	°C	
θ _{JA}	Thermal Resistance (Note 2)	SOIC-20W TSSOP-20	96 150	°C/W
P _D	Power Dissipation in Still Air at 25 °C	SOIC-20W TSSOP-20	1302 833	mW
MSL	Moisture Sensitivity	SOIC-20W All Other Packages	Level 3 Level 1	–
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.573 in	–
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V
I _{LATCHUP}	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage (T/ $\overline{R}$, $\overline{OE}$)	0	5.5	V
V _{I/O}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	–40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25 °C			T _A = -40 to 85 °C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = -50 μA I _{OH} = -50 μA I _{OH} = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{in}	Input Leakage Current	V _{in} = 5.5 V or GND (T/R, OE)	3.6			±0.1		±1.0	μA
I _{oz}	Maximum 3-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	3.6			±0.2 5		±2.5	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions	T _A = 25 °C			T _A = -40 to 85 °C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay Input to Output	V _{CC} = 2.7 V C _L = 15 pF C _L = 50 pF		6.1 8.6	10.7 14.2	1.0 1.0	13.5 17.0	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		4.7 7.2	6.6 10.1	1.0 1.0	8.0 11.5	
t _{PZL} , t _{PZH}	Output Enable Time to High and Low Level	V _{CC} = 2.7 V C _L = 15 pF R _L = 1 kΩ C _L = 50 pF		9.0 11.5	16.9 20.4	1.0 1.0	20.5 24.0	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 15 pF R _L = 1 kΩ C _L = 50 pF		7.1 9.6	11.0 14.5	1.0 1.0	13.0 16.5	
t _{PLZ} , t _{PHZ}	Output Disable Time From High and Low Level	V _{CC} = 2.7 V C _L = 50 pF R _L = 1 kΩ		11.5	18.0	1.0	21.0	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 50 pF R _L = 1 kΩ		9.6	12.8	1.0	14.5	
t _{OSSL} , t _{OSLH}	Output-to-Output Skew (Note 5)	V _{CC} = 2.7 V C _L = 50 pF V _{CC} = 3.3 ± 0.3 V C _L = 50 pF			1.5 1.5		1.5 1.5	ns

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

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CAPACITIVE CHARACTERISTICS

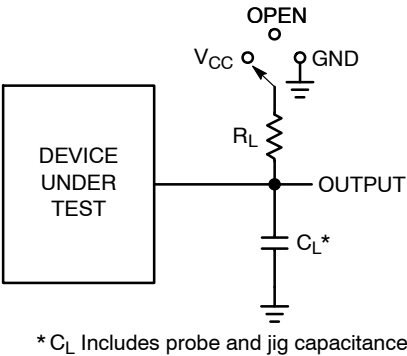
Symbol	Parameter	T _A = 25 °C			T _A = -40 to 85 °C		Unit
		Min	Typ	Max	Min	Max	
C _{in}	Input Capacitance (T/ $\bar{R}$, $\bar{O}\bar{E}$)		4	10		10	pF
C _{I/O}	Maximum 3-State I/O Capacitance		8				pF
C _{PD}	Power Dissipation Capacitance (Note 6)		21				pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 3.3 V, Measured in SOIC Package)

Symbol	Characteristic	T _A = 25 °C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.5	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.5	-0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

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Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	See AC Charact eristics Table	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 2. Test Circuit

SWITCHING WAVEFORMS

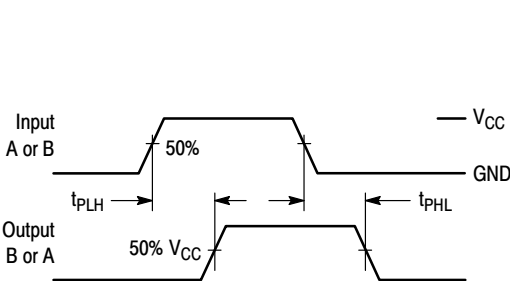


Figure 3.

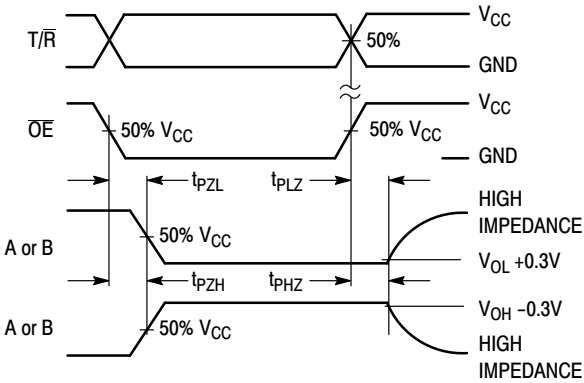


Figure 4.

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74LVX245DWR2G	LVX245G	SOIC-20 WB	1000 / Tape & Reel
MC74LVX245DTR2G	LVX245	TSSOP-20	2500 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MC74LVX245

REVISION HISTORY

Revision	Description of Changes	Date
7	Modified voltage ratings from 7.0 V to 6.5 V.	07/09/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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